



McMOS Handbook

PRODUCTS - CHARACTERISTICS - APPLICATIONS



MOTOROLA *Semiconductors*

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FIRST EDITION

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PREFACE

In developing a specific technology to implement a range of logic devices, various trade-offs must be made. These considerations may cover, for instance, speed versus amplitude of logic swing, as in ECL, or pulse current demands on the power supply versus output drive capability, as in TTL. In general, no logic family has yet been developed which provides a "perfect" solution.

The outstanding performance of CMOS results from the compromises adopted for the various parameters, and represents in many ways a close approach to the ideal. For example, essentially no power is required here to hold the quiescent state; power is consumed only when a logical decision is made. This is in contrast to bipolar circuits, where the steady-state power consumption is considerable, and switching further increases the power demands. Other features of CMOS, such as the flexibility of supply voltage, the high noise immunity, the large fan-in/fan-out capability, the high level of on-chip logic complexity, etc., present unique opportunities to the user.

Here, for the first time, the designer can afford to concentrate on solving the design problems without continually having to compromise the system parameters in order to satisfy semiconductor constraints. MOTOROLA believes that CMOS will rapidly become a major dominant technology, and to assist in optimising system design, it is important that the user understands the performance of CMOS. This book is dedicated to providing a ready source of knowledge, and it is hoped that this stimulates interest in exploiting the unique design situation that CMOS offers.

Mc MOS

HANDBOOK

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Fundamentals of Metal-Oxide- Semiconductors

FUNDAMENTALS OF METAL-OXIDE-SEMICONDUCTORS

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A. HISTORY OF MOSFET TRANSISTOR

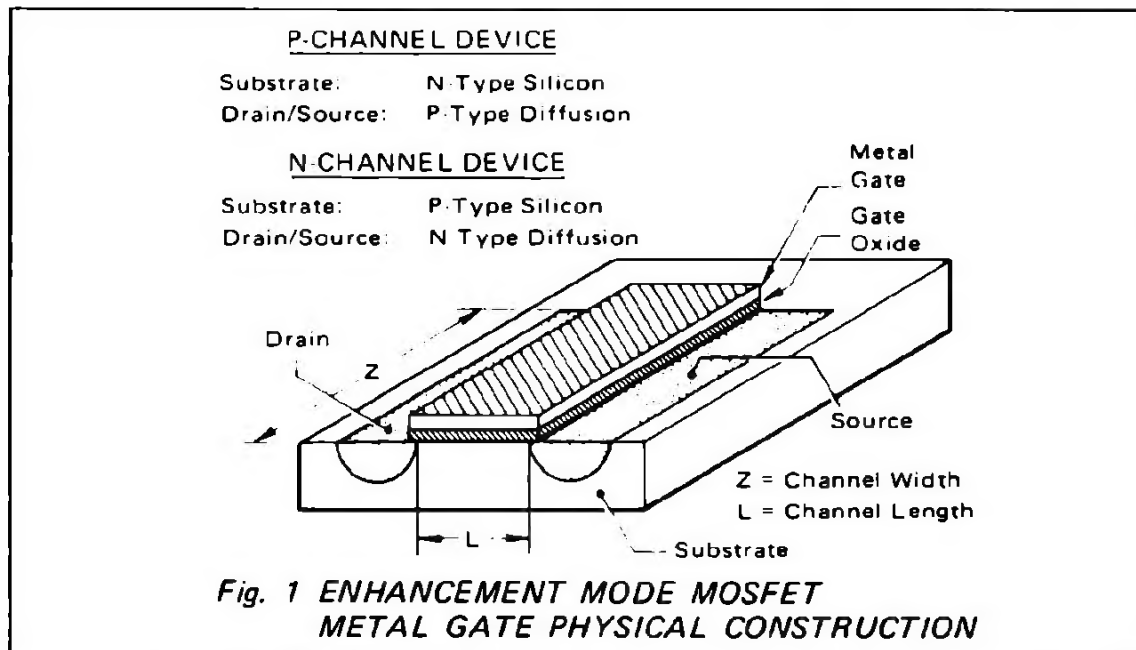
(Metal-Oxide-Semiconductor Field-Effect-Transistor)

The principle of the surface field-effect transistor dates back to the early 1930's. The original proposal for controlling the conduction of a semiconductor by applied electric fields was made by LILIENTHAL (1,2) in 1926 and 1930. In 1935 Oscar NEIL (3) took out a British Patent on the same subject. The use of the surface field-effect to achieve a solid-state amplifier was investigated by the BELL LABORATORIES GROUP, but no practical results were reported until 1948. In that year a letter was published by SHOCKLEY (4) describing how they observed changes in conductivity of thin films of semiconductors by surface charges induced by means of an electric field.

The discovery of the bipolar transistor directed solid-state device development and research in different directions for more than ten years. In approximately 1960 the planar transistor was developed in which doping by diffusion employing the masking properties of the SiO_2 layer can be used as an isolation between the semiconductor and the gate electrode of a field-effect transistor. The use of a thermally oxidized silicon structure in surface field-effect transistors was described by KAHNG and ATALLA (5). The following years brought about an intense activity in this field. It led to a better knowledge and understanding of the thermally oxidized silicon surface. In fact, using the MOS configuration as a sensitive tool for investigation of silicon layers brought deeper understanding of surface effects on semiconductors.

B QUALITATIVE ANALYSIS OF THE ENHANCEMENT MODE MOSFET TRANSISTOR

The MOSFET operation is based upon a voltage-controlled flow of current near the surface of a doped silicon substrate. This operation differs considerably from that of the bipolar transistor, which involves a current controlled flow of current. A MOSFET is a unipolar device involving only one polarity carrier; the bipolar transistor involves both minority and majority carriers. Fig. 1 shows a basic "enhancement mode MOSFET" device. It consists of a silicon substrate with source and drain diffusions. Physically, the drain diffusion is identical to the source diffusion, but they are distinguished when the device is used in a circuit. The region between the source and the drain, named the channel, is under the influence of a metal field plate or gate. The channel is covered by the gate oxide. This insulator prevents current flow from the gate to the substrate resulting in extremely high input impedance for MOSFET devices.



A simplified qualitative understanding of the manner in which an "enhancement mode MOSFET" operates can be obtained by considering the structure shown in Fig. 2. We refer to a P-channel MOSFET on N-type substrate and suppose that there are no trapped charges in the isolator.

For zero gate voltage (zero bias conditions) the charge distribution is shown schematically in Fig. 2a., resulting from the "built-in" junction voltage across P^+-N junctions (N^+ , P^+ indicate heavily doped N and P regions). Since the N-region contains very few holes, the resistance from source to drain will be very high (essentially that of two P-N junction diodes in series opposition maintained at zero bias).

When a negative voltage is applied to the gate (greater than some voltage V_T , the threshold voltage), a positive space-charge is induced in the semiconductor by the negative metal gate charge (Fig. 2b.). This charge Q_1 consists of a heavy concentration of holes close to the surface and a deeper depletion

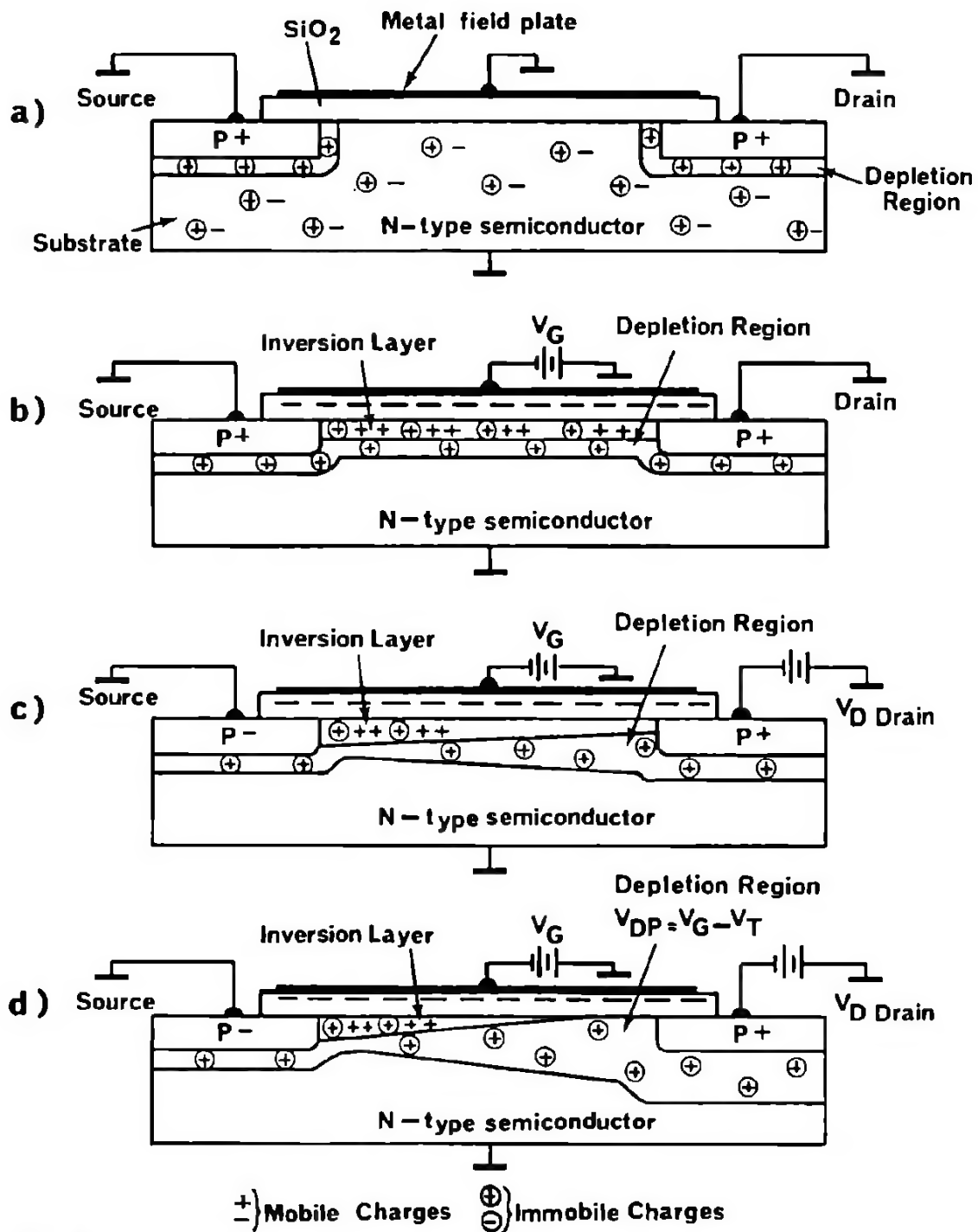


Fig. 2
SIMPLIFIED SCHEMATIC DIAGRAM OF A P-CHANNEL ENHANCEMENT MOSFET UNDER VARIOUS BIAS-CONDITIONS

a) $V_D = V_G = 0$ b.) V_G - NEGATIVE, $V_D = 0$

c.) $|V_G| > |V_D|$; V_D - NEGATIVE, NONSATURATION CONDITIONS

d.) V_G - NEGATIVE; $V_D = V_G$ - SATURATION CONDITIONS

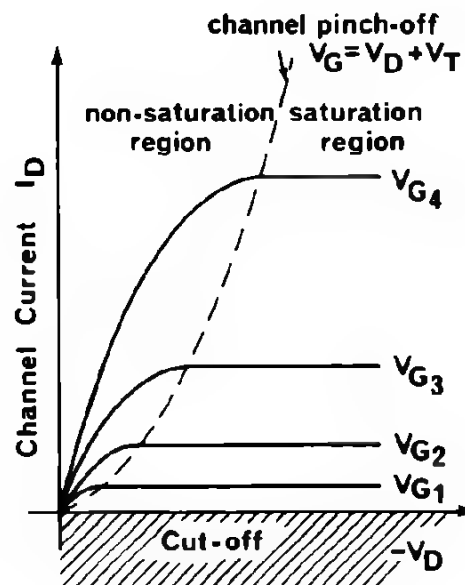
layer of ionized donor atoms from which the free electrons have been repelled. The layer of holes, being opposite in sign to the normal majority carriers, is called the inversion layer, and provides a direct electrical connection between the P^+ regions. Hence, the drain-source resistance is much less than for (a) and can be controlled by the gate voltage. (Similarly, the N-channel device consists of a N^+ doped source and drain diffusion and P-doped silicon substrate. The inversion occurs only in the region between the source and drain diffusions to the depth of 10 to 100 Å. The accumulation of holes in the P-channel MOSFET (or electrons in the N-channel MOSFET) "enhances" current flow between the source and drain. Therefore, the name "enhancement mode".

The situation is a little different when a negative drain-source voltage is applied (Fig. 2c). Current I_D flows from the source to the drain through the inversion region and the ohmic voltage drop in the channel results in the drain end of the channel having a smaller field, normal to the surface, than it has at the source end. The density of holes decreases going from source to drain. The depletion width at the drain end is greater, since the potential difference between the drain and substrate is greater than between the source and substrate.

As the drain voltage V_D is increased with V_G kept constant, the value of the current I_D will increase too. The ohmic voltage drop in the channel means that the field normal to the surface of the drain will be smaller and as a consequence, with the further increase of V_D , the current I_D increases less and less.

When the drain voltage reaches the value V_{DP} , the voltage drop across the channel near the drain falls below the level required to maintain an inversion layer ($V_{DP} = V_G - V_T$), so that pinch-off occurs, the channel near the drain disappears, part of the surface is depleted and no longer inverted (Fig. 2d.). The flow of current now is due to the carriers that flow down the inversion layer and are injected into the depletion region near the drain.

Fig. 3
DRAIN CHARACTERISTICS OF
P-CHANNEL MOS TRANSISTOR



The drain current-voltage characteristics of a P-channel MOS transistor are shown in Fig. 3. There are three regions shown on these characteristics : nonsaturation, saturation and cut-off. These regions of operation may be easily defined according the gate voltage necessary to place the transistor in that condition:

Cut-off $|V_G| < |V_T|$

gate voltage insufficient to form any channel.

Saturation $|V_T| \leq |V_G| \leq |V_D + V_T|$

gate voltage is sufficient to form a channel at the source end but not at the drain end

Nonsaturation $|V_D + V_T| < |V_G|$

gate voltage is sufficiently large to form a channel everywhere

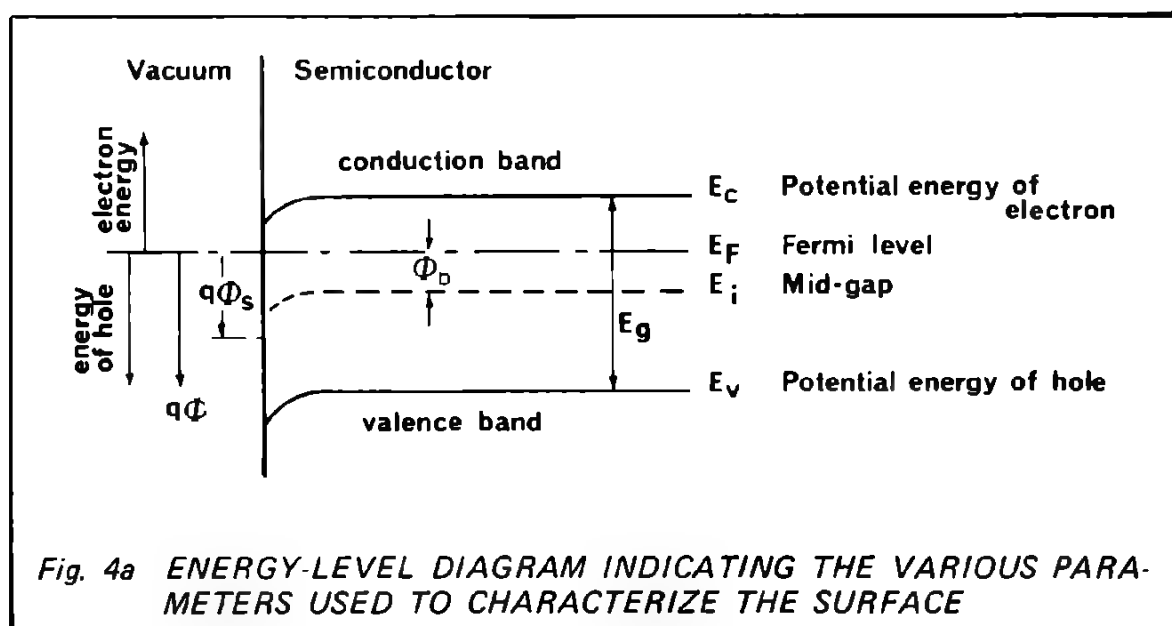
C QUANTITATIVE ANALYSIS OF THE MOS TRANSISTOR *

1. SIMPLE BAND THEORY AND FREE CHARGE CONCENTRATIONS

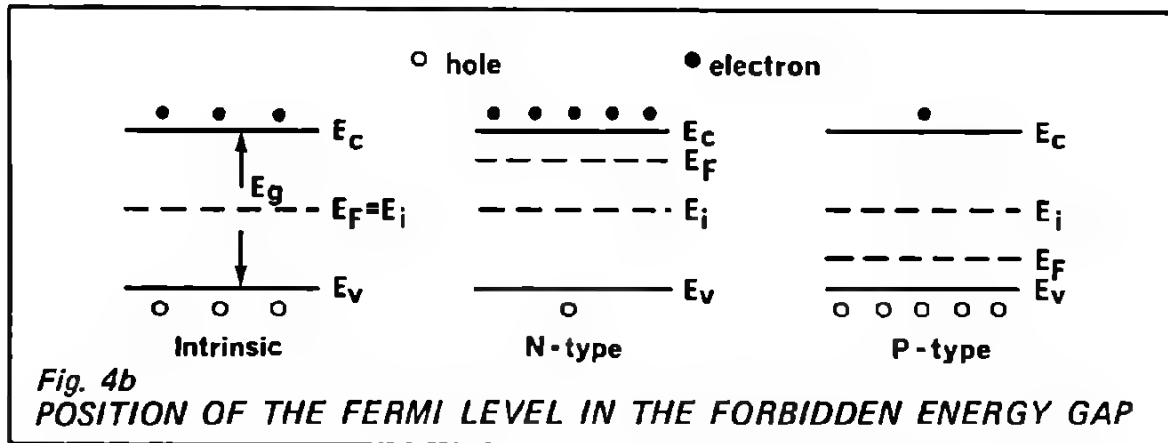
The operation of the enhancement mode MOSFET transistor can be explained on a qualitative basis by studying the energy band diagrams of a silicon surface under various bias conditions.

In Figure 4a there is an energy-band diagram indicating the various parameters used to characterize the surface and bulk of silicon, where E_g is the forbidden band width, or forbidden energy gap. For silicon it is $E_g = 1.1$ eV. The lower band, called the valence band, is that band of energies occupied by the holes that are bound between pairs of atoms, as part of a chemical bond between those atoms. The upper band is the conduction band. Electrons that occupy energy levels in the conduction band are free and, consequently, may take part in the conduction of electronic currents. E_F is the Fermi level. The Fermi level is defined as that energy level at which the probability of finding an electron is just one-half. E_i is the Fermi level for an intrinsic semiconductor. In an intrinsic semiconductor the number of energy states in the conduction and valence bands is the same and the number of electrons in the conduction band and the number of holes in the valence band is also the same. Thus, the Fermi level must be in the middle of the forbidden band.

* For further study of semiconductor theory and the electrical characteristics associated with semiconductor surfaces refer to (5), (6), (9), (10). It is beyond the scope of this publication to develop the concise treatment of semiconductor phenomena. It is assumed that the basics of semiconductor physics are known to the reader.



Since in a N-type semiconductor the concentration of electrons in the conduction band is larger than in the intrinsic case, it follows that in an N-type semiconductor the Fermi level will be shifted upward in the energy-band picture (Figure 4b). In contrast, in a P-type semiconductor the Fermi level will be shifted downward. The type of the semiconductor is identified by the position of the Fermi level in the energy band diagram: If the Fermi level is closer to the conduction band, conduction is mostly provided by electrons - it means that the semiconductor is of N-type. If the Fermi level is closer to the valence band, conduction is provided by holes and the semiconductor is of P-type. (The Fermi level in the forbidden band, exactly mid-way for intrinsic material, varies up or down as dopants are added.)



The concentrations of free electrons, n , and of free holes, p , in the semiconductor bulk in thermal equilibrium using the assumption $N_c \approx N_v$ are given by the following expressions: (5), (8), (9).

$$n = N_c e^{-(E_c - E_F)/kT} = n_i e^{(E_F - E_i)/kT} = n_i e^{q\phi/kT}$$

and

$$p = N_v e^{(E_v - E_F)/kT} = n_i e^{(E_i - E_F)/kT} = n_i e^{-q\phi/kT}$$

where:

- N_c = density of energy levels or states in the conduction band
- N_v = density of energy levels in the valence band
- E_c = energy at the conduction band edge
- E_v = energy at the valence band edge
- q = charge of the electron $q = 1.6 \times 10^{-19}$ coulomb
- k = Boltzmann constant $k = 1.38 \times 10^{-23}$ Joule/°K
- T = absolute temperature

The macroscopic potential, ϕ_b , in the bulk of the semiconductor is defined by:

$$q\phi_b = (E_i - E_f)$$

The electrostatic potential at the surface is called the surface potential and is designated by ϕ_s

From Eq. (1) and (2) one can obtain the product of electron and hole densities:

$$n_p = n_i^2 = N_C N_V e^{-(E_C - E_V)/kT} = N_C N_V e^{-E_g/kT}$$

which is constant for a given temperature. The concentration of donor atoms N_D and the concentration of acceptor atoms N_A can easily be calculated by using the assumption that $n \approx N_D$ and $p \approx N_A$ (concentration of free electrons is equal to the concentration of donor atoms and concentration of free holes is equal to the concentration of acceptor atoms) from Eq. (1) and (2):

$$N_D = n_i e^{q\phi/kT}$$

$$N_A = n_i e^{-q\phi/kT}$$

In the bulk of the material, far from the surface, the energy bands are assumed to be flat. The value of the electrostatic potential in this region is called the bulk potential, ϕ_b (Figure 4a). The free carrier densities in the bulk are given by (5), (6), (9):

$$N_D \approx n_b = n_i e^{q\phi_b/kT}$$

$$N_A \approx p_b = n_i e^{-q\phi_b/kT}$$

The bulk densities n_b and p_b are determined by the doping of the material. The electrostatic potential at the surface is called the surface potential ϕ_s . The free carrier densities at the surface are given by:

$$n_s = n_i e^{q\phi_s/kT} = n_b e^{q(\phi_s - \phi_b)/kT}$$

$$p_s = n_i e^{-q\phi_s/kT} = p_b e^{-q(\phi_s - \phi_b)/kT}$$

The densities n_s and p_s at the surface are determined by the doping material and the voltage applied to the surface.

2. SILICON-SILICON DIOXIDE SYSTEM

The electrical conduction of the silicon near the surface is defined according to whether the mobile density n or p , at (but below) the surface is greater than, less than, or of opposite type to that in the bulk. These states are called accumulation, depletion or inversion.

In present devices the dielectric layer ϵ_{ox} on silicon is silicon dioxide (SiO_2) of a thickness $t_{ox} = 800 - 2000 \text{ \AA}$ and permittivity ϵ_{ox} . On top of this layer is the gate metal, usually aluminium. It creates a capacitance per unit area C_{ox} . The ideal silicon-silicon dioxide system has the bulk properties of silicon persisting up to the surface, and no excess charges are present at the interface (Figure 5). There are no extra surface states. Unfortunately with today's technology, this ideal is very difficult to realize. Within the oxide there always are electric charges present. These charges are created by impurity ions incorporated within the oxide, ionized silicon within the oxide or charges near the silicon to oxide interface due to the termination of the regular silicon crystal lattice. The charges are not mobile and are located close to the surface of the silicon. As a good approximation one may consider all the fixed charges as combined in a sheet of charge Q_{ox} (coulombs/cm²), located at the silicon-oxide interface (7). As indicated in the charge diagrams in Figure 6, Q_{ox} is generally a positive charge. This effective charge, Q_{ox} , has an important effect on the characteristics of the MOS transistor modifying the electric field in both the oxide and the silicon. The charge Q_{ox} can be compensated by applying sufficiently negative gate voltage, so that an equal negative charge $-Q_{ox}$ appears on the metal

$$V_G = -\frac{Q_{ox}}{C_{ox}}$$

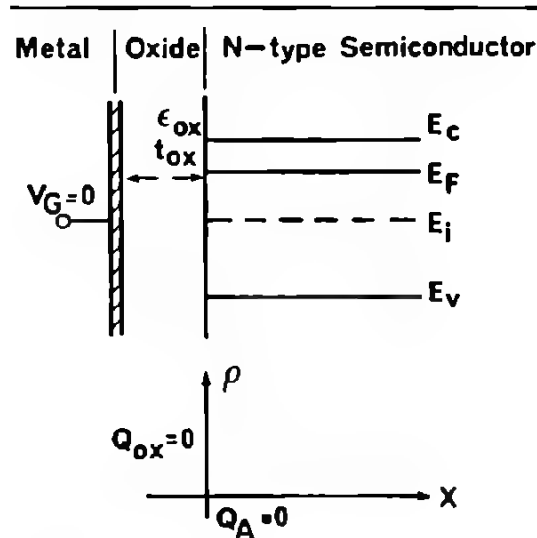


Fig. 5
IDEAL SILICON-SILICON DIOXIDE
SYSTEM. NO BENDING OF THE
ENERGY LEVELS. FLAT BAND
EASE

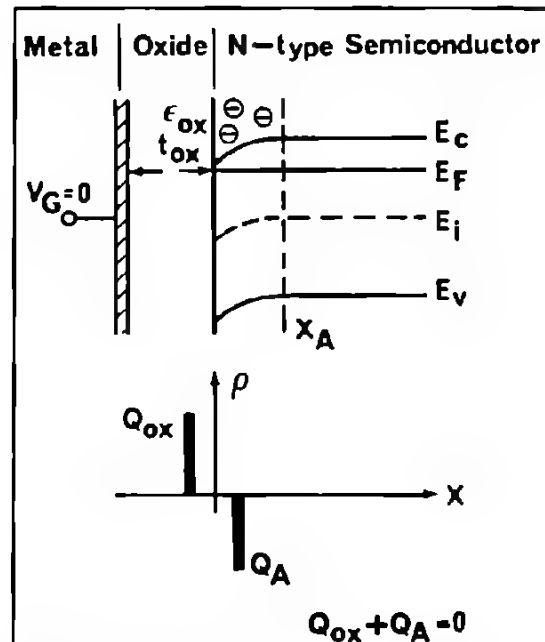


Fig. 6
BAND BENDING DUE TO THE
PRESENCE OF Q_{ox}

The energy-band diagram of a P-channel device under zero applied gate voltage is shown in Figure 6. Because of the positive surface-state charge, negative electrons from within the N-type bulk are attracted to and accumulate at the surface. This results in a downward bending of the conduction and valence bands. The density of electrons at the surface is greater than in the bulk. The Fermi energy level must be closer to the conduction band edge. However, the Fermi level, which is set by the substrate doping in the semiconductor must stay as a horizontal line if the thermodynamic equilibrium holds. It results in a downward bending of the conduction and valence bands. (E_g is constant too !). The closer E_c is bent toward the Fermi level, the heavier the surface concentration of electrons becomes. The positive charge per unit surface area Q_{ox} must be exactly balanced out by the negative charge accumulated near the silicon surface Q_A . The silicon surface is still of the same type as the bulk, but of higher conductivity. If a small positive bias V_G is now applied to the gate, additional band bending and accumulation result (Figure 7). In order to maintain charge neutrality, the total positive charge must be equal to the total negative charge

$$Q_G + Q_{ox} + Q_A = 0.$$

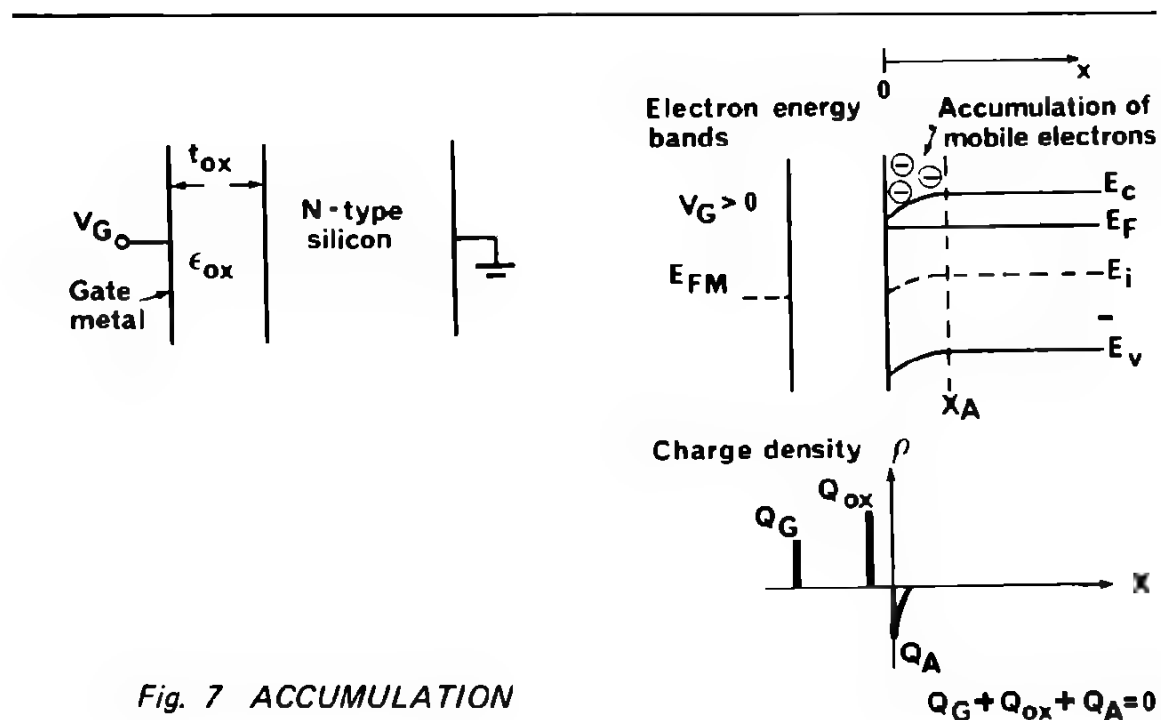


Fig. 7 ACCUMULATION

2. 1. DEPLETION OF MAJORITY CARRIERS FROM THE SURFACE

Applying a small negative voltage to the gate induces a surface positive charge in the N-type semiconductor Figure 8. If a negative voltage is such that it just counters the effect of Q_{ox} , then no bending of the bands exists, a condition which is known as the flat-band case (Figure 5). Further application of a negative gate voltage repels the mobile electrons from the vicinity of the interface, leaving behind a depletion region consisting of non-compensated donor ions and creating the fixed positive charge Q_B of the donor impurity ions. The charge per unit area contained in the semiconductor will then be given by the charge contained within this depletion region (of thickness x_d) as (5), (6), (9) :

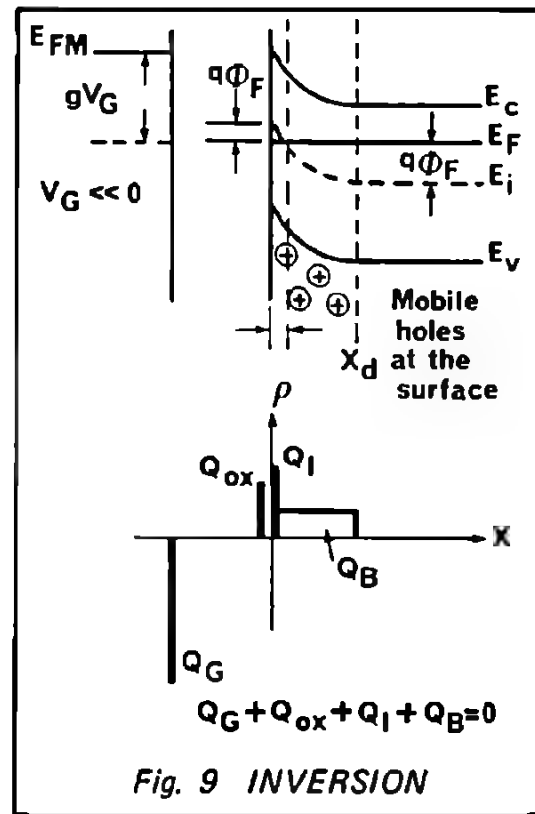
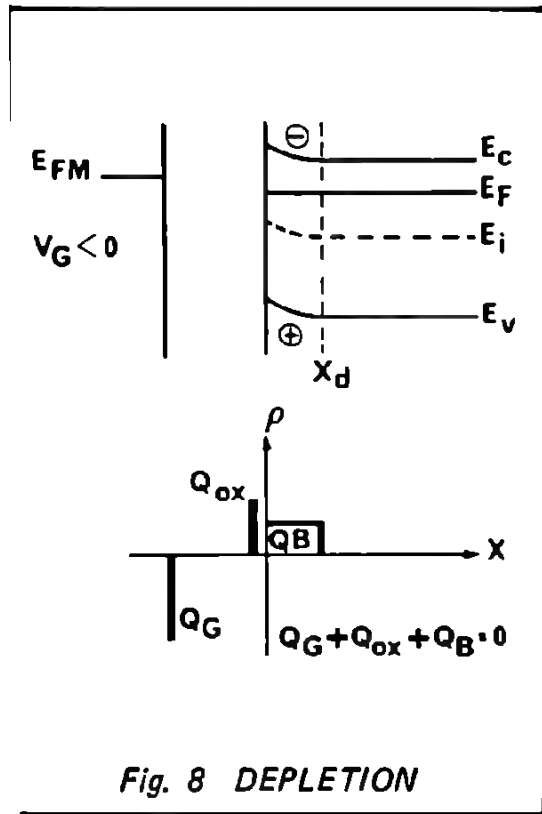
$$Q_B = q N_D x_d$$

The width of the depletion layer x_d is :

$$x_d = \left(\frac{2\epsilon_s [-\phi_b]}{q N_D} \right)^{1/2}$$

where :

ϵ_s = permittivity of the silicon.



As the negative potential applied to the gate is raised, the width of the depletion layer x_d of the surface region will increase. When the intrinsic Fermi level E_i is bent just enough to intersect the Fermi level at $x = 0$, the surface of the semiconductor becomes exactly intrinsic (Figure 9). As the voltage V_G is increased, the energy bands are bent further, E_i rises above E_F near the surface, and the density of holes becomes greater than of electrons. The density of holes remains fairly small until E_i rises considerably above E_F . A good approximate criterion for the onset of this condition of "strong inversion" is that : the strongly inverted surface is considered to be formed only after E_i at the surface is as far above E_F as it was below E_F in the bulk. The total bending of the energy bands corresponds to potential barrier ϕ_s -of twice the Fermi potential and in the opposite direction.

$$\phi_s = -2\phi_F$$

Q_i is the mobile charge per unit area in the inversion layer.

3. THRESHOLD VOLTAGE

The transition between the accumulation and the depletion states occur when the "flat-band" condition is reached. This means that the energy bands in the silicon continue horizontally up to the surface as in Figure 5.

In this condition mobile electrons in the N-type substrate just balance the positive charges of the donor atoms. There is no electric field in the silicon and the net charge density in the silicon is zero.

The electron energies at the Fermi level in the metal and in the semiconductor of a MOS structure will, in general, be different. This energy difference is usually expressed as a difference in work functions. The work function is the energy required to remove an electron from the Fermi level in a given material to vacuum. When the metal of a MOS structure is connected to the semiconductor, electrons will flow from the metal to the semiconductor or vice-versa, until a potential is built up between the two which will counterbalance the difference in work functions. When equilibrium is reached, the Fermi level in the metal is lined up with the Fermi level in the semiconductor with an electrostatic potential variation from one region to the other.

The effect of a work function difference on MOSFET characteristics is defined by the flat-band voltage V_{FB} ; the gate voltage necessary to counterbalance the work function difference is :

$$V_{FB} = \phi_M - \phi_{Si} = \phi_{MSi}$$

where:

ϕ_M = the work function of the metal

ϕ_{Si} = the work function of the silicon.

however, the gate voltage necessary to achieve the flat-band condition is also dependent on the oxide charge Q_{ox} . Under flat-band conditions there is no electric field in the silicon (Figure 10).

From equations (11) and (15), the gate voltage, V_{FB} to cause the flat band condition is :

$$V_G = V_{FB} = \phi_{MSi} - \frac{Q_{ox}}{C_{ox}}$$

The threshold voltage, V_T , is the gate voltage required to bring about strong inversion. This voltage is the flat-band voltage plus the band bending to reach strong inversion, plus the voltage necessary to generate the electric field that holds the Q_B in the depletion region.

The depletion region charge Q_B requires a charge $-Q_B$ on the metal gate, which in turn requires a gate voltage $-Q_B / C_{ox}$. Adding these terms, for the V_T (at the onset of strong inversion) we have :

$$V_T = V_{FB} + \phi_s - \frac{Q_B}{C_{ox}}$$

and using equation (16) :

$$V_T = \phi_{MSi} + \phi_s - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B}{C_{ox}}$$

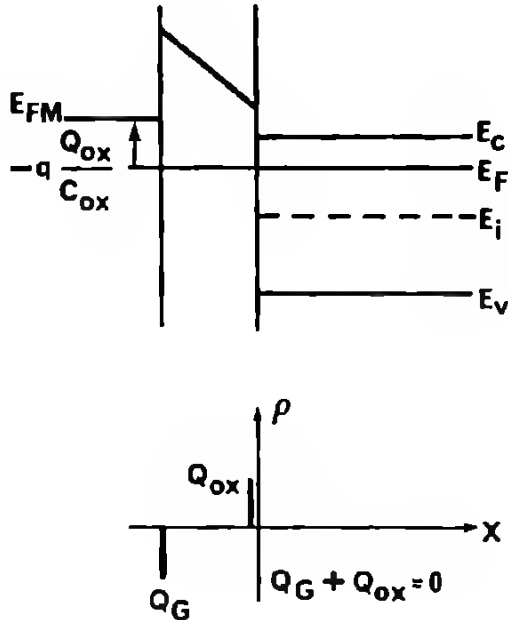


Fig. 10
ENERGY-BAND DIAGRAM AND
CHARGE DENSITY DISTRIBUTION
FOR THE FLAT BAND CASE
WITH PRESENCE OF Q_{ox} AND
THE DIFFERENCE IN THE WORK
FUNCTION BETWEEN THE
SILICON AND METAL.

4. DRAIN CHARACTERISTICS OF MOS TRANSISTOR

The basic theory of the MOS transistor was first presented by Ihantola (8). Sah (12) in his work, included the effects of the oxide charge and the interface properties of the material used in the construction. The theory was further extended by Ihantola and Moll (11), Sah and Pao (13). Here simplified theory of the drain characteristics of the MOS transistor will be developed just to show the principal behavior of MOSFET devices.

4. 1. NON-SATURATION DRAIN CURRENT

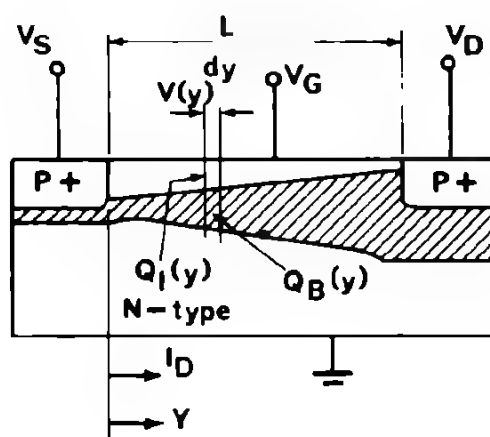
Figure 11 illustrates the structure of a MOS transistor with an N-type substrate. The metal gate completely covers the area lying between the source and drain contacts. The P⁺ regions, forming source and drain, are of the same conductivity type as the inversion layer. In the absence of any inversion layer the drain current becomes negligible since the drain-substrate junction is normally reverse biased.

Let Z be the channel width, L the channel length (source-drain spacing), and $V(y)$ the potential of the surface of the channel with respect to the origin of the coordinate system.

For small drain voltages, the channel induced between source and drain essentially behaves like a resistor. Its resistance is directly proportional to the L and inversely proportional to Z . If μ is the mobility of the charges in the inversion layer and Q_i the charge density of electrons in the inversion layer, then

$$R = \frac{L}{Z\mu Q_i}$$

Fig. 11
ELEMENTAL SECTION OF THE
CHANNEL EMPLOYED IN THE
DERIVATION OF THE CURRENT-
VOLTAGE CHARACTERISTICS
OF MOSFET



The voltage drop across an elemental section (Figure 11) of the channel is given by :

$$dV = I_D dR = \frac{I_D dy}{Z\mu Q_I(y)}$$

This equation is analogous to the previous one.

$Q_I(y)$ begins to form only when the gate voltage is equal to the threshold voltage. With V on the channel, the voltage across the wide capacitor is $V_G - V$, and the charge $Q_I(y)$ in the channel inversion layer is:

$$Q_I(y) = -C_{ox}(V_G - V_T - V)$$

Using Eq. (18) for V_T , and Eq. (12) for Q_B and substituting into Eq. (20) gives

$$dV = I_D dR = \frac{I_D dy}{Z\mu C_{ox} (V_G - \phi_{MSi} - \phi_s + \frac{Q_{ox}}{C_{ox}} + \frac{2\epsilon_s q N_D (-V - \phi_s)^{1/2}}{C_{ox}} - V)}$$

It is convenient to write Eq. (21) in the following form:

$$I_D dy = \mu Z C_{ox} (V_G - \phi_{MSi} - \phi_s + \frac{Q_{ox}}{C_{ox}} - V + \frac{2\epsilon_s q N_D (-V - \phi_s)^{1/2}}{C_{ox}}) dV$$

Forming the integral from $y = 0$ to $y = L$ with boundary conditions $V = V_{SS} = 0$ at the source and $V = V_{DS}$ at the drain results in

$$I_D \int_0^L dy = \mu Z C_{ox} [(V_G - \phi_{MSi} - \phi_s + \frac{Q_{ox}}{C_{ox}}) \int_{V_{SS}=0}^{V_{DS}} dV - \int_{V_{SS}=0}^{V_{DS}} V dV + \frac{(2\epsilon_s q N_D)^{1/2} V_{DS}}{C_{ox}} \int_{V_{SS}=0}^{V_{DS}} (-V - \phi_s)^{1/2} dV]$$

From which:

$$I_D = \mu C_{ox} \frac{Z}{L} [(V_G - \phi_{MSi} - \phi_s + \frac{Q_{ox}}{C_{ox}}) V_{DS} - \frac{1}{2} V_{DS}^2 - \frac{4(\epsilon_s q N_D)^{1/2}}{3 C_{ox}} [(-V_{DS} - \phi_s)^{3/2} - (-\phi_s)^{3/2}]$$

If the charge, Q_B , in the depletion region is considered to be constant

$$Q_B = (2\epsilon_s q N_D [-\phi_s])^{1/2}$$

equation (23) will be simplified to

$$I_D = \mu C_{ox} \frac{Z}{L} (V_G - \phi_{MSi} - \phi_s + \frac{Q_{ox}}{C_{ox}} + \frac{Q_B}{C_{ox}}) V_{DS} - \frac{1}{2} V_{DS}^2$$

Using Eq. (18) for V_T then

$$I_D = \mu C_{ox} \frac{Z}{L} [(V_G - V_T) V_{DS} - \frac{1}{2} V_{DS}^2]$$

Equation (24) is called the SAH Equation after his first application to the MOS transistor. This is a good approximation for most cases and, because of its reduced complexity, it is usually used in most design work.

4. 2. SATURATION

In developing Eq. (25) Q_I was assumed to always be a finite quantity. However, as V_{DS} is increased, there comes a point at which Q_I at the drain becomes zero. This is the "pinch-off" point. The expression for the drain voltage at which pinch-off occurs, V_{DP} , can be found from equation (21) for the inversion layer.

$$Q_I = -C_{ox} (V_G - V_T - V) = 0 \quad (26)$$

When this relation holds, the transistor is in the saturation region and V_{DP} is just equal to the voltage V , so

$$V_{DP} = V_G - V_T$$

The equation for the current can be found by placing

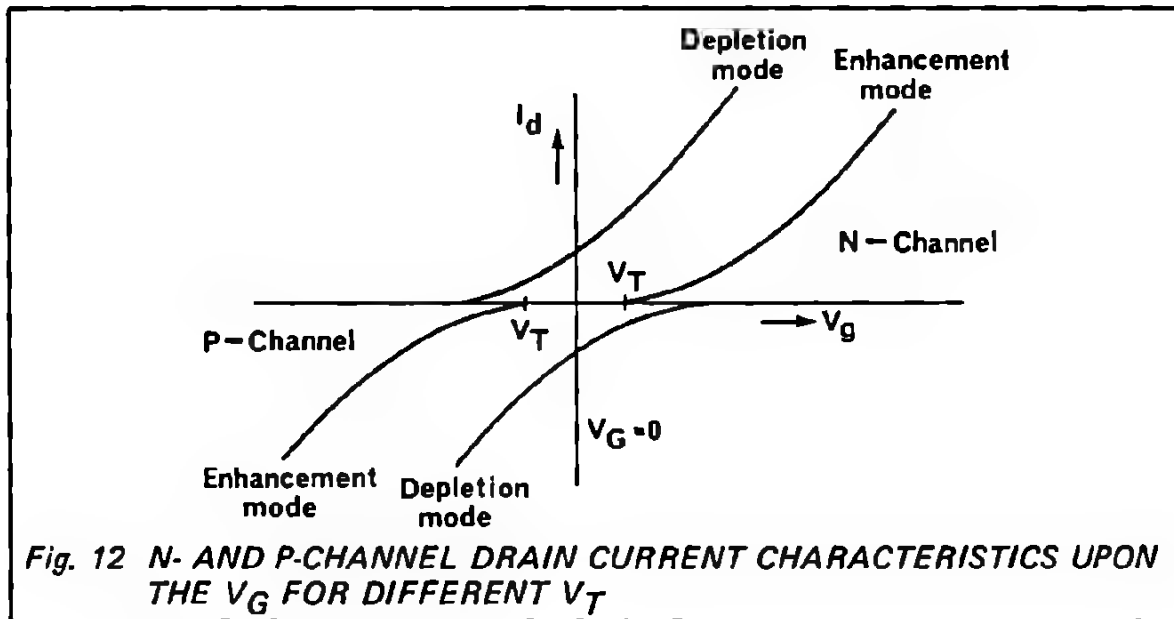
$V_D = V_{DP} = V_G - V_T$ into Eq. (25), which results in:

$$I'_D = \frac{1}{2} C_{ox} \frac{Z}{L} (V_G - V_T)^2 \quad (27)$$

where I'_D represents the current in the saturation region.

5. DEPLETION AND ENHANCEMENT MODE MOSFET TRANSISTOR

MOSFET transistors are classified as P-MOSFET or N-MOSFET according to the conduction of the channel Eq. (27) shows a square-law dependence of the drain current I_D upon the gate voltage V_G . In principle the threshold voltage V_T for P-channel and N-channel can be positive or negative. In Figure 12 are shown the drain current characteristics (P- and N-channel) with the gate voltage, V_G , for V_T both positive and negative. Considering this figure results in further classification of MOSFET transistors:



- a) Depletion mode MOSFET transistors
- b) Enhancement mode MOSFET transistors

Depletion mode devices are conducting even at $V_G = 0$. The drain current is reduced by applying a reverse voltage at the gate terminal. Enhancement mode MOSFET devices have extremely low drain-current flow for low gate voltage. Drain current conduction occurs for a V_G greater than V_T , the transfer characteristics are similar to depletion mode MOSFET transistors.

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CHAPTER 2

Technology

TECHNOLOGY



- A INTRODUCTION**
- B BASIC OPERATIONS IN
IC PROCESSING**
- C THE CMOS PROCESS**
- D RELIABILITY
PROFITABILITY
PROCESS CONTROL
PROCESS DESIGN**

A INTRODUCTION

Before looking at MOTOROLA's Complementary MOS Technology in detail, it is useful to make a general analysis of integrated circuit technology, which undergoes evolutionary and revolutionary changes each year. To all but the closely involved specialist, confusion can arise when considering the claims made for the latest breakthrough in integrated circuit process design. Too frequently, the user must be content with black box function specifications, being denied some of the information and perhaps the technique or background knowledge, required to make a critical evaluation of the technology.

Consideration of a company's other process technologies is useful, as a well planned evolution of process design and production techniques is often more successful than a revolution in the same. Revolutionary changes necessarily do occur however, and here good indications of a successful technology are, the length of time it has been established, the size of its product range, and the number of other major integrated circuit manufacturers that have adopted the same approach.

Almost invariably that which is considered beneficial by the process designer is also good for the product user, for example:

1. Simplicity of design, in terms of as few process steps as possible, means higher yields which are closely linked with higher quality and reliability. Also the fewer steps, the faster turn round time, which means faster deliveries on custom designs; the less capital investment on processing equipment necessary the more readily plant capacity may be increased, an important consideration in today's rapidly expanding market when even standard products could be in short supply.
2. The change to processing three inch diameter wafers from two inch, not only means a doubling of output for small increases in equipment and handling costs, but also leads to more confidence in quality and reliability as each wafer has become an individual small batch of IC's and each wafer continues to undergo the same thorough investment despite the size increase.

B BASIC OPERATIONS IN I.C. PROCESSING

MOS and Bipolar integrated circuits can be described in terms of the choice and arrangement of certain basic operations:

1. Thermal Oxidation:

heating silicon at typically 1000 – 1200°C, in an oxidizing atmosphere of oxygen or steam, results in the growth of thin films of silicon dioxide, which are used as diffusion masks and as gate dielectrics in MOSFET's.

2. Doping (loosely referred to as diffusion):

consists of the introduction of n- and p-type impurities into the silicon, again at high temperatures, from one of a variety of solid, liquid and gaseous sources, e.g. boron nitride, phosphorus oxychloride, arsine.

Alternatively solid phase doping may be utilized with spun on films of say boron trioxide or chemical vapor deposited (CVD) doped silica films.

Also of considerable importance today is the ion implant dopant source. Here solids or vapors are ionized in vacuum, the ions are accelerated to energies up to 300 kev, the useful ion species is selected by an electromagnetic analyser similar to those used in mass spectrometers, the ions finally impinge on the device wafers which are held in a rotating carousel. Dopant ions penetrate the silicon by several thousands of Angstroms or less if desired.

3. Epitaxy:

the growth of single crystal layers of silicon on silicon substrates or on insulating substrates such as sapphire and spinel. MOSIC's fabricated in silicon on insulating substrates (S.O.I.S.) are in late stages of development and will form a new generation of high complexity, ultra fast circuits.

4. Photolithography:

the use of photomasks and photosensitive organic films for pattern definition and etch masking.

5. Etching:

the use in general of wet chemical etchants to perform a number of functions such as:

a) the opening of windows in silicon dioxide prior to doping or contacting by metallization.

b) the definition of metal interconnect patterns.

c) the removal of silicon in certain isolation processes.

6. Deposition:

(a) Chemical Vapor Deposition (CVD) being the most common technique for the deposition of common materials such as silicon dioxide, silicon nitride, and polycrystalline silicon.

(b) Evaporation and sputtering techniques are also used, most usefully for metal rather than non-metal deposition.

7. Passivation:

Either thick or high density dielectric films are used to isolate the chip from the contamination and hostile environments. High density silicon nitride is used as a thin film below the first interconnection level, whereas relatively thicker layers of phosphorus doped silicon dioxide layers are deposited on the level above the interconnections, giving the additional benefits of mechanical protection, this being the technique employed in the fabrication of MOTOROLA CMOS chips.

8. Gettering:

Despite good process design and the use of high purity processing materials, it is still possible to produce circuits contaminated by both light and heavy metals which are manifested by their effects on threshold voltage and junction stability and leakage levels. Gettering techniques are employed in MOTOROLA's semiconductor processes to eliminate these contaminants.

Gas-Solid gettering will remove metal contaminants from the surface dielectric layers of an integrated circuit: in this technique judicious amounts of chlorine or hydrogen chloride are mixed with other gases such as oxygen, steam, and nitrogen; thermal treatment in these ambients result in complete decontamination of the surface layers.

Solid-Solid gettering is designed to remove metal contaminants from the silicon bulk; here the highly doped silicon dioxide films deposited on the wafer are used to preferentially absorb contaminants, the films subsequently removed.

9. Thermal Treatments:

A number of important heat treatments can be grouped under this heading:

a) Annealing: High temperature (900-1200°C) heat treatment in an inert ambient such as nitrogen or argon will anneal out charge in traps at the oxide silicon interface, thus allowing lower and more stable threshold voltages to be achieved.

b) Drive-In: Also carried out at high temperature, this heat treatment follows a doping step in the process, its purpose being to increase the penetration of the dopant into the silicon substrate or into an already doped region. In high speed bipolar technology, for example, the base width is extremely narrow, in the order of a few thousand Angstroms, and the emitter drive-in must be controlled precisely. In MOS technology the main reason for drive-in of junctions is to decrease the radius of curvature of the junctions, thereby elevating the breakdown voltage to an acceptable level. Drive-in of junctions can also occur incidentally as the result of a thermal oxidation process, which is used to minimize dielectric capacitance by growing a thick oxide.

c) Alloying: Being carried out at lower temperatures of 350-550°C for purpose of forming a low resistance contact between silicon and interconnection metal, alloying appears to be a simple process but, in MOS technology, the temperature, composition of the gas ambient, and the process time are all important factors in controlling surface charge levels, charge stability, and surface carrier mobility.

10. Metallization:

Interconnection of diffused regions has been achieved by a variety of metals, by far the most commonly used is aluminium. Wafers are coated by evaporating aluminium in high vacuum from a resistance heated filament or more usually from a source heated by an electron beam. The latter technique allows finer evaporation rate and thickness control.

Yet another system, the sputter source, is becoming important in view of the improvement in surface step coverage possible with a sputtered beam in which metal atoms have a short mean free path, which facilitates uniform coverage of non-ideal step profiles.

In "silicon gate" technology, highly doped polycrystalline layers are also used as an interconnection material, the commonly used technique for forming these layers is that of chemical vapor deposition.

C THE CMOS PROCESS

The MOTOROLA Complementary MOS process consists of forming the basic circuit building unit, a pair of n- and p-channel enhancement mode, insulated gate FET's utilizing metal gate electrodes.

The process steps are as follows:

1. Initial Thermal Oxidation of the substrate to produce 6000^oA SiO₂. The substrate is n-type 4-6 Ωcm <100> orientation. Surface charge on this orientation is three times less than on <111> making lower threshold voltages possible. The resistivity chosen allows optimized values of punch-through voltage, body effect and threshold voltage, referring, of course, to the p-channel devices. When transistors are connected in series, only the source of the first device is at substrate potential; on other devices in a chain the source potentials are elevated. An unfortunate effect is that the threshold voltages of these devices are increased. A simplified relationship is shown as:

$$\Delta V_T = K_B \sqrt{V_S} \text{ where } K_B = \text{body effect constant}$$

$V_S = \text{source potential.}$

The body effect constant K_B is a function of substrate resistivity ρ and gate dielectric thickness t_{ox} :

$$K_B \propto \frac{t_{ox}}{\sqrt{\rho}}$$

A typical value of K_B is 0.5.

2. The "P-tub" photolithographic operation is performed where windows are etched out of the oxide in the areas to be doped P-type prior to N⁺ source and drain diffusions.

3. The tubs are implanted with 60 ReV boron ions. This technique provides fine control of surface concentration, a prerequisite for threshold voltage and gain control, precise circuit design and high processing yield.

4. Subsequently oxidation and drive-in are performed producing p-tubes at 1000 Ω/□ sheet resistance and 10 μm depth. At this depth punch-through of N⁺ diodes to the n-type substrate is prevented and spurious n-p-n bipolar action prevented.

5. N⁺ source -drain and N⁺ stops are photoengraved. As shown, the N⁺ stops are situated between active devices being used to prevent inversion layers from forming to cause unwanted leakage. P⁺ stops are similarly used between p-channel devices.

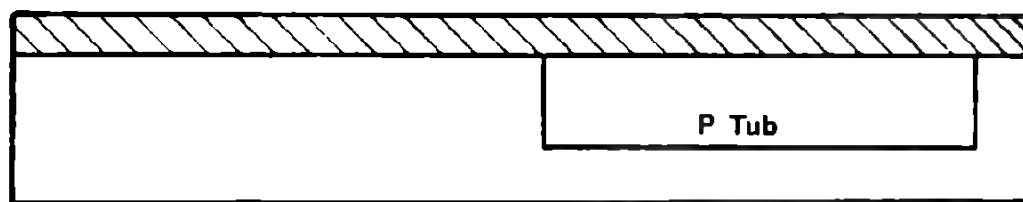
Despite a potential increase in packing density MOTOROLA standard CMOS products are designed with diffusion stops, allowing high voltage operation which is desirable for many applications.

6. A conventional phosphorus source is used to dope the N⁺ regions; oxidation and drive-in are subsequently performed resulting in less than 50 Ω/□ sheet resistance and 3 μm junction depth.

7. The P⁺ source-drain and stops are photoengraved.

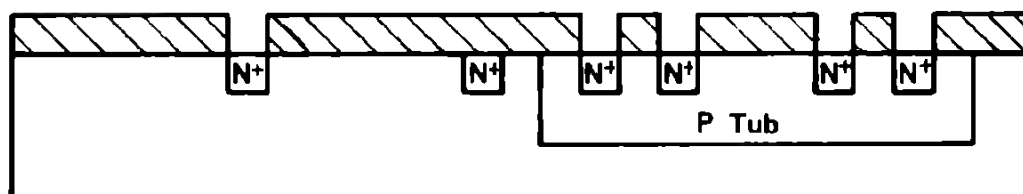
8. A conventional boron source is used for doping, here control of surface concentration within the close limits set for the P-tub is not required. After oxidation and drive-in, sheet resistance is less than 50 Ω/□ and junction depth 3 μm.

9. Photoengraving of the gate and contact hole composite pattern is carried out.
10. Gate oxidation produces 1000 \AA of SiO_2 dielectric which is annealed to minimize surface charge.
Also at this stage, gettering processes are used to eliminate all traces of metallic contamination to ensure low junction leakage and highly stable threshold voltages.
11. The contact holes are opened by standard photoengraving techniques.
12. Aluminium evaporating from an electron-beam source ensures uniform coverage of the shallow contoured oxide steps.
13. Photoengraving of the interconnection pattern is followed by alloying and deposition of 1 μm of phosphorus doped silicon dioxide passivation. This crack free film is formed by the reaction of silane (SiH_4), phosphine (PH_3) and oxygen on the heated wafer surface. The passivation film prevents ingress of contaminants and provides protection against mechanical damage during the final stages of assembly.
14. A final photoengravure process exposes the aluminium bonds pads in readiness for probing and assembly and testing.

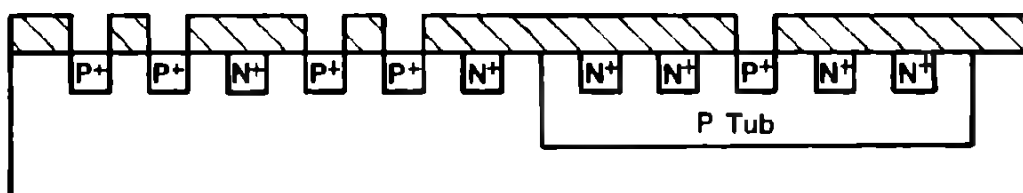


1. P-TUB DIFFUSION

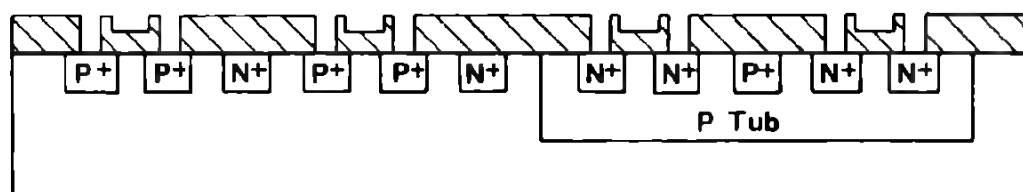
SiO₂
N substrate



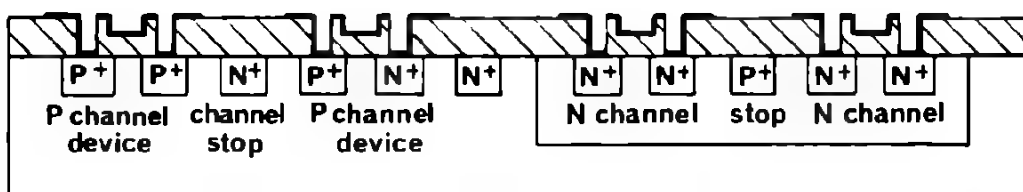
2. N⁺SOURCE-DRAIN CHANNEL STOP



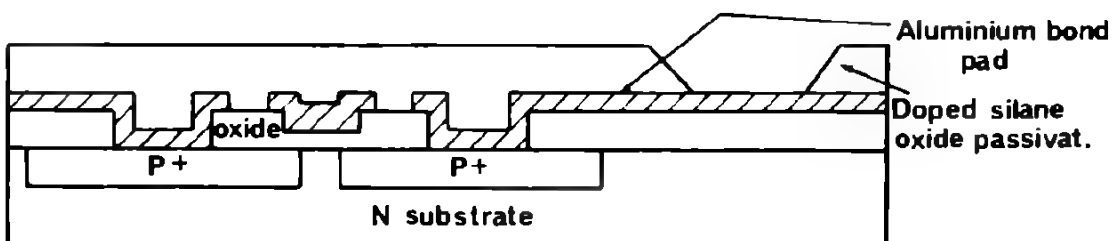
3. N⁺P⁺SOURCE-DRAIN AND CHANNEL STOPS



4. GATE OXIDATION COMPLETED



5. ALUMINIUM INTERCONNECTIONS PHOTO ENGRAVED



6. FINAL DEVICE STRUCTURE P-CHANNEL EXAMPLE

CMOS-WAFER PROCESSING

3) RELIABILITY; PROFITABILITY; PROCESS CONTROL; PROCESS DESIGN

As the complexity of integrated circuits increases, it is not obvious that the best manufacturing methods necessary to provide inherently highly reliable circuits, are also those methods which ensure high profitability to the manufacturer. As a result of many years of experience in manufacturing across the whole range of MOS and bipolar integrated circuits, MOTOROLA's policy is to invest in a high level of process control and in-process quality assurance, in addition to the high degree of quality assurance already ensured in the final stages of assembly and testing.

Because of the intense competition between suppliers of raw materials and piece parts to the microelectronics industry, the highest quality can be bought for a small premium; to buy the cheapest is certainly an outmoded technique for increasing profitability. Today and tomorrow the real solution to increased or even maintained profitability is to manufacture integrated circuits in high yield. There is a close link between high yield and high inherent reliability.

During manufacture, final testing and screening, defective circuits are rejected by virtue of a typical and mal-functional electrical behavior, and for detected visual effects. Despite designed-in tolerance to spreads in parametric values there are outer limits to be observed; the closer control within such limits, the higher the manufacturing yield and reliability; here failure due to gradual drift in operating characteristics is being considered, rather than the occurrence of catastrophic failure.

In the case of catastrophic failure, examination of failure modes shows the incidence of the incipient defects involved to be closely related to the incidence of gross defects. In the elimination of gross defects as a necessity for increased manufacturing yield, there is therefore an additional pay-off to user and manufacturer, that of improved reliability.

RAW MATERIALS PHOTOMASKS e.g.

Raw Silicon — involve a wide range of evaluation at incoming inspection

Note: The major supplier of silicon and photomasks is MOTOROLA.

INITIAL OXIDATION

1. Embraced by a basic furnace operating specification (F.O.S.)
Gas Purity (Chemical and Physical)
Gas Flow Rate
Uniformity and Stability of furnace temperature
Routine examination for ingress of contaminants, such as sodium
2. Oxide thickness
Uniformity of thickness, wafer to wafer, batch to batch.

<u>P-TUB PHOTOMASKING</u>	<ol style="list-style-type: none"> Embraced by a basic photo-masking operations specification (P.O.S.) <ol style="list-style-type: none"> Photoresist quality: <ul style="list-style-type: none"> viscosity solids content sensitivity particle density absorption spectrum Spin on speed and acceleration Thickness variations Alignment fixture: lamp intensity and uniformity Control of baking temperatures Control of pattern development equipment Assessment of acuity of pattern print-out Quantative assessment of pin-hole density Adhesion characteristics during etching Assessment of gross defects before and after etching Completeness of etching. This list is not exhaustive! Specific to this process step <ol style="list-style-type: none"> Dimensional control Alignment of pattern with respect to wafer reference flat.
<u>P-TUB DOPING BY ION INPLANT</u>	<ol style="list-style-type: none"> Ion Implanter Operating Spec. Sheet resistance value and uniformity.
<u>P-TUB OXIDATION</u>	<ol style="list-style-type: none"> F.O.S. Oxide thickness Sheet resistance Junction depth
<u>P-TUB DRIVE-IN</u>	<ol style="list-style-type: none"> F.O.S. Sheet resistance Junction depth
<u>N⁺ PHOTOMASKING</u>	<ol style="list-style-type: none"> P.O.S. Dimensional control Alignment with respect to P-Tub
<u>N⁺ DOPING</u>	<ol style="list-style-type: none"> F.O.S. Glass thickness Sheet resistance

N ⁺ DRIVE-IN	<ul style="list-style-type: none"> 2. Oxide thickness 3. Sheet resistance 4. Junction depth
P ⁺ PHOTOMASKING	<ul style="list-style-type: none"> 1. F.O.S. 2. Sheet resistance 3. Junction depth 1. P.O.S. 2. Dimensional control 3. Alignment with respect to the two previous patterns
P ⁺ DOPING OXIDATION DRIVE-IN	As for N ⁺
GATE PHOTOMASKING	<ul style="list-style-type: none"> 1. P.O.S. 2. Dimensional control 3. Critical alignment for gate overlap of N⁺ and P⁺ source and drain
GATE OXIDATION ANNEAL AND GETTERING	<ul style="list-style-type: none"> 1. F.O.S. 2. Oxide thickness 3. Evaluation of surface charge level and stability
CONTACT HOLE PHOTOMASKING	<ul style="list-style-type: none"> 1. P.O.S. 2. Dimensional control 3. Alignment 4. Completeness of etching is critical
ALUMINIZATION	<ul style="list-style-type: none"> 1. Vacuum system operating spec. 2. Electron Beam source operation 3. Aluminium Thickness and Uniformity 4. Stability of the Aluminium oxide system 5. Etchability 6. Step coverage
INTERCONNECTION PHOTOMASKING	<ul style="list-style-type: none"> 1. P.O.S. 2. Dimensional control 3. Alignment critical: gate coverage and track width important
PASSIVATION	<ul style="list-style-type: none"> 1. Deposition System Operation Spec. 2. Oxide thickness 3. Doping concentration 4. Cracking and film perfection
PASSIVATION PHOTOMASKING	<ul style="list-style-type: none"> 1. P.O.S. 2. Alignment 3. Condition of bond pads after etching.

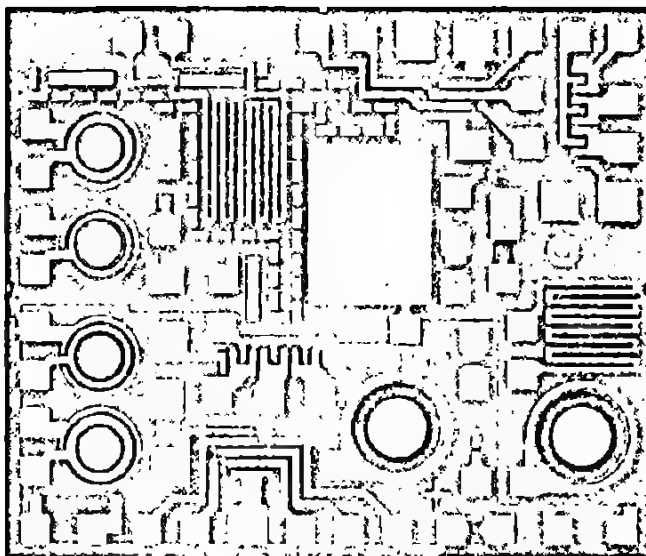
In addition to the process evaluations just described, there are also assessments of oxide perfection, carried out as a means of monitoring furnace status: sophisticated techniques allow pinhole and flow densities to be examined on a routine basis, together with measurements of gate rupture voltage. Typically CMOS gates would rupture at 100 volts, i.e. considerably above rated operating voltages; high voltage transients however, associated with static discharge, make it necessary to protect gates with special devices built in to each chip, the design and operating characteristics of these protection devices are described in a later chapter.

To allow routine monitoring of basic factors and operating characteristics, every CMOS wafer contains standard process control chips. This standard design comprises n-channel MOST's, p-channel MOST's, capacitors, resistors and diodes allowing assessment of threshold and breakdown voltages, contact resistances, hole and electron mobility, surface charge density, surface doping levels, gate oxide thickness, and sheet resistance of doped regions. Also the reliability and stability of the IC's on a wafer can be predicted using thermal and electrical stress tests on these test structures.

An aspect of process design which is all important in the attack on defect levels is that of wafer handling techniques. Traditionally, semiconductor device manufacturers have used manual techniques for handling wafers into and out of furnace boats, inspection stations, alignment stations, evaporators, passivators, etc.. Despite modern designs of tweezers and vacuum pick-ups, build-up of defects occurs if process operators move wafers.

By using modern wafer handling equipment which utilizes blown air tracks to float and transport wafers, and by using new designs of wafer cleaning jigs and furnace boats which allow mass transfer of wafers, then the handling by operators can be cut down to 5% of that necessary in more traditional manufacturing facilities.

Reduction of major and minor defects increases yield and reliability. The welcome benefits of advanced technology are being felt in CMOS wafer processing facilities and by the users of CMOS microcircuits.



THE CMOS STANDARD PROCESS CONTROL CHIP

CHAPTER 3

General CMOS
characteristics

GENERAL CMOS CHARACTERISTICS

A BASIC CIRCUIT CONFIGURATIONS

B MAIN CMOS ELECTRICAL CHARACTERISTICS

C VOLTAGE AND ENERGY NOISE IMMUNITY OF CMOS INTEGRATED CIRCUITS

D INPUT PROTECTION CIRCUITS

E REFERENCES

1. CMOS INVERTER
2. NOR AND NAND GATES
3. TRANSMISSION GATE

1. POWER SUPPLY VOLTAGE AND TEMPERATURE RANGE
2. SWITCHING CHARACTERISTICS
3. POWER DISSIPATION CHARACTERISTICS
4. CLOCK-WAVEFORM SPECIFICATION

1. GENERAL
2. D-C NOISE IMMUNITY
3. A-C NOISE IMMUNITY
4. ENERGY NOISE IMMUNITY

A BASIC CIRCUIT CONFIGURATIONS

1. CMOS INVERTER

The basic building block of the CMOS logic circuits is the complementary pair MOS inverter. It consists of the p- and n-channel device connected as shown in Figure 1. In order to describe the function of this CMOS inverter circuit, it is very convenient to introduce equations describing the channel characteristics of the p- and n-channel MOS devices.

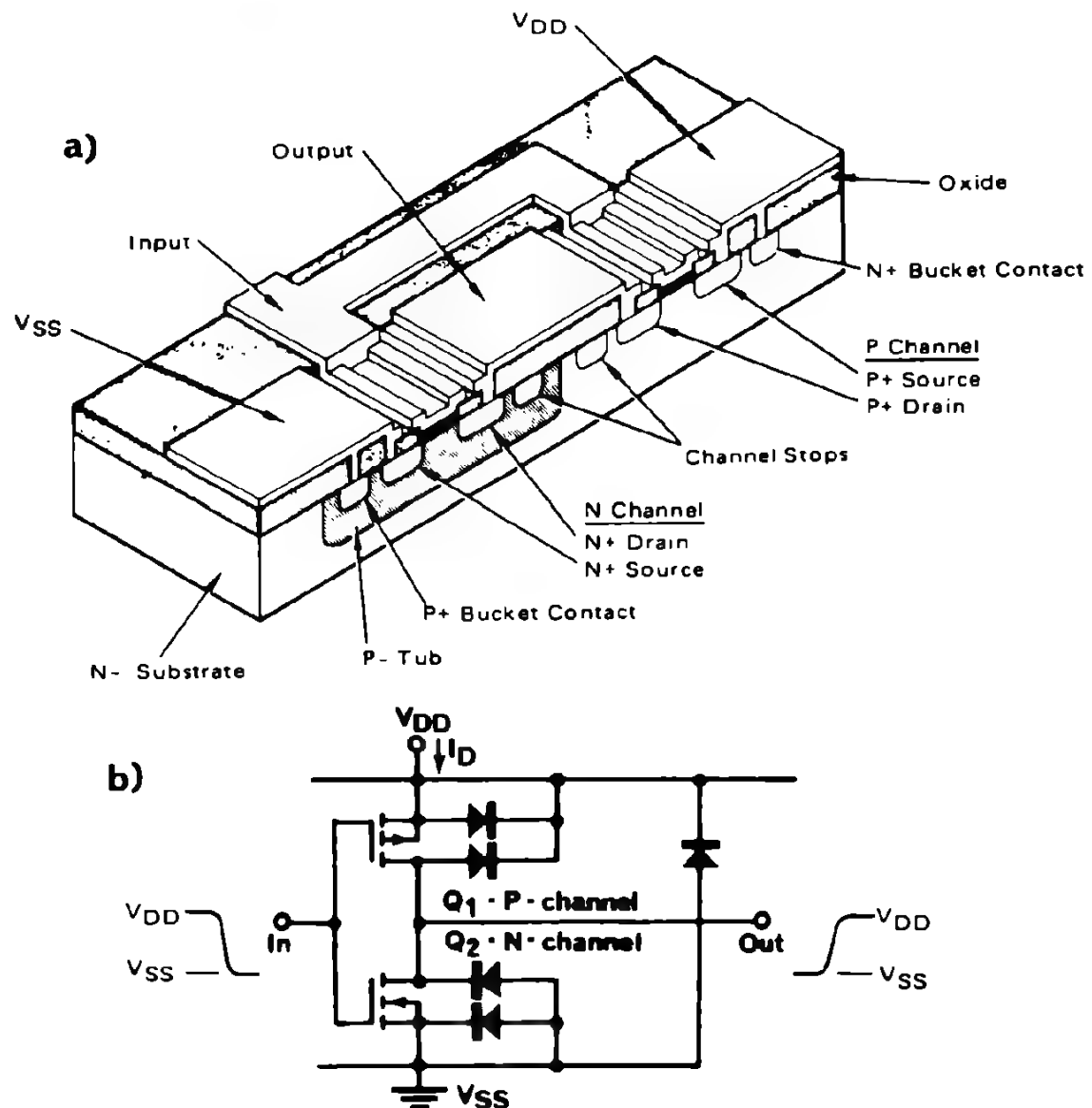
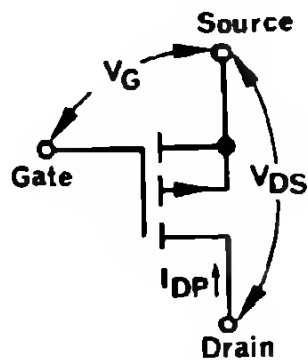
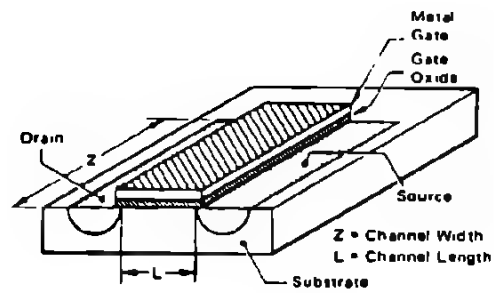


Fig. 1 THE BASIC CMOS P-CHANNEL AND N-CHANNEL DEVICES CONNECTED TO FORM AN INVERTER

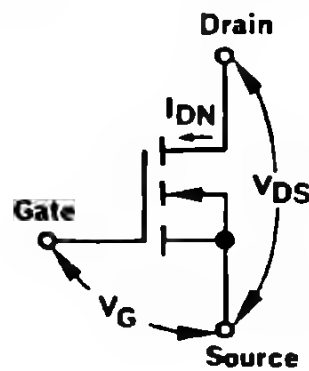


P-CHANNEL DEVICE

Substrate: N-Type Silicon
 Drain/Source: P-Type Diffusion

N-CHANNEL DEVICE

Substrate: P-Type Silicon
 Drain/Source: N-Type Diffusion



**Fig. 2 EXPLANATION
OF SYMBOLS**

In Figure 3 the source-to-drain characteristics are shown as a function of source to-drain voltage in an enhancement type MOS transistor as described by the equations. If p-channel and n-channel MOS devices are connected as shown in Figure 1b, the equations describing the drain-current characteristics of both p- and n-channel devices transform to the following expressions:

N-channel device non-saturation region:

$$I_{DN} = K_N \left[V_{out} (V_{in} - V_{TN}) - \frac{V_{out}^2}{2} \right] \quad \text{where:} \quad \begin{array}{l} V_{out} \leq V_{in} - V_{TN} \\ V_{in} > V_{TN} \end{array} \quad \mathbf{1}$$

For the saturated region:

$$I'_{DN} = \frac{K_N}{2} (V_{in} - V_{TN})^2 \quad \text{where:} \quad \begin{array}{l} V_{out} \geq V_{in} - V_{TN} \\ V_{in} > V_{TN} \end{array} \quad \mathbf{2}$$

For the p-channel device in the non-saturated region:

$$I_{DP} = -K_P \left[(V_{out} - V_{DD}) (V_{in} - V_{DD} - V_{TP}) - \frac{(V_{out} - V_{DD})^2}{2} \right] \quad \text{where:} \quad \begin{array}{l} V_{out} \geq V_{in} + |V_{TP}| \\ V_{in} \leq V_{DD} - |V_{TP}| \end{array} \quad \mathbf{3}$$

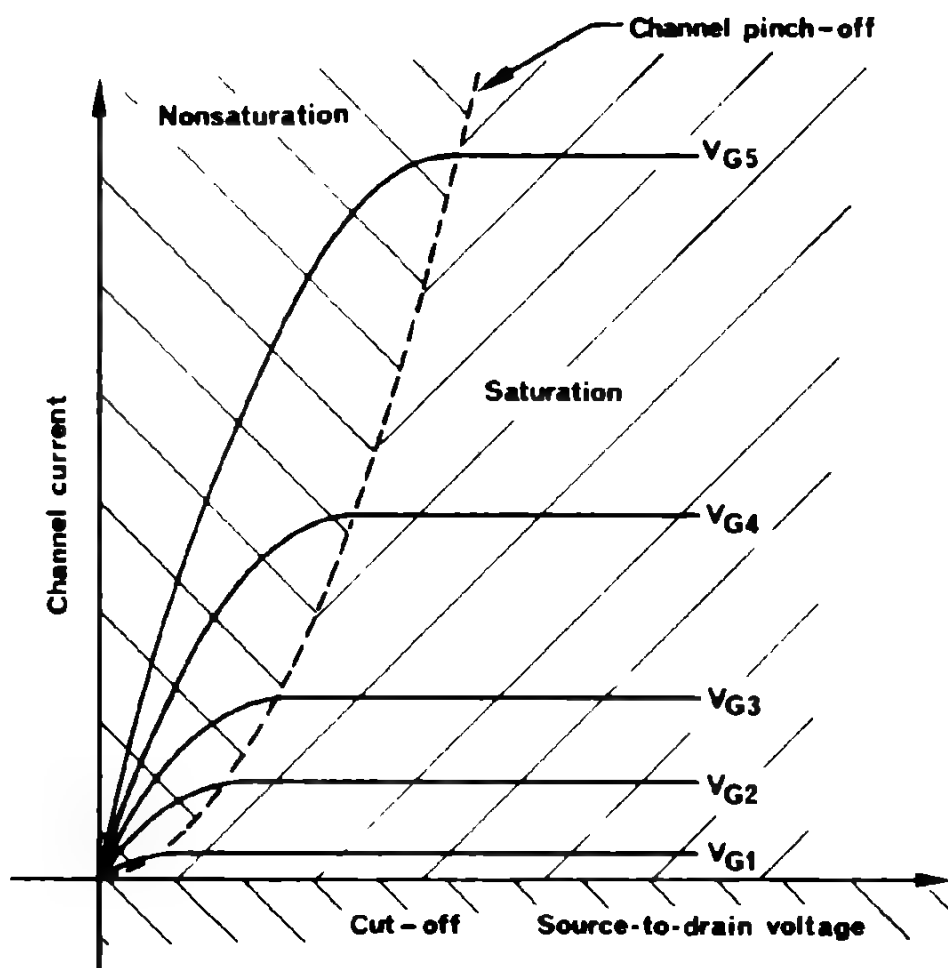


Fig. 3 DRAIN CHARACTERISTIC CURVES

For the saturation region:

$$I_{DP} = -\frac{K_p}{2} (V_{in} - V_{DD} - V_{TP})^2$$

where:

$$V_{out} \leq V_{in} + |V_{TP}|$$

$$V_{in} \leq V_{DD} + |V_{TP}|$$

4

In Figure 1a, the cross section of the CMOS inverter circuit on the chip is shown. Figure 1b illustrates schematic diagrams of this circuit. The processing of source-drain and p-well diffusions also creates parasitic diodes, which are connected to the basic inverter. These parasitic elements are reverse biased across the power supply and they are the major source of power dissipation in the quiescent state.

In the following, the operation of the complementary pair MOS inverter will be described in detail. Figure 4 gives the voltage transfer characteristic (or the V_{in} versus V_{out} transfer curve) for the basic inverter, at the power supply voltage of 10V. These characteristics can be divided into the five regions in which the functions of the transistor Q_1 and Q_2 are summarized by the following table.

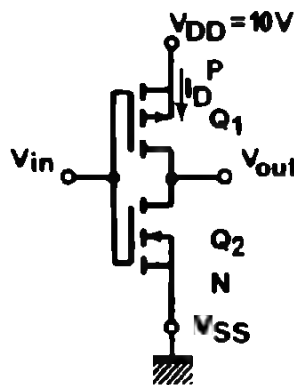
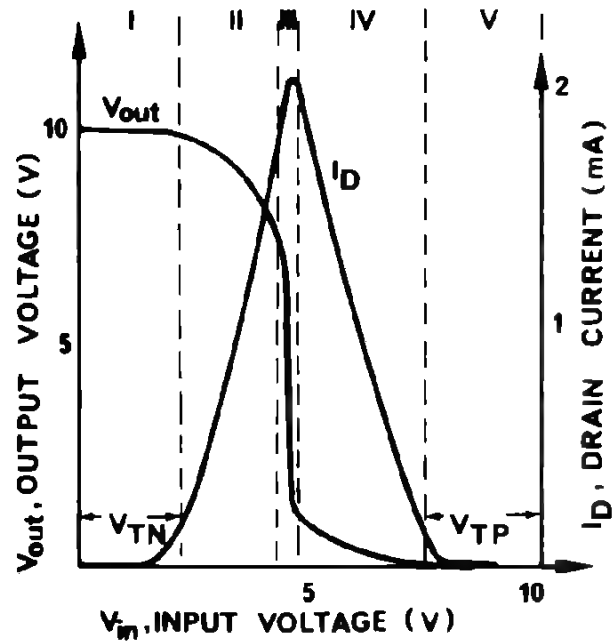


Fig. 4
VOLTAGE AND CURRENT
TRANSFER CHARACTERIS-
TICS OF AN INVERTER



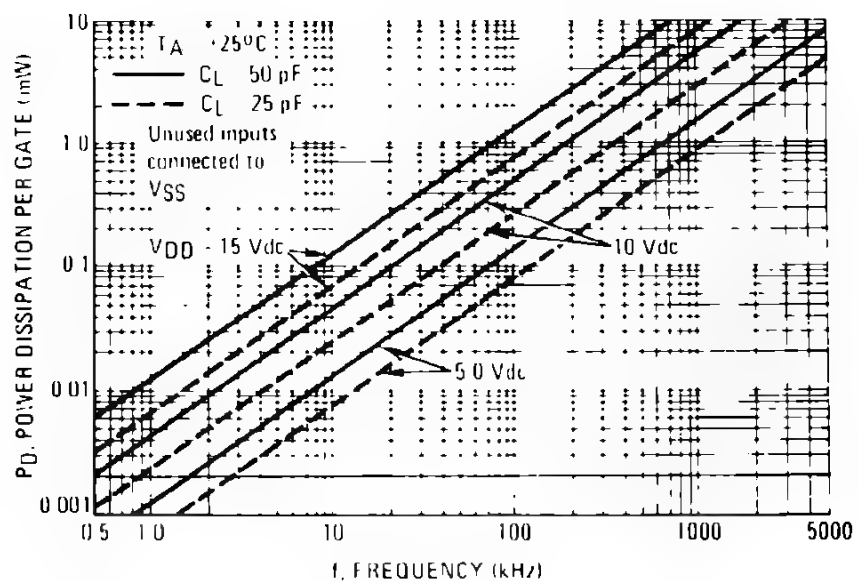
V_{in}	Region	Q_1	Q_2
$0 \leq V_{in} \leq V_{TN}$	I	Non-saturated	Cut-off
$V_{out} - V_{TP} \geq V_{in} \geq V_{TN}$	II	Non-saturated	Saturated
$V_{out} - V_{TP} \leq V_{in} \leq V_{out} + V_{TN}$	III	Saturated	Saturated
$V_{out} + V_{TN} \leq V_{in} \leq V_{DD} - V_{TP} $	IV	Saturated	Non-saturated
$V_{DD} - V_{TP} \leq V_{in} \leq V_{DD}$	V	Cut-off	Non-saturated

If V_{in} is smaller than threshold voltage V_{TN} of the transistor Q_2 , which is n-type, the transistor is cut-off. The p-type transistor Q_1 is non-saturated and is biased on by approximately V_{DD} volts. The output is now $+V_{DD}$, since the n-type transistor shows extremely high resistance relative to the p-transistor. This is region I. With increasing V_{in} one enters into region II. Here the transistor Q_2 is saturated, $V_{TN} \leq V_{in}$, and the transistor Q_1 is still non-saturated, $V_{out} - |V_{TP}| \geq V_{in}$.

Only in region III are both transistors saturated and act as a perfect current source. This is the transfer high-gain region. In region IV, transistor Q_2 is non-saturated because $V_{out} + V_{TN} \leq V_{in}$ and transistor Q_1 is saturated because $V_{in} \leq V_{DD} - |V_{TP}|$. In region V, the transistor Q_1 is at cut-off $V_{in} \geq V_{DD} - |V_{TP}|$ and transistor Q_2 is non-saturated.

In regions I, II and III, the inverter appears from the output as a low resistance to V_{DD} ($500\Omega - 1\text{ K}\Omega$); and in regions I, II as a high resistance to the ground. In region III, the inverter shows a low resistance between the output and V_{DD} and also between the output and ground. In regions II, III, and IV (both transistors either saturated or non-saturated) current flows from V_{DD} to ground; figure 4 illustrates this current I_D as a function of V_{in} , together with voltage transfer characteristics. The current transfer characteristic is a measure of the dependence on the input voltage of the current flowing between the V_{DD} and V_{SS} . In a situation involving the application of a switching waveform to V_{in} (rise and fall times in the range of 20 – 200 ns) the current I_D does not flow through both Q_1 and Q_2 . The reason for this may be explained as follows: Assume Q_1 is "OFF" (Region V) and Q_2 is "ON". As V_{in} switches from V_{DD} to ground, there is a period of time when both Q_1 and Q_2 are "ON" (Region I, III and IV). However, because of stray and load capacitance at the output, the output voltage is still nearly 0V, when Q_1 and Q_2 are both "ON". Thus, little current flows through Q_2 to ground. Because of this fact, the power dissipation of CMOS circuits, under switching conditions, is due almost entirely to capacitive loading.

Fig. 5
POWER
DISSIPATION OF
CMOS INVERTER



he dynamic power dissipation result
 nction of the frequency at which t
 igure 5 shows the effect of capacitive
 higher operating speeds are possible
 lower dissipation.

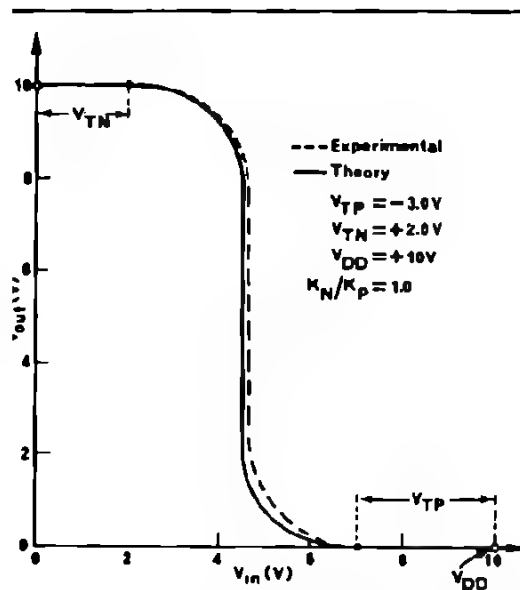
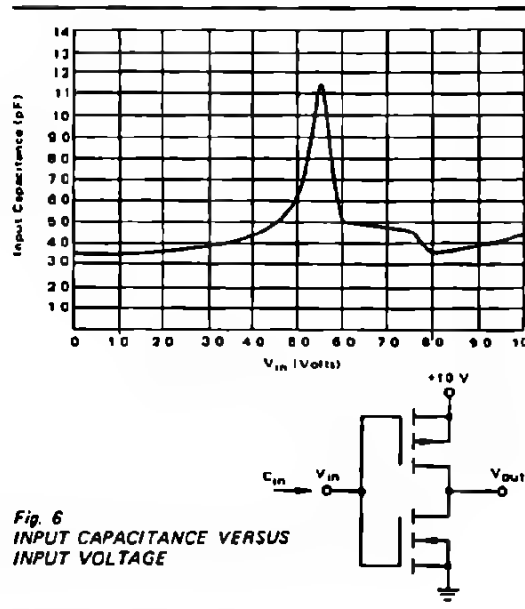


Fig. 7 COMPLEMENTARY INVERTER TRANSFER
 CHARACTERISTICS

one must compromise between noise immunity and switching speed.

Figure 7 illustrates the calculated and measured voltage transfer characteristics for a CMOS inverter with K_N/K_P ratio approximately unity, assuming threshold voltages of $V_{TN}=+2V$, $V_{TP}=-3V$ and $V_{DD}=10V$.

In order to be able to calculate V_{out} as function of V_{in} , the equations for regions II, III and IV are expressed as:

$$\begin{aligned} \text{Regions II : } V_{out} &= V_{in} - V_{TP} + \left[(V_{DD} - V_{TP} - V_{in})^2 - \frac{K_N}{K_P} (V_{in} - V_{TN})^2 \right]^{1/2} \\ \text{III : } V_{in} &= V_{in}^* \text{ for } V_{in}^* - V_{TN} \leq V_o \leq V_{in}^* - V_{TP} \\ \text{IV : } V_{out} &= V_{in} - V_{TN} - \left[(V_{in} - V_{TN})^2 - \frac{K_P}{K_N} (V_{in} - V_{DD} - V_{TP})^2 \right]^{1/2} \end{aligned}$$

It appears that the transfer characteristic of a CMOS inverter is characterized with well defined "1" and "0" levels and a narrow high gain region. This characteristic approaches those for an ideal switch. The function of the CMOS inverter can be simulated with two voltage dependent resistors R_P and R_N connected in series as shown in Figure 8.

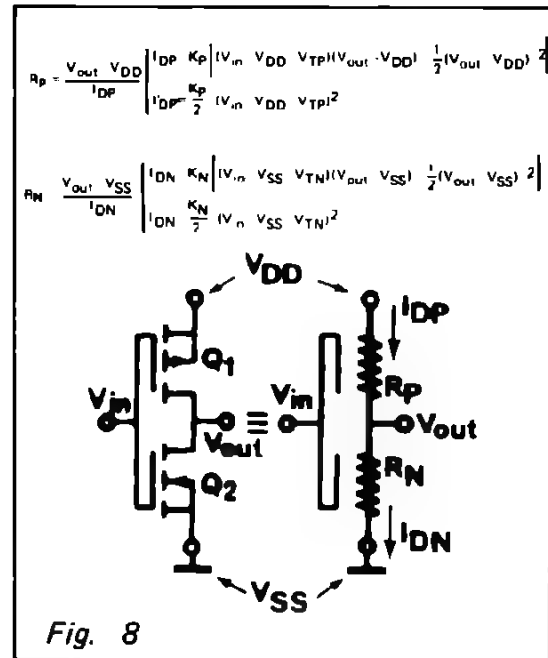


Fig. 8

The effect of series and shunt transistors on the DC transfer characteristic of the circuit is to change the constants K_N and K_P . If the transistors are in parallel, with the same voltage at the inputs, the current is increased by a factor of n , ($K_{eff} = nK$). For transistors in series, the total current is scaled down by a factor of n ($K_{eff} = \frac{K}{n}$). Using equation (2) and (4), for I'_{DN} and I'_{DP} the following transfer voltage relations are obtained ($V_{in}^* = \text{transfer voltage}$):

$$K_N (V_{in}^* - V_{TN})^2 = K_P (V_{in}^* - V_{DD} - V_{TP})^2.$$

Defining:

$$\frac{K_P}{K_N} = \beta$$

The β of the NOR and NAND circuits depends on the number of inputs. For the NOR gate the worst case occurs when only one input is high so that

$$\beta_{\text{eff}} = \frac{K_P}{\frac{n}{K_N}} = \frac{\beta}{n}$$

This means that resistance of each n-channel should be equal to the resistance of all p-channels in series

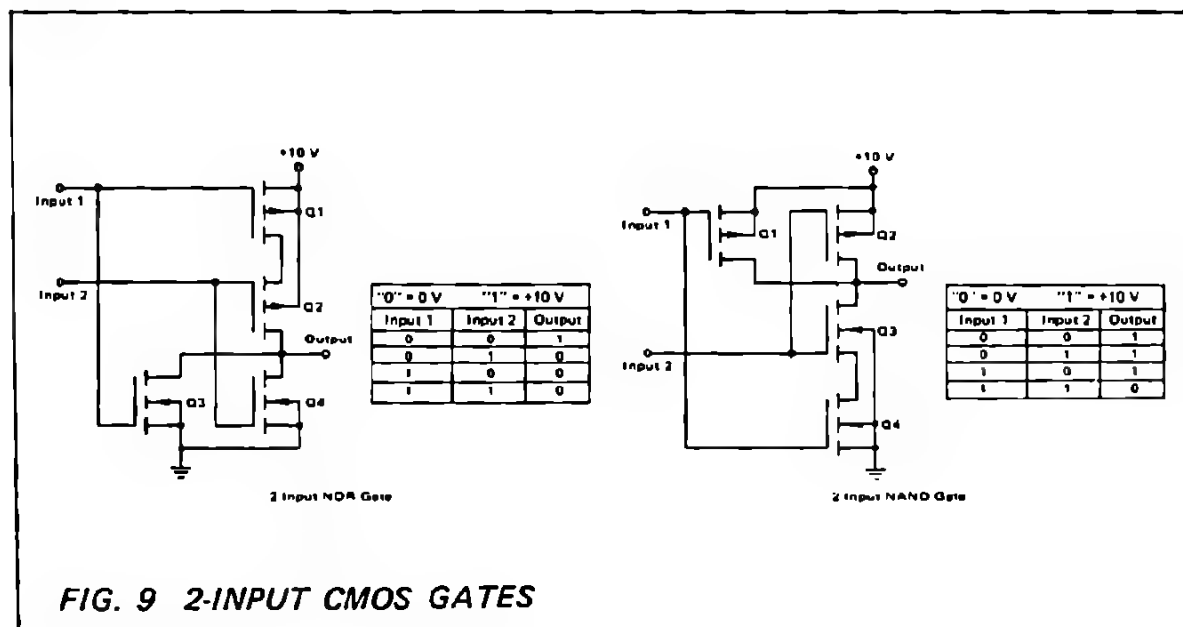
For the NAND gate the resistance of the p-channel should be equal to the series resistance formed by the n-channel transistors.

Calculations show that the practical number of inputs for NAND and NOR gates is limited to 4, in order to keep the transfer characteristic within the limits demanded by the CMOS family noise immunity requirements.

2. NOR AND NAND GATES

Figure 9 shows how the inverter is connected to form the NAND and NOR logic functions (3). Considering the NOR function, gates of Q_1 and Q_3 are tied together to form the input 1 of the basic inverter. The gates of Q_2 and Q_4 form input 2. Device Q_2 acts as a series resistance which is either extremely high or low, depending upon its gate signal in the inverter formed by Q_1 and Q_3 . Likewise Q_4 acts as a series resistance in the second inverter. The output of the circuit is at +10V only when both Q_1 and Q_2 are "ON". This occurs only if both inputs 1 and 2 are at ground. Thus, the output is a logic "1" only when both inputs are logic "0" which is the NOR function.

The CMOS NOR gate can be converted to a NAND gate by interchanging the p- and n-channel devices, and turning the circuit upside down. It can be seen that Q_3 and Q_4 must be "ON" for the output to be in the logic "0" condition. More inputs can be added to make 3- and 4-input gates by adding complementary pairs.



V_{in} , INPUT VOLTAGE (Vdc)

FIG. 10 VOLTAGE TRANSFER CHARACTERISTICS VERSUS TEMPERATURE

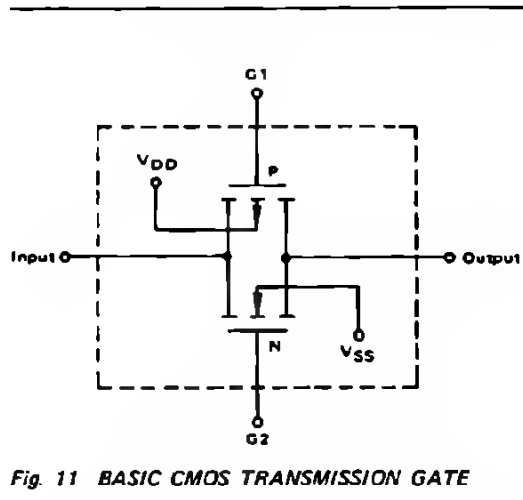


Fig. 11 BASIC CMOS TRANSMISSION GATE

te (G1) of the p-channel device is at
vice is at V_{DD} . When G2 is at V_{SS}
"OFF" and a resistance greater than

ut of a basic transmission gate in the
tage applied at the input, the poten-
($V_{DD}-V_{SS}$), and the load on the
put resistance with a 10 k Ω load

effect which occurs in the R_{ON}
gate shown in Figure 11. When V_{in}
providing the low resistance. The n-

channel device is "OFF" since the potential difference between G2 and the drain or source of the n-channel device is less than the threshold voltage. When V_{in} is at or near V_{SS} , the n-channel device is conducting and the p-channel device is "OFF". At voltages between the two extremes, both devices are partially "ON" and the value of R_{ON} is due to the parallel resistance of the p- and n-channel devices. The different slope of the curve on either side of the peak is due to the greater sensitivity of the n-channel resistance to substrate degeneration (or substrate bias) than the p-channel. Thus, the rate of increase in R_{ON} with respect to V_{in} is greater for input voltages between V_{SS} and the "peaking voltage" than for input voltages greater than the "peaking voltage".

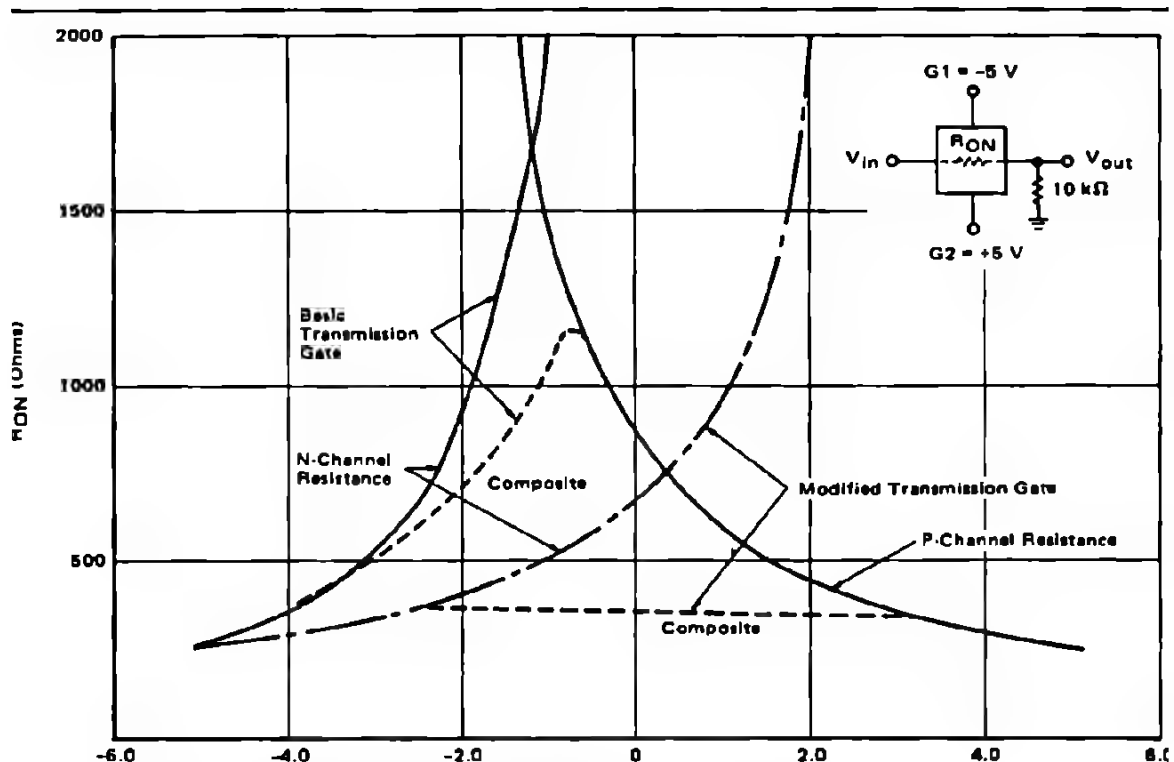


Fig. 12 TYPICAL R_{ON} RESISTANCE VERSUS V_{in} OF CMOS TRANSMISSION GATE

Figure 13 shows a modification to the basic transmission gate: the addition of a third device to control the substrate bias of the n-channel device. The effect of this third device is to delay the turn "OFF" of the n-channel device, which results in a much flatter R_{ON} versus V_{in} curve, as shown in Figure 12. This concept is used in the MC 14016 Quad Analog Switch.

All integrated CMOS logical circuits are composed of two basic blocks: inverter and transmission gate.

The transmission gate when combined with basic inverter circuits, Figure 14 forms a CMOS bilateral switch.

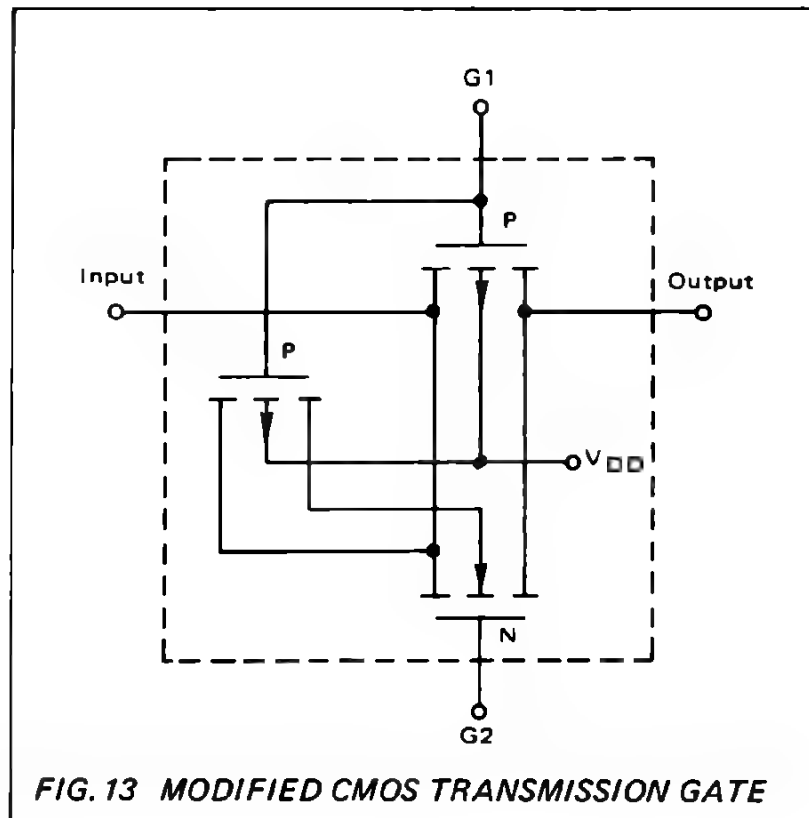
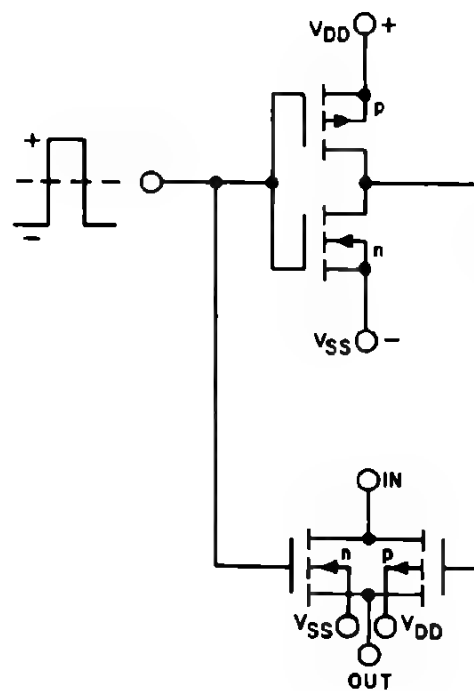


FIG. 14
BASIC CONFIGURATION
OF CMOS BILATERAL
SWITCH



B MAIN CMOS ELECTRICAL CHARACTERISTICS

CMOS devices are completely specified in the appropriate data sheets. A complete knowledge of any logic family generally involves a thorough review of available standard product data sheets. However, only a few CMOS characteristics are of major importance to the logic system designer. The following characteristics are discussed hereunder: power supply and temperature range, switching characteristics, dissipation characteristics, clock-waveform specification. The noise immunity specifications, because of their complexity, will be treated in a separate part of this chapter (section C).

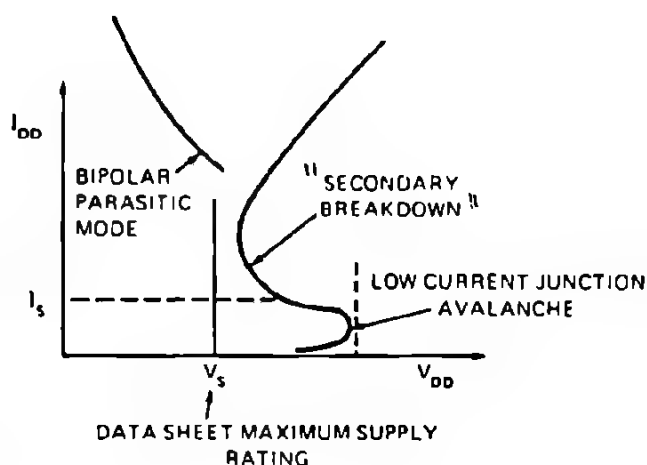
1. POWER SUPPLY VOLTAGE AND TEMPERATURE RANGE

MOTOROLA CMOS devices are available in three series, "AL", "CL", and "CP" which differ primarily in their operating temperature range and power supply voltages [4].

"AL" devices are in hermetic ceramic packages and will operate over the full -55°C to $+125^{\circ}\text{C}$ temperature range with 3 to 18V power supply limits.

The more limited "CL" (in ceramic package) and "CP" (in plastic package) series operate between -40°C and 85°C over 3-16V range. The maximum operating supply voltage ($V_{DD} - V_{SS}$) is limited due to the "breakdown effects" (see Figure 15). In MOS transistors there are drain breakdowns and gate breakdowns. (For details see [2]). The low current junction avalanche appears at 25-35 volts.

Fig. 15
"SECONDARY BREAKDOWN"
of CMOS devices can be sustained at voltages which are substantially lower than the low-current avalanche level.



from this point of view a maximum operating voltage of 18V seems to be conservative. Sustaining currents, I_S , at the "second breakdown", generally vary only from 10 to 50 mA, but such a current jump could be deadly to the device. Once in this breakdown mode, in which the power supply voltage is above V_S , any on-chip current transient having a value greater than the sustaining current can forward bias the parasitic bipolar devices which are present on all CMOS devices. (V_S — the voltage at which the current gradually begins to increase).

The resulting high currents can produce a short circuit of the power supply. CMOS devices, of course, are tested for this condition and, according to the test, the maximum operating voltage is specified ("AL" or "CL/CP" series). The minimum recommended supply voltage of 3V is based on the maximum allowed individual device threshold voltage levels for either p- or n-channel transistors. At this minimum value of 3V, the CMOS device performs satisfactorily in all digital logic applications.

2. SWITCHING CHARACTERISTICS

A typical DC voltage-transfer characteristic (DC switching characteristics) of a CMOS device (MC 14001 AL) is shown in Figure 16 for V_{DD} equal to 5, 10 and 15 volts. The calculated statistical values from measurements on 50 devices, the arithmetic mean and the spread of $\pm 3\sigma$ are shown here. The high noise immunity and the symmetry of this switching characteristic is evident. The voltage transfer characteristics of a CMOS device approaches the characteristics of an ideal switch; this is illustrated in Figure 17.

The spread of characteristics shown in the following figures is only an indication and no guarantee can be furnished.

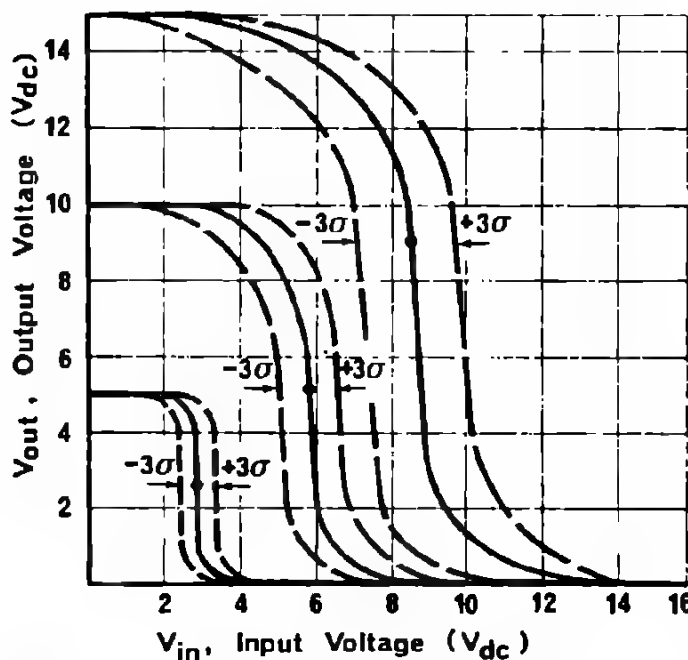


Fig. 16
TYPICAL VOLTAGE
TRANSFER
CHARACTERISTICS
(calculated statistical values)
MC 14001 AL, 50 devices
 $T=25^{\circ}\text{C}$, one input activated

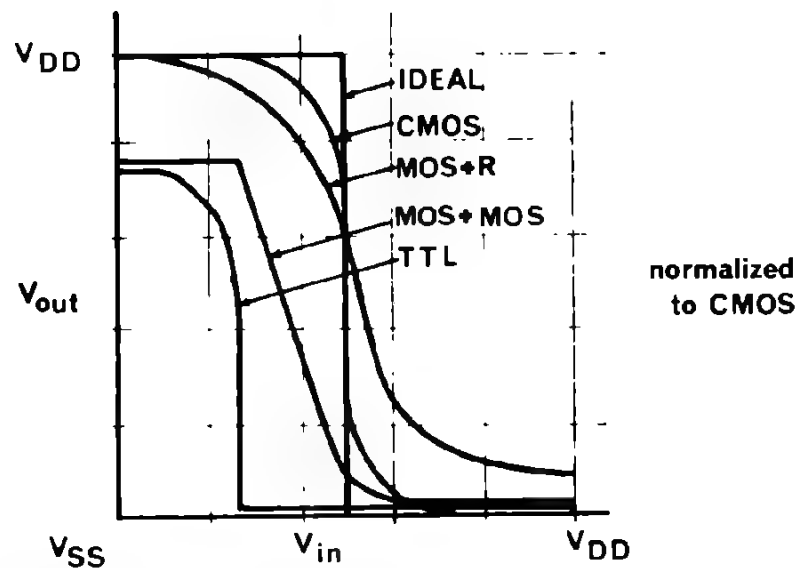


Fig. 17
VOLTAGE TRANSFER CHARACTERISTICS – A COMPARISON BETWEEN SOME LOGIC FAMILIES AND CMOS

When a CMOS device switches, it goes through a transition region. (Region III, Fig. 4). Here, both transistors are "ON" simultaneously and there is a current flow between V_{DD} and V_{SS} . In Figure 18 the current transfer characteristics for NAND gate MC 14011 AL are shown.

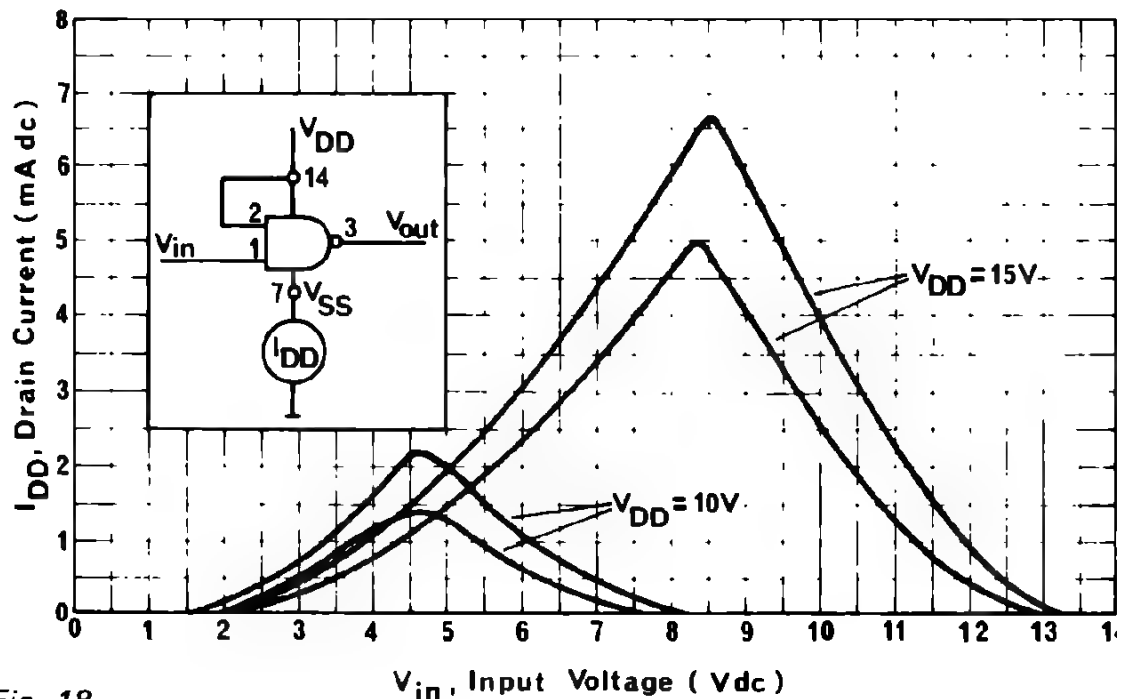
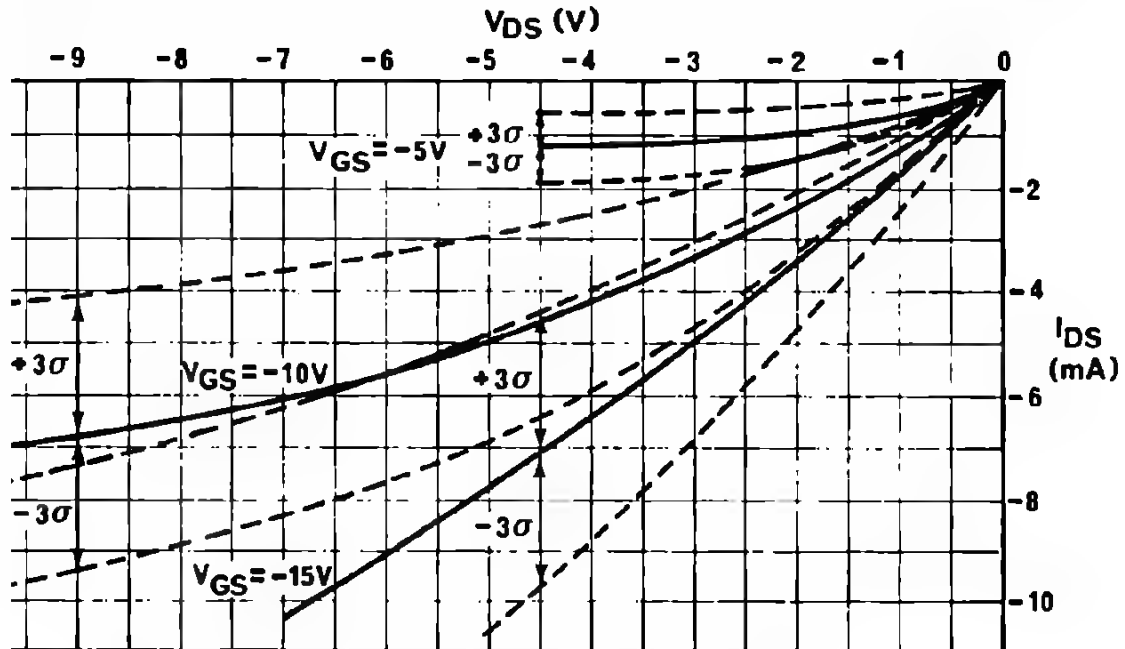
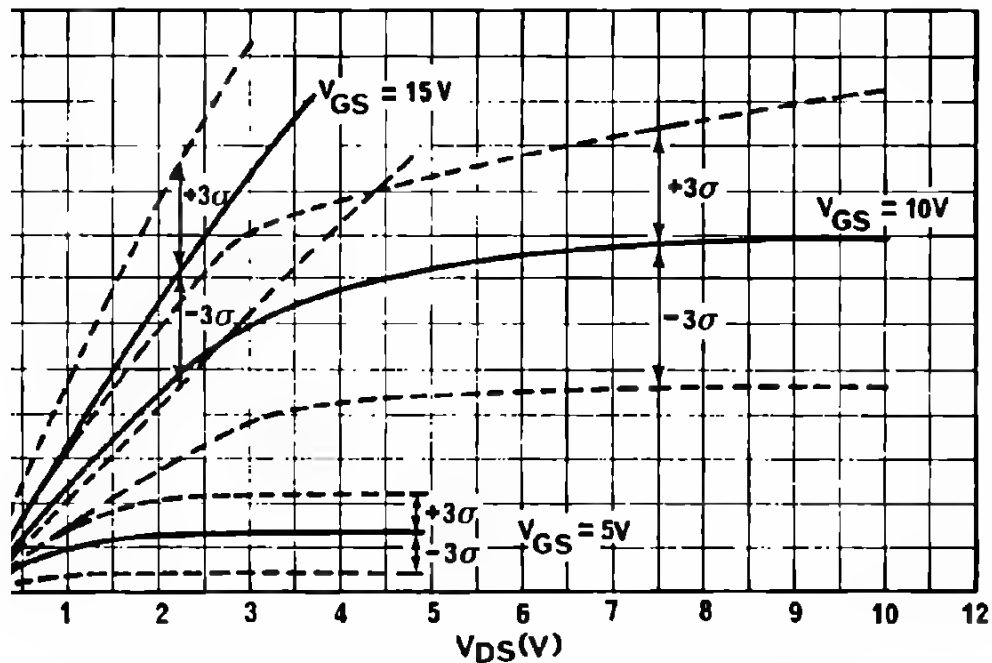


Fig. 18
MINIMUM AND MAXIMUM CURRENT TRANSFER CHARACTERISTICS

ty devices were tested and the maximal and minimal current transfer characteristics are given for $V_{DD} = 10$ and 15 volts. The output characteristics of IOS devices play an important role. A large output current is required to charge and discharge the load capacitance in order to achieve a reasonable speed. The output characteristics generally known as the n-channel and p-channel characteristics or n- and p-drain characteristics are also sometimes called "current



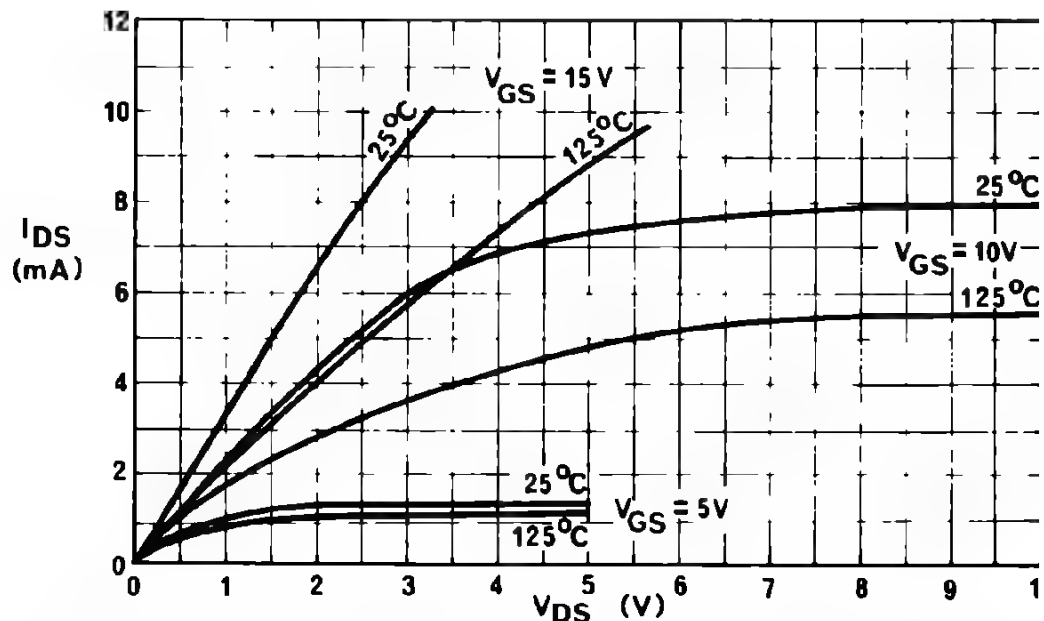
TYPICAL P-CHANNEL DRAIN CHARACTERISTICS
(calculated statistical values) MC14011AL - 50 units - $T = 25^{\circ}C$



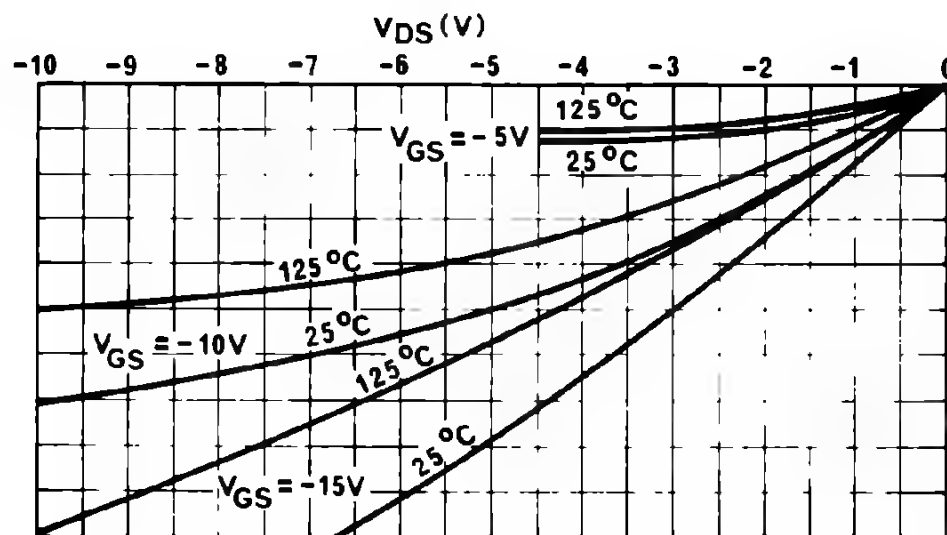
TYPICAL N-CHANNEL DRAIN CHARACTERISTICS
(calculated statistical values) MC14011AL - 50 units - $T = 25^{\circ}C$

Fig. 19 CMOS OUTPUT CHARACTERISTICS

source capability" and "current-sinking capability" respectively. In Figure 19, n-channel and p-channel characteristics are shown as a statistical result of the measurement on 50 MC 14011 AL devices. The arithmetic mean and the spread of $\pm 3\sigma$ values is shown for a V_{DD} of 5, 10 and 15 volts. With increasing V_{DD} , the impedance of the conducting channel decreases. The output source and sink currents are dependent on temperature; this is illustrated in Figure 20 for both n- and p-channels at temperatures of 25°C and 125°C.



TYPICAL N-CHANNEL DRAIN CHARACTERISTICS (calculated statistical values)
Arithmetic mean values at $T = 25^{\circ}\text{C}$ and $T = 125^{\circ}\text{C}$ · MC14011 · 50 units · $T = 25^{\circ}\text{C} - 125^{\circ}\text{C}$



TYPICAL P-CHANNEL DRAIN CHARACTERISTICS (calculated statistical values)
Arithmetic mean values at $T = 25^{\circ}\text{C}$ and $T = 125^{\circ}\text{C}$ · MC14011AL · 50 units · $T = 25^{\circ}\text{C} - 125^{\circ}\text{C}$

Fig. 20

TEMPERATURE DEPENDENCE OF CMOS OUTPUT CHARACTERISTICS

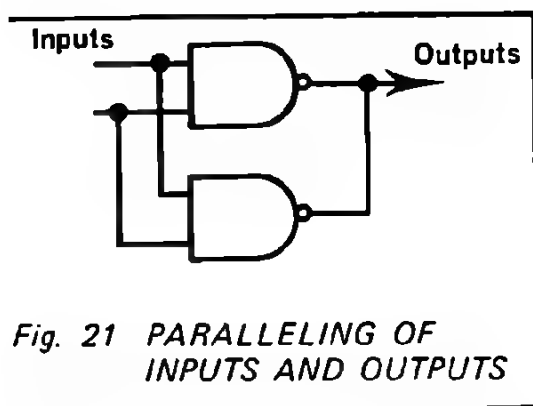


Fig. 21 PARALLELING OF INPUTS AND OUTPUTS

The output source and sink characteristics play an important role when CMOS is designed to interface with TTL, DTL, ECL or used for driving the base of p-n-p or n-p-n bipolar transistors. Source and sink capabilities of gates and inverters can be increased by paralleling inputs and outputs of similar devices in the same package. The current capabilities increase in proportion to the number of inputs/outputs paralleled

see Fig. 21). Increasing the drive output current capability causes a slight increase in switching speed.

As was mentioned earlier, propagation delays and transition times for a given CMOS circuit are dependent on the output capacitance. Figure 22 illustrates a suitable arrangement for testing the switching speeds. Input rise and fall times are adjusted to 20 ns and the output rise and fall times, t_r , t_f , are measured from 10 to 90 percent of the voltage transition. Propagation delays, t_{PHL} , t_{PLH} , are measured from the 50 percent point of the input to the 50 percent point of the output.

Some typical switching speed characteristics are shown in Figure 23, as a function of load capacitance and power supply. It is evident that the switching speed can be altered by changing the power supply voltage and that increasing load capacitance decreases switching speed. The NAND and NOR gates working at 10 to 15 volts with 15 pF load capacitance, operate with 12 to 25 ns propagation delays. This, of course, is higher than for TTL, but it is sufficient for many digital applications.

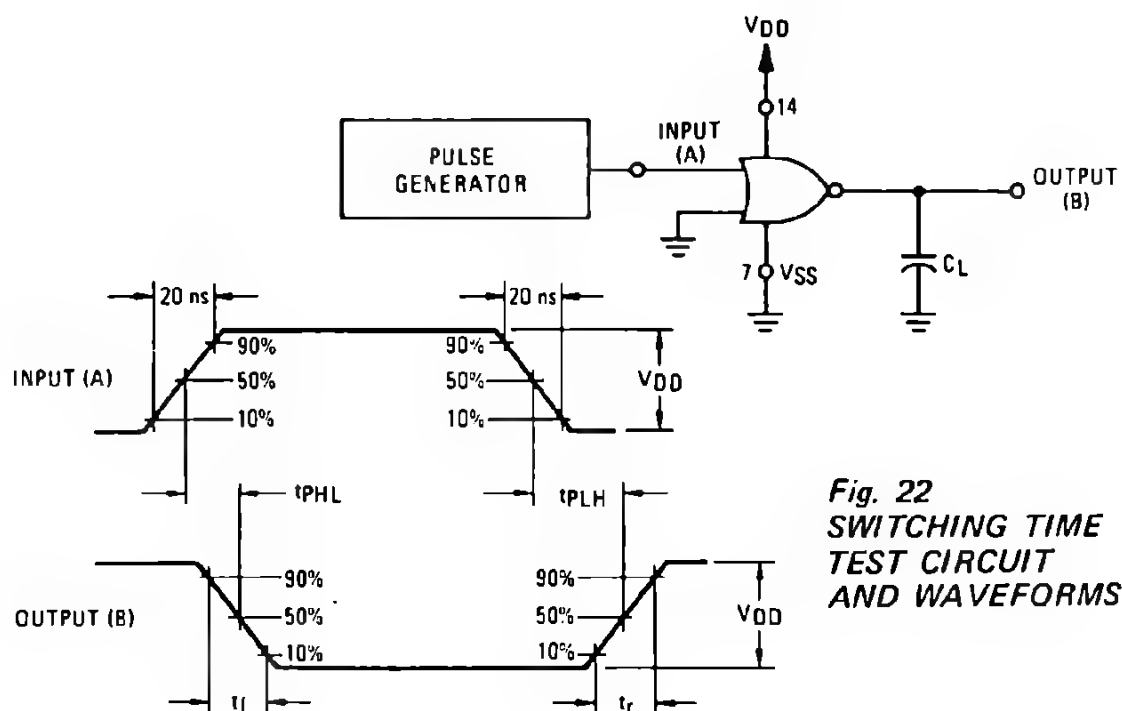


Fig. 22 SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

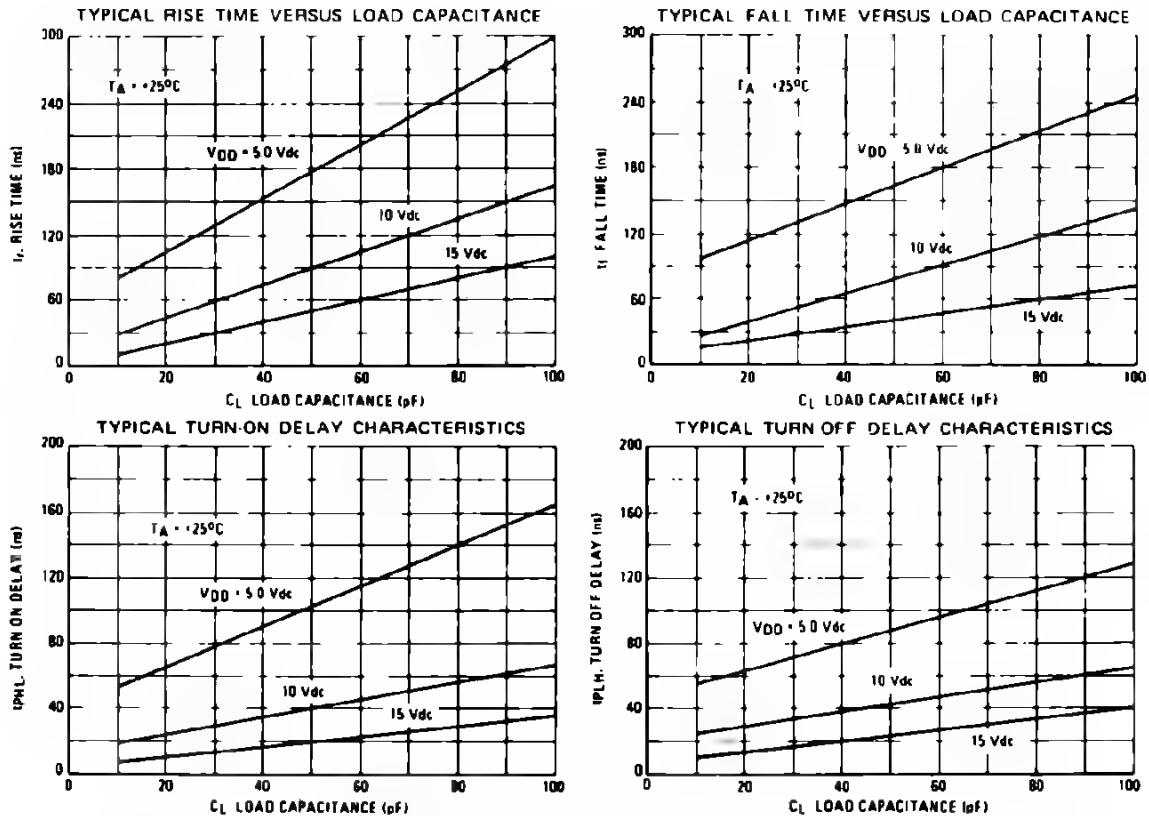


Fig. 23 Dependence of the switching times on load capacitance and power supply voltage (MC 14001 AL)

3. POWER DISSIPATION CHARACTERISTICS

Power dissipation is an extremely important consideration when large numbers of devices are involved; it may be the ultimate limitation in determining device packing density. CMOS devices show a standby power dissipation P_{st} in the order of nanowatts only. However, when a CMOS circuit switches, a considerable amount of current flows during the switching interval.

The power dissipated during switching, under the assumption of a step input voltage and capacitive load can be found by using the model shown in Figure 24

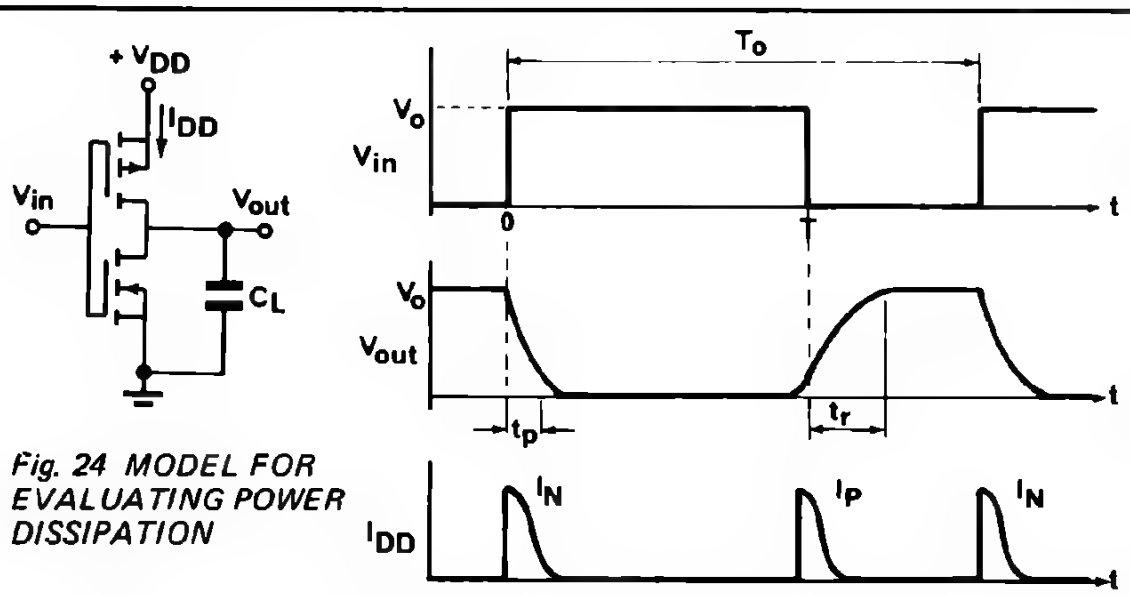


Fig. 24 MODEL FOR EVALUATING POWER DISSIPATION

The average power dissipation for a square-wave input voltage is given by: [1].:

$$P = \frac{1}{T_o} \int_0^{T_o/2} I_N \cdot V_{out} dt + \frac{1}{T_o} \int_{T_o/2}^{T_o} I_P \cdot (V_{DD} - V_{out}) dt$$

Supposing that $I_N = I_P = C_L \cdot (dV_{out}/dt)$ (for step inputs only)

$$P = \frac{C_L}{T_o} \int_0^{V_{DD}} V_{out} dV_{out} + \frac{C_L}{T_o} \int_{V_{DD}}^0 (V_{DD} - V_{out}) d(V_{DD} - V_{out})$$

$$P = \frac{C_L V_{DD}^2}{T_o} = C_L \cdot V_{DD}^2 \cdot f_o$$

8

The total dissipation P_D is given by:

$$P_D = P_{st} + P$$

$$P_D = P_{st} + C_L \cdot V_{DD}^2 \cdot f_o$$

For a step input, the average power dissipation is directly related to the energy required to charge and discharge the circuit capacitance C_L to the supply voltage V_{DD} and the switching frequency. This power is independent of the device parameters.

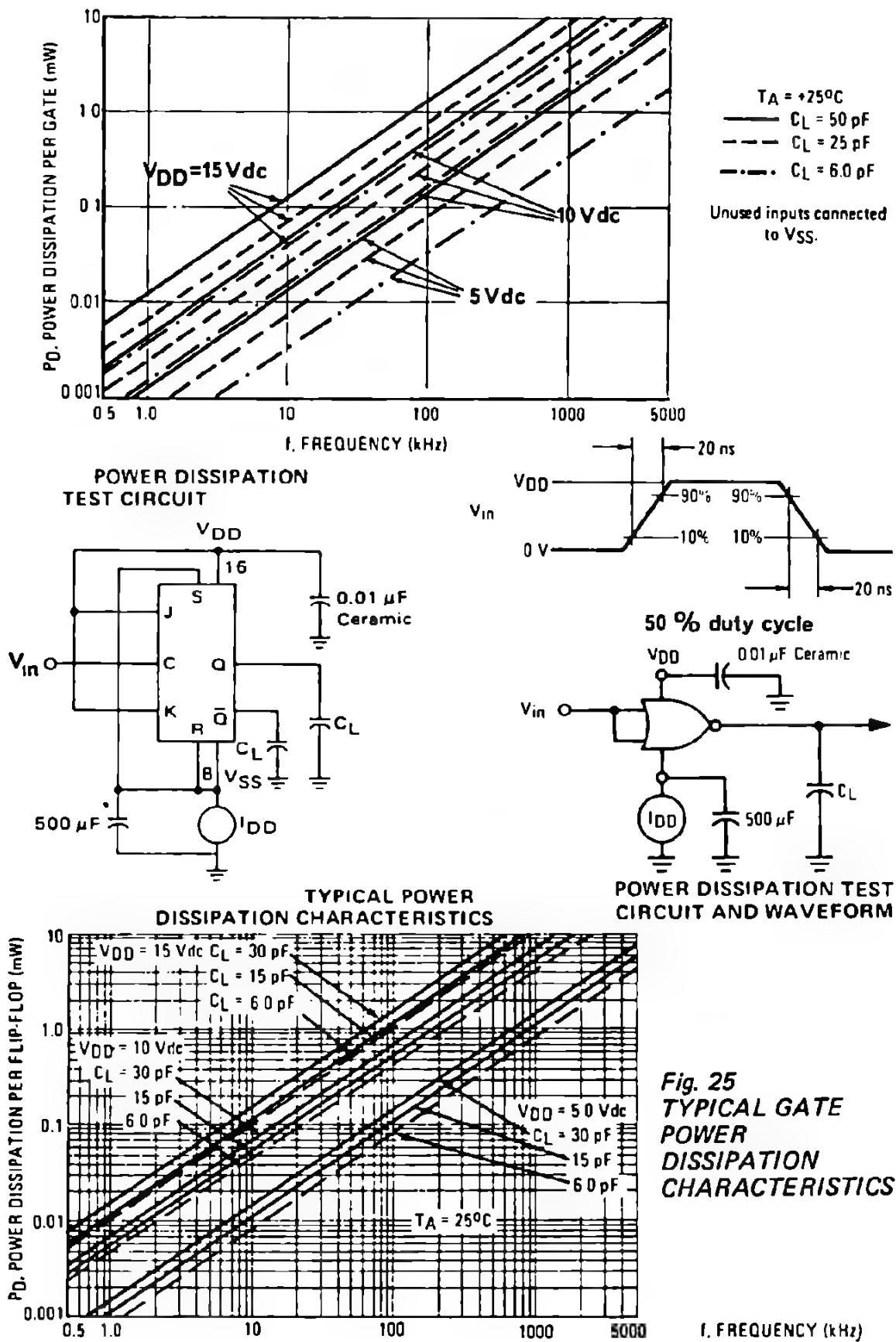
When testing CMOS devices for power dissipation characteristics, the transition times of the input voltage are adjusted to 20 ns, a good approximation of a step function for CMOS devices.

The shape of the input wave is depicted in Figure 25, together with the test circuits for the NOR gate MC 14001 and the J-K flip-flop MC 14027. The results as a function of frequency obtained for different values of load capacitance C_L and supply voltage V_{DD} are also shown.

The expression (8) was obtained for the step input voltage (zero rise and fall times). When the input has a "non-zero" rise time, the situation is different, since not all the current is used for charging the load capacitance. The device remains longer in the state when both n- and p-transistors are conducting. Figure 26 illustrates how the power dissipation of a CMOS gate is determined by the input transition times for a fixed frequency—100kHz. For lower V_{DD} , the equation (8) is valid even for the longer rise and fall times, however, for power supply voltages higher than $V_{DD} = 10V$, as the input rise and fall times increase beyond 200 ns, power consumption of a CMOS device is higher than given by equation (8). This is really not usually a critical factor, since in complex CMOS integrated circuits or in large logical systems only a few gates are connected to the input voltages with these slow rise and fall times.

As was mentioned above, current flowing between the V_{DD} and V_{SS} depends on the transition times. This is depicted in Figure 27, for measurements on a NAND gate MC 14011 AL.

The nature of CMOS operation is such that, in either of the two logic states, one of the MOS transistors is ON while the other is OFF. The direct current



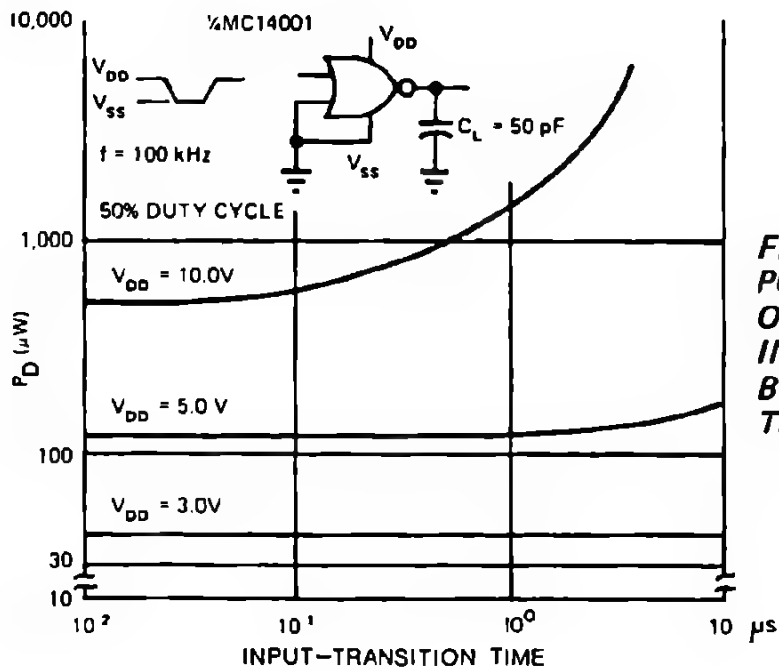
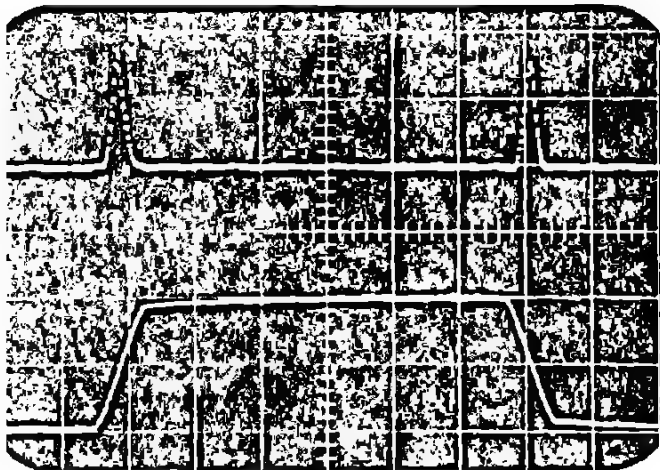
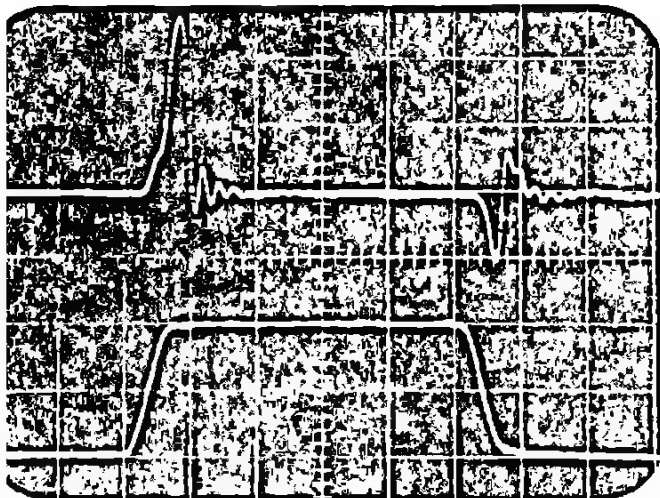


Fig. 26
POWER DISSIPATION
OF A CMOS GATE IS,
IN PART, DETERMINED
BY INPUT-TRANSITION
TIME



Vertically
Drain current I_D
1mA/div.
Input voltage V_{in}
5V/div.

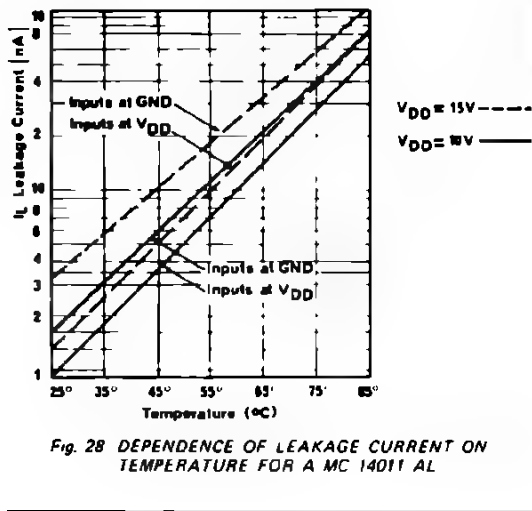
Horizontally
Time
20 μs /div.



Vertically
Drain current I_D
2mA/div.
Input voltage V_{in}
5V/div.

Horizontally
Time
50ns/div.

Fig. 27
CURRENT FLOW
DEPENDENCE ON
TRANSITION TIME



$T_A = 25^{\circ}\text{C}$		
CHARACTERISTIC	Symbol	V_{DD} Vdc
Operating Power Supply Voltage	V_{DD}	—
Quiescent Dissipation	P_D	
Gates		5.0
		10
		15
Dual Flip-Flops		5.0
		10
		15

Table 1 QUIESCENT DISSIPATION

I. CLOCK-WAVEFORM SPECIFICATIONS

The 10–90% maximum clock transition time is specified in the 5 to 15 μsec range, depending on the system transition time (see Table 2). As the system transition time increases, false triggering problems and input errors are considered [4]. In Figure 29, there is a long clock rise time could produce ripple on the triggered storage elements. As long as the clock rise time (t_r) is kept at a value less than the output driving stage for the estimated system, the following parallel-clocked unit as a problem.

Table 2 MAXIMUM CLOCK RISE AND FALL TIMES ($t_r = t_f$ (μs)) LIMITS

Types	$V_{DD} = 5V$	$V_{DD} = 10V$
All except as noted	15	15
Dual "D" Flip-Flop MC14013	5	5
Dual 3-K Flip-Flop MC14027	15	5
Decade Counter/ Divider MC14017 AL Seven Stage Ripple Counter MC14024 AL	No practical limit	

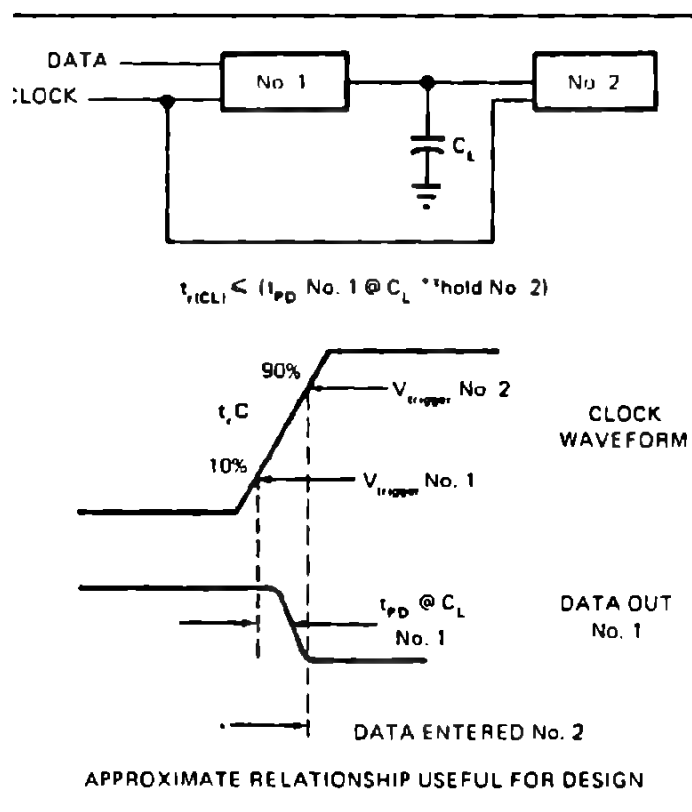


Fig. 29
MAXIMUM CLOCK
TRANSITION TIMES CAN
BE LIMITED BY THE
VOLTAGE THRESHOLD
DISTRIBUTION
Ref. [4]

C VOLTAGE AND ENERGY NOISE IMMUNITY OF CMOS INTEGRATED CIRCUITS

1. GENERAL

The noise immunity of CMOS circuits is dependent on many parameters, such as supply voltage, fan-in and fan-out, stray inductance and capacitance, source of the noise, noise signal shape, individual chip differences. The general analysis of the noise immunity of a logic circuit is a complex process since there are many variables involved. Many manufacturers of integrated circuits characterize the noise immunity of logic circuits in terms of the noise voltage and pulse width which is tolerable. However, rather than using voltages, it is better to define it on the basis of the total energy needed to cause a false output.

CMOS devices usually have higher transfer voltages than other families of logical circuits. However, their energy noise immunity is not necessarily higher, due to the relatively high output impedance, in comparison to devices with lower transfer voltages and smaller output impedances. Furthermore, the noise immunity of a logical circuit family is strongly dependent on its speed. Since noise is capacitively coupled on to the signal-lines, this means that the slower the response time of the logic, the greater the immunity to noise, e.g. ECL circuits are often not considered for use in noisy environment.

Several types of noise must be dealt within a logical system. The following classification of noise is used:

1. External noise —
environmental noise radiated into the system.
2. Power-line noise —
noise coupled through a-c or d-c power distribution system.
3. Ground-line noise —
noise that is created on the ground line because of improper ground returns.
4. Crosstalk —
noise induced into signal-lines from adjacent signal-lines.
5. Transmission-line reflections —
noise from unterminated transmission lines that cause ringing and overshoots.

Noise is a random combination of many sources and as such is extremely hard to analyse. Before describing the test procedure for the noise immunity estimation, the noise immunity specifications will be discussed.

There are the following possible noise immunity specifications:

D-C noise immunity } — Voltage noise immunities
A-C noise immunity }
Energy noise immunity

D-C NOISE IMMUNITY

ise immunity may be defined as the maximum noise voltage that can appear the input without switching an inverter from one logic state to another. itching will not occur if the gain of the inverter is less than unity. There are o points on the transfer characteristics where the gain of the inverter is unity. MOS devices typically reject voltage noise pulses of 45% of the power supply ltage, but the standard guaranteed value throughout the semiconductor in- stry is 30%.

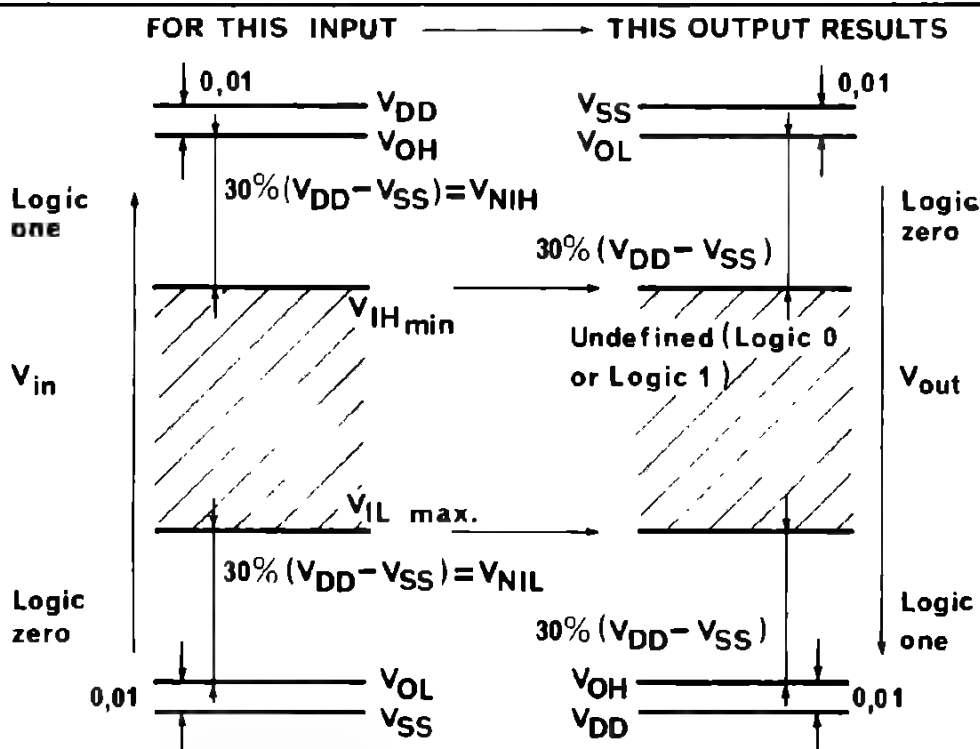
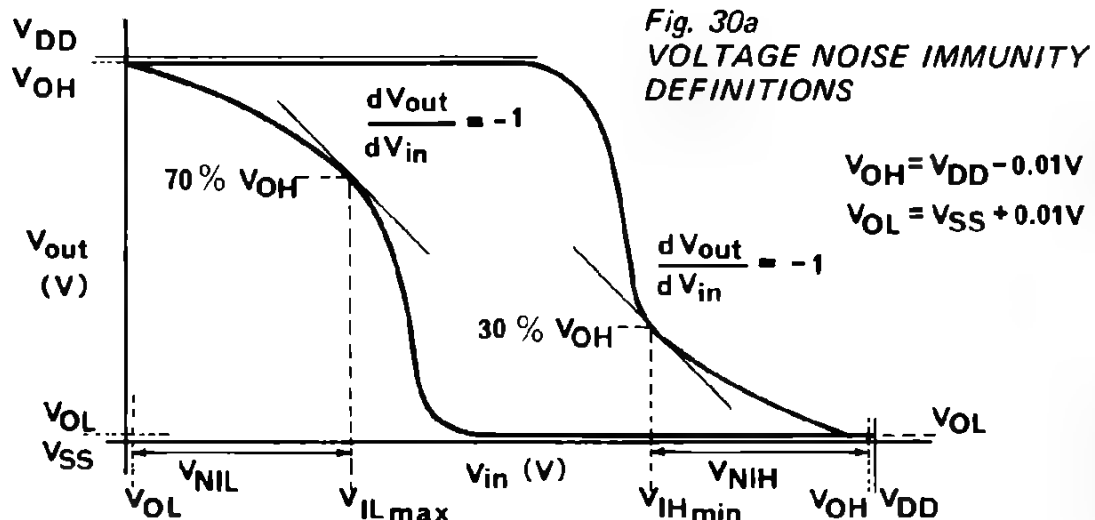


Fig. 30b **VOLTAGE NOISE IMMUNITY GUARANTEED INPUT/OUTPUT RELATIONSHIPS**

CMOS manufacturers have applied the unity-gain, worst case D-C voltage noise immunity definitions, as presented in Figure 30 a and b, where the worst case signal-line d-c noise immunity of a family is defined by the equations:

$$V_{NIL} = |V_{ILmax} - V_{OL}| = \text{low level signal-line noise immunity}$$

$$V_{NIH} = |V_{OH} - V_{IHmin}| = \text{high level signal-line noise immunity}$$

with:

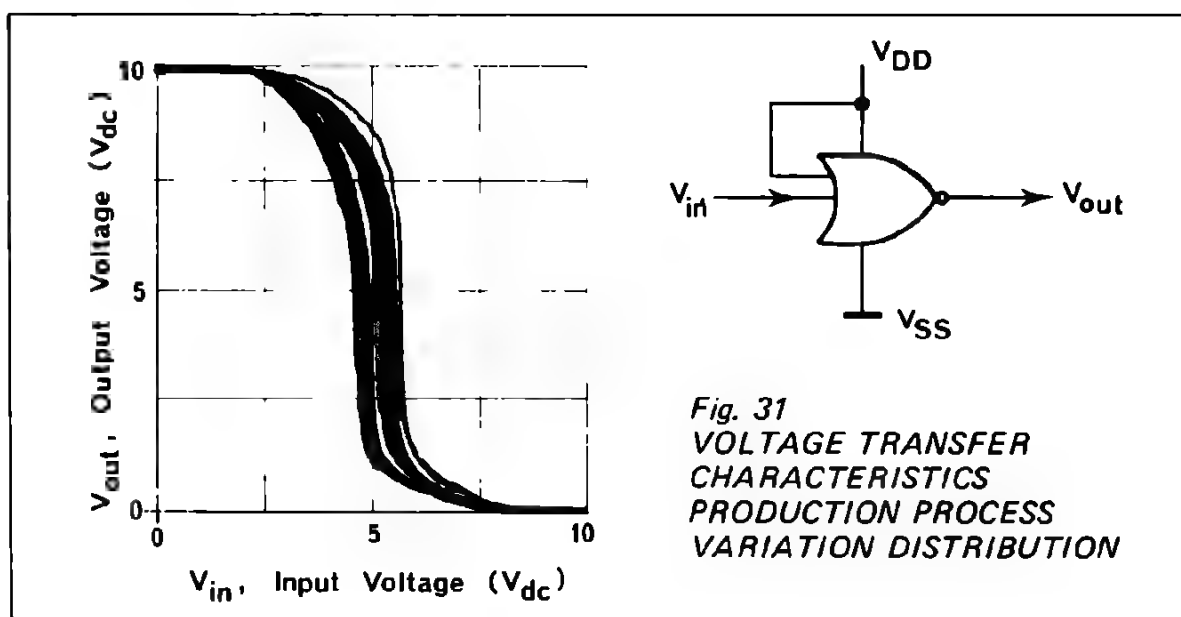
V_{OH} – minimum output voltage at the high level

V_{IHmin} – minimum input voltage at the high level that will guarantee the appropriate output logic level (V_{OH} or V_{OL})

V_{ILmax} – maximum input voltage at the low level that will guarantee the appropriate output logic level (V_{OH} or V_{OL})

V_{OL} – maximum output voltage at the low level.

A relatively large input voltage range remains for which the output logic state is undefined (40% of $V_{DD}-V_{SS}$). This area is needed for the production-process variation (see example Fig. 31 – Voltage transfer characteristics for 50 units of MC 14001) and for allowed voltage transfer curve shifts due to various input combinations of multiple input gates (Fig. 32).



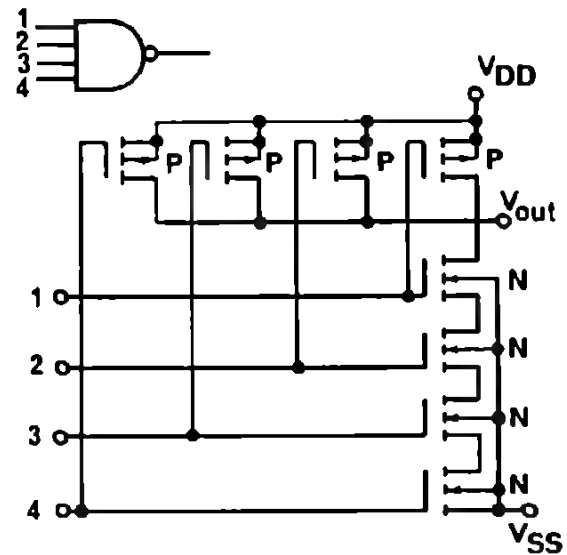
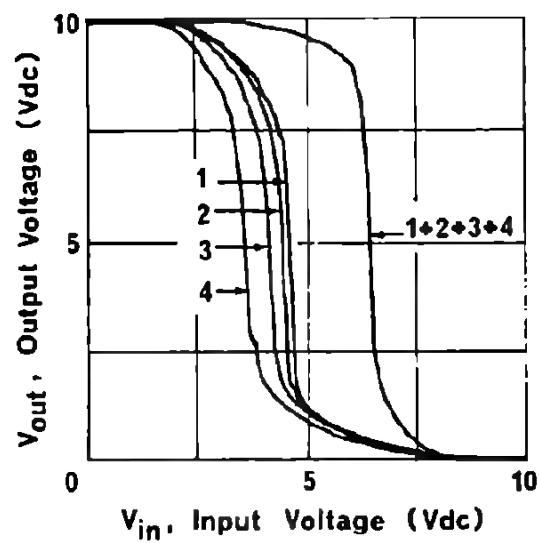
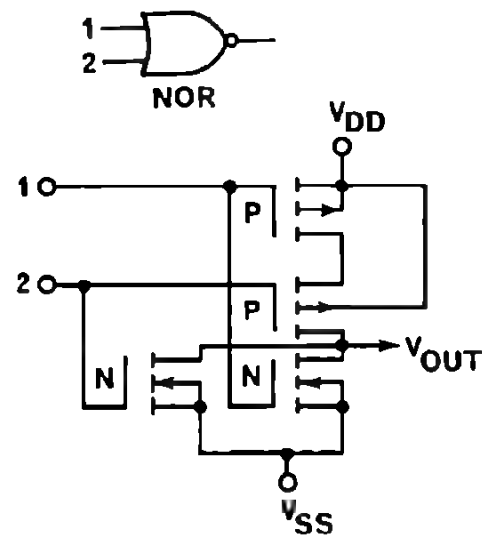
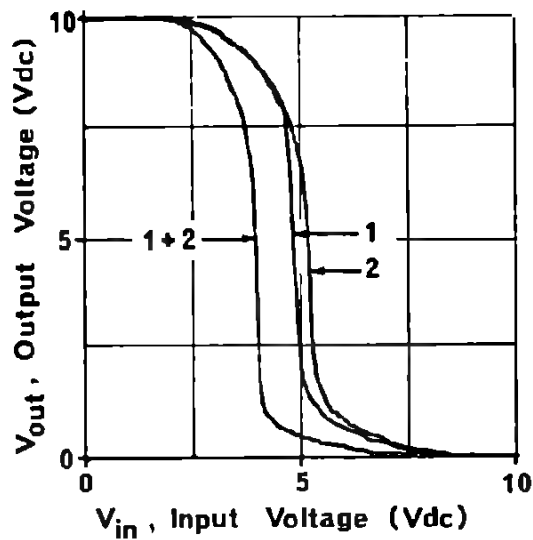
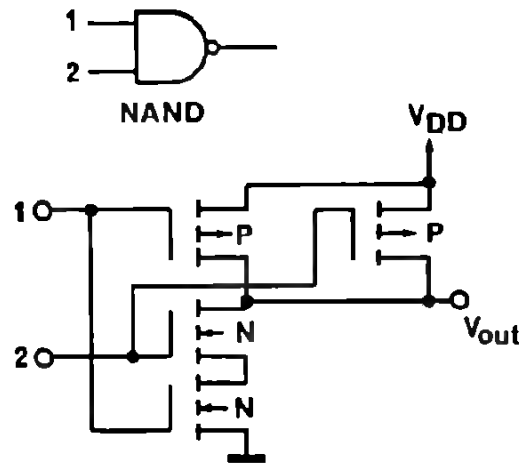
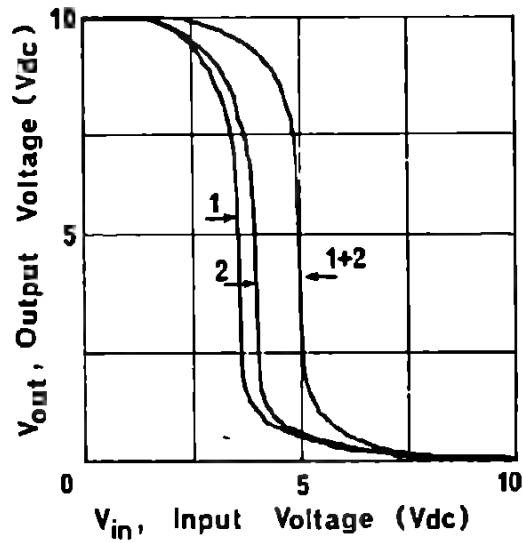


Fig 32 ALLOWED VOLTAGE TRANSFER CURVE SHIFTS DUE TO VARIOUS INPUT COMBINATIONS OF MULTIPLE INPUT GATES.

It appears that 4-inputs is the practical limit when both causes of transfer curve shifts are considered.

An example of D-C noise immunity calculation for a worst-case gate function and using 10V power supply is given below:

a) V_{NIL} = Input low level d-c voltage noise immunity

$$\begin{aligned} V_{NIL} &= (V_{in} @ V_{out} = 70\% V_{OH}) - V_{OL} \\ &= |3.0 - 0.01| \\ &\approx 3.0V \text{ (general assumption)} \end{aligned}$$

b) V_{NIH} = Input high level d-c voltage noise immunity

$$\begin{aligned} V_{NIH} &= (V_{in} @ V_{out} = 30\% V_{OH}) - V_{OH} \\ &= |7.0 - 9.99| \\ &\approx 3.0V \end{aligned}$$

where V_{OL} , V_{OH} values are the guaranteed output voltage levels for the specified temperature range when the CMOS device is driving another CMOS device or a capacitive load.

Depicted in Figure 33, are the voltage noise immunity margins for different V_{DD} . The noise immunity changes very little with temperature, because of the excellent temperature stability of the transfer characteristics (Fig. 10).

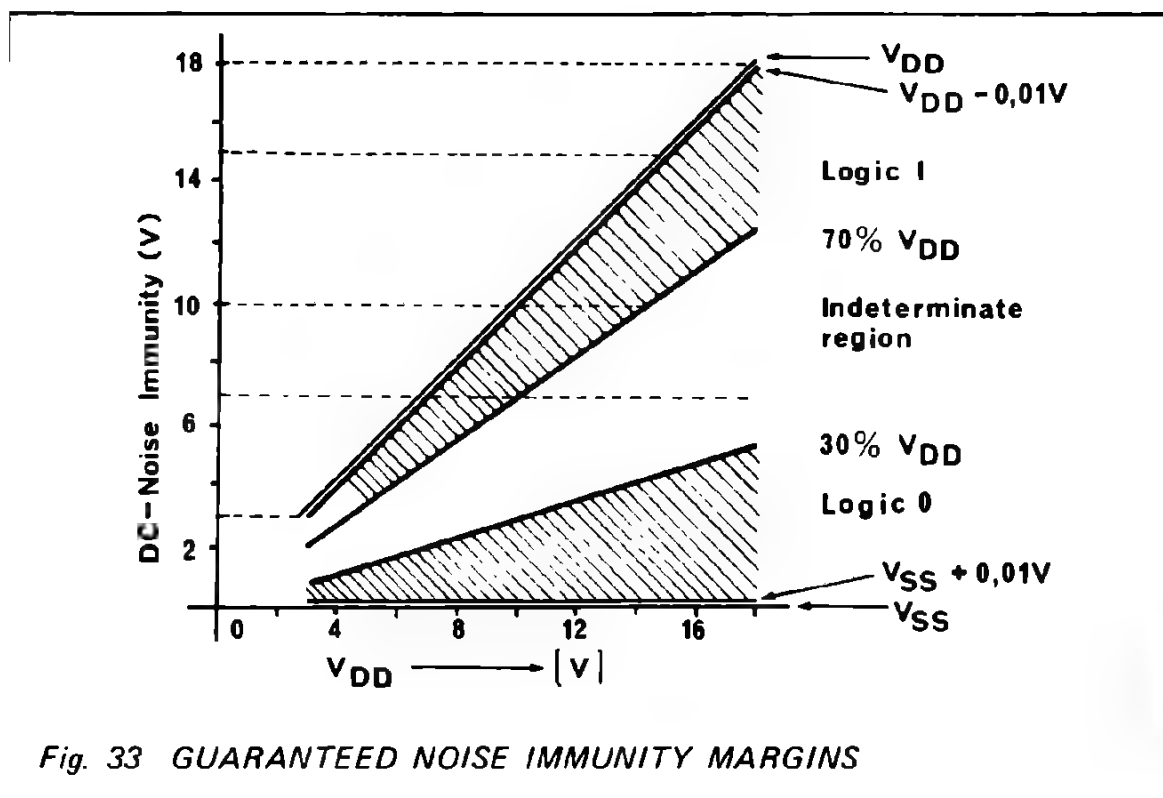
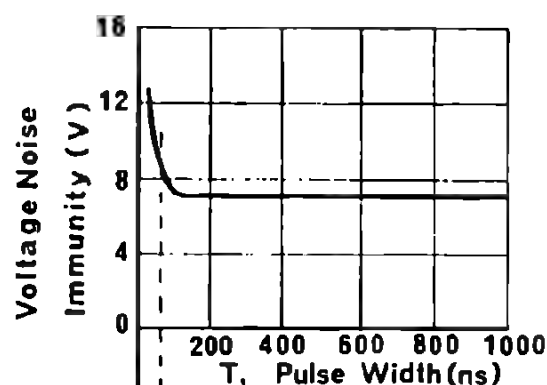


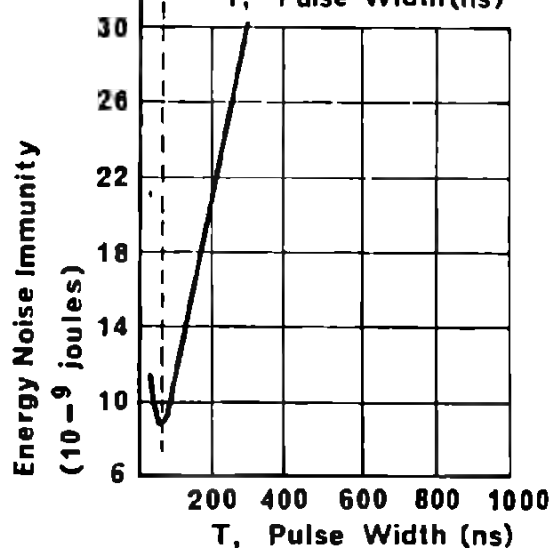
Fig. 33 GUARANTEED NOISE IMMUNITY MARGINS

B. A-C NOISE IMMUNITY

D-C noise immunity predicts only the effects of a steady-state variation in signal line voltage levels. A-C noise immunity extends the noise immunity specifications. It shows the relationship of the amplitude and the pulse width of the noise. It is a function of the propagation delays and output transition times of logic gates, and thus, is a function of the input and output capacitances. An A-C noise immunity plot is shown in Figure 34a and from it the effect of propagation delay on noise immunity is evident. As the noise pulse width approaches the propagation delay of the circuit, the voltage amplitude required to affect the circuit becomes quite high. On the other hand, as pulse width increases, the noise amplitude approaches the D-C noise margin.



a. AC NOISE IMMUNITY PLOT



b. ENERGY NOISE IMMUNITY PLOT

Fig. 34 AC AND ENERGY NOISE IMMUNITIES

4. ENERGY NOISE IMMUNITY

An energy noise immunity specification gives the best characterization of a logic family to withstand noise signals. It takes into account the effects of noise voltage amplitude, the line impedance effect, circuit response time and duration of the noise pulse. A typical energy noise immunity plot is shown in Figure 34b. The noise energy required to affect a circuit reaches a minimum value at the point where A-C energy noise immunity is specified.

The noise can enter the circuit in three ways:

by coupling on gate-to-gate signal-lines

by injection on the power supply leads

by being superimposed on ground points.

This gives us 4 types of logical noise immunity:

logical "0" state signal-line noise immunity

logical "1" state signal-line noise immunity

ground-line noise immunity

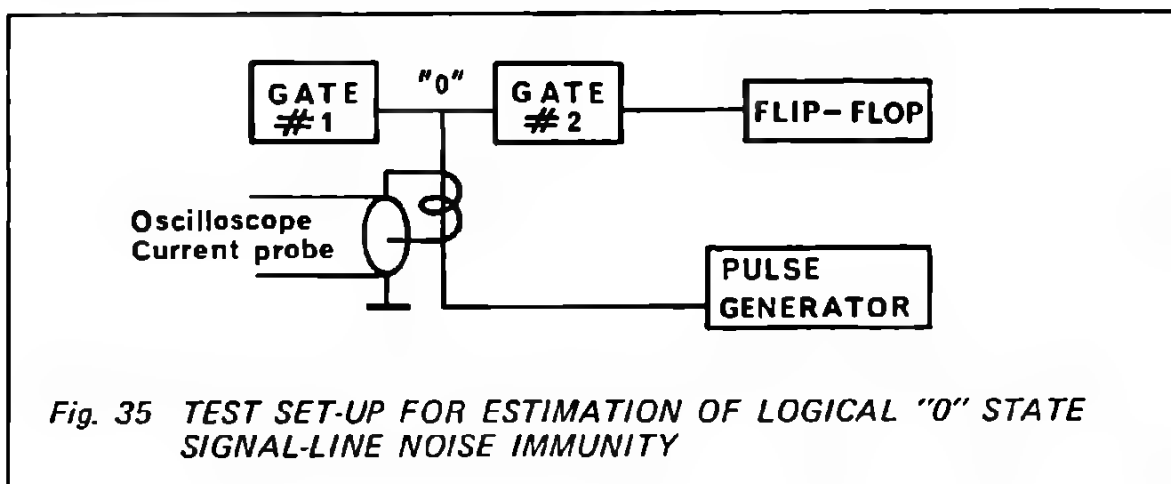
power-line noise immunity.

The basic approach in estimating the noise immunity under question is that a noise input signal is injected into the corresponding line of the gate, at different voltage levels and pulse width, and any false switching noted.

General schematics for the measurement of noise-rejecting characteristics are shown in Figure 35 for estimation of logical "0" state signal-line noise immunity, in Figure 36 for logical "1" state signal-line noise immunity, in Figure 37 for ground-line noise immunity and in Figure 38 for power-line noise immunity.

The ground-line noise immunity test provides information on the immunity to noise injected at the ground terminal. The power-line noise immunity test measures the ability of CMOS circuits to withstand a negative-going noise pulse on the supply-line without a change of state. The effect of the injected noise signal is indicated by the state of flip-flop. When sufficient noise energy is injected, the flip-flop driven by the gate begins to trigger, indicating that the threshold of the injected noise energy has been reached. The energy can then be calculated from the values of U (noise voltage) and I (noise current) and T (pulse

width) according to the formula $E = \int_0^T U \cdot I \, dt$.



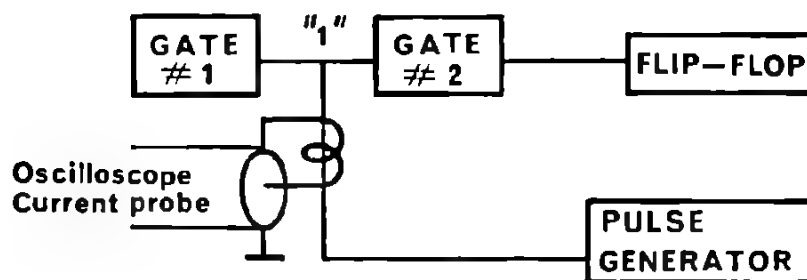


Fig. 36 TEST SET-UP FOR ESTIMATION OF LOGICAL "1" STATE SIGNAL-LINE NOISE IMMUNITY

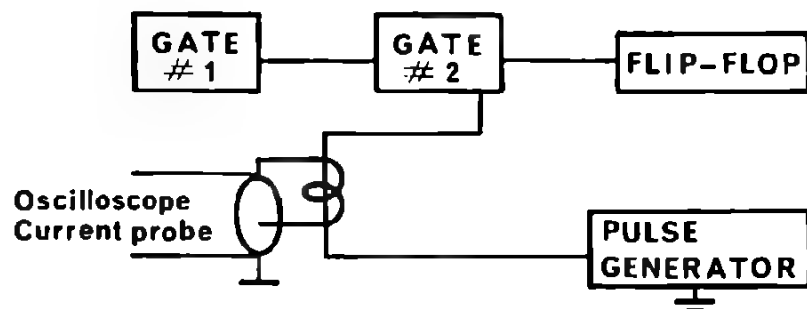


Fig. 37 TEST SET-UP FOR ESTIMATION OF "GROUND-LINE" NOISE IMMUNITY

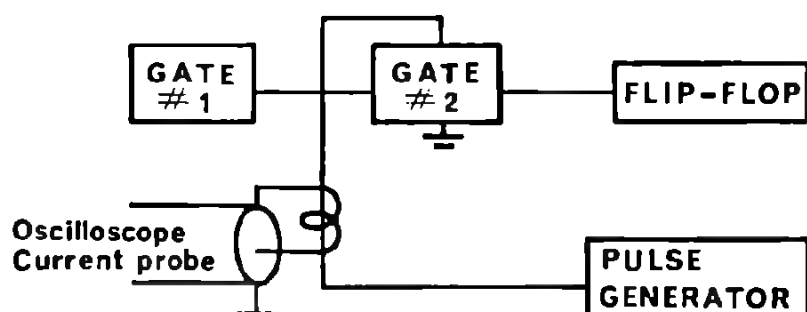


Fig. 38 TEST SET-UP FOR ESTIMATION OF "POWER-LINE" NOISE IMMUNITY

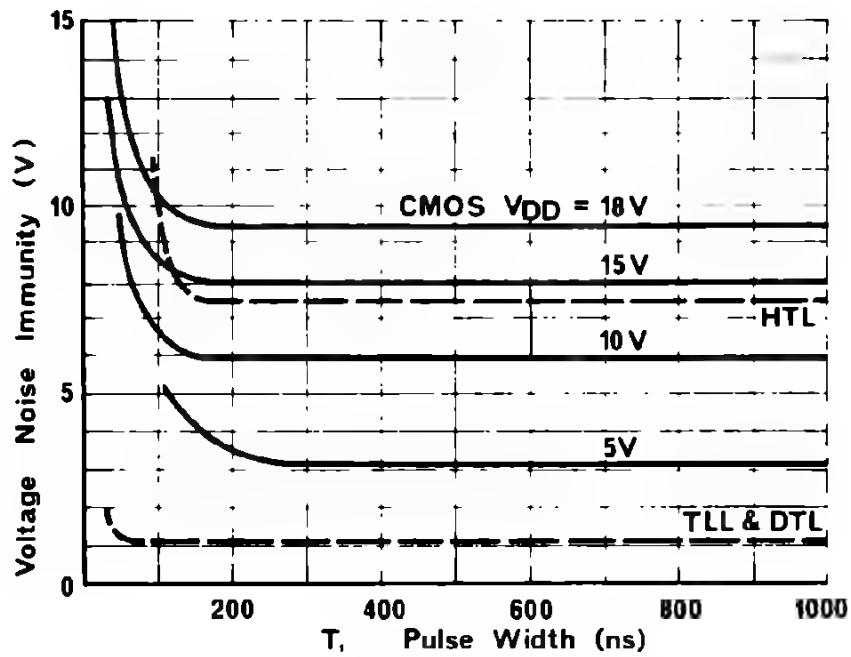


Fig. 39 SIGNAL-LINE VOLTAGE NOISE IMMUNITY, LOGICAL "0" STATE

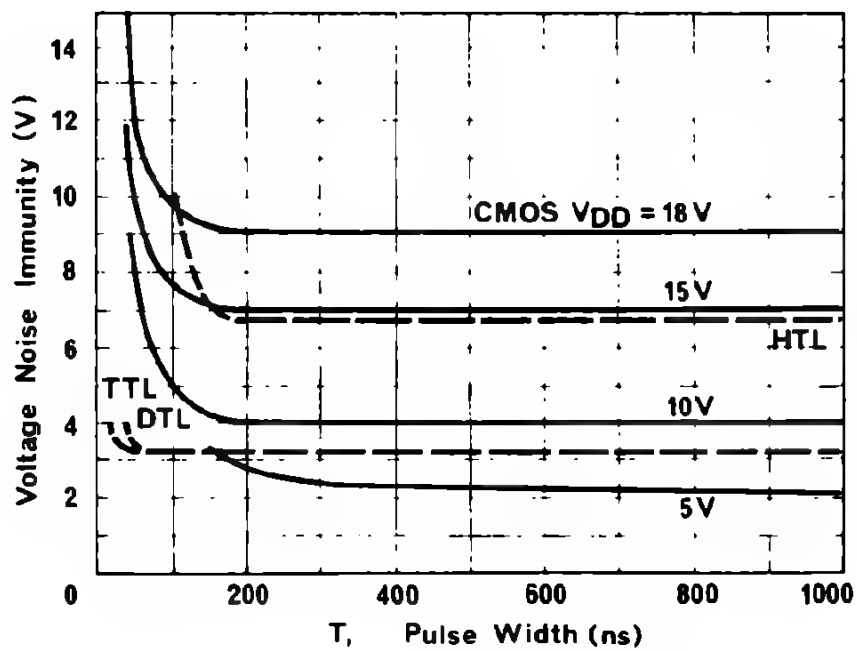


Fig. 40
SIGNAL-LINE
VOLTAGE NOISE
IMMUNITY
LOGICAL "1"
STATE

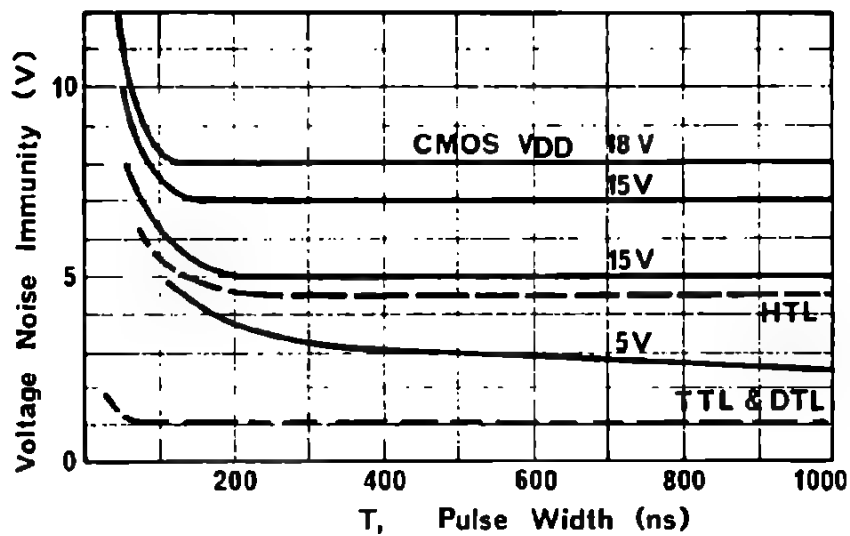


Fig. 41 GROUND-LINE VOLTAGE NOISE IMMUNITY

results for logical "0" and logical "1" state signal-line noise immunity test are shown in Figure 39 and 40. CMOS circuits may be compared with different logic families as shown in Figure 41 for power-line noise immunity and in Figure 42 for ground-line noise immunity.

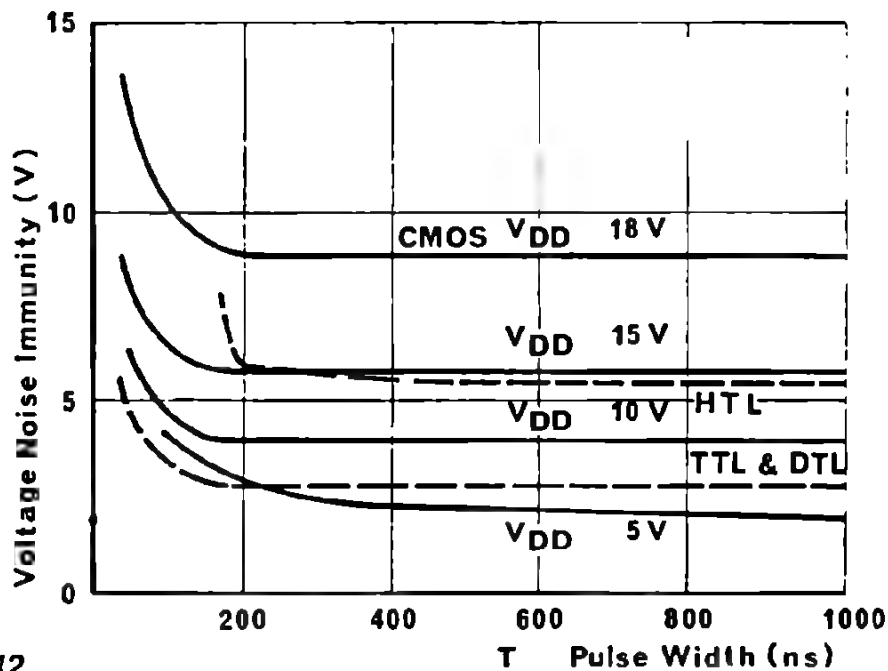


Fig. 42
POWER-LINE VOLTAGE NOISE IMMUNITY

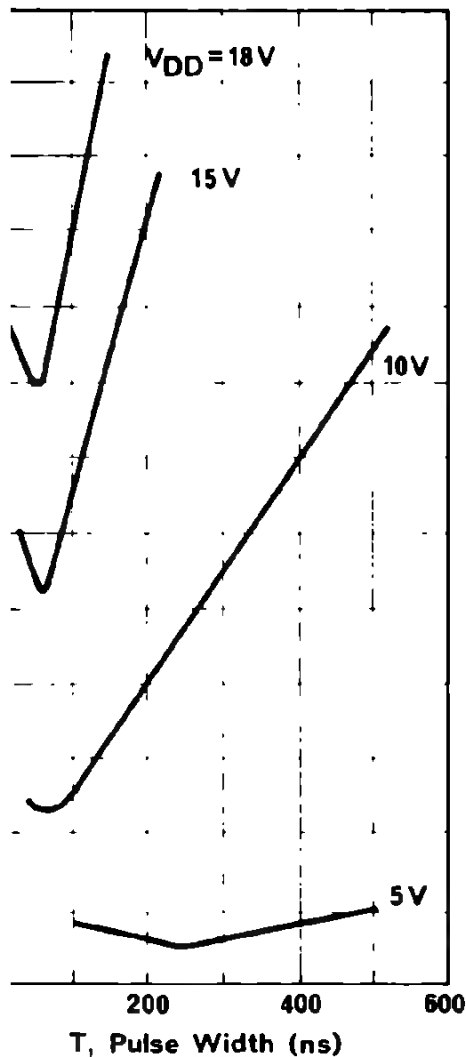


Fig. 43
ENERGY NOISE IMMUNITY
SIGNAL-LINE, LOGICAL "0"
STATE

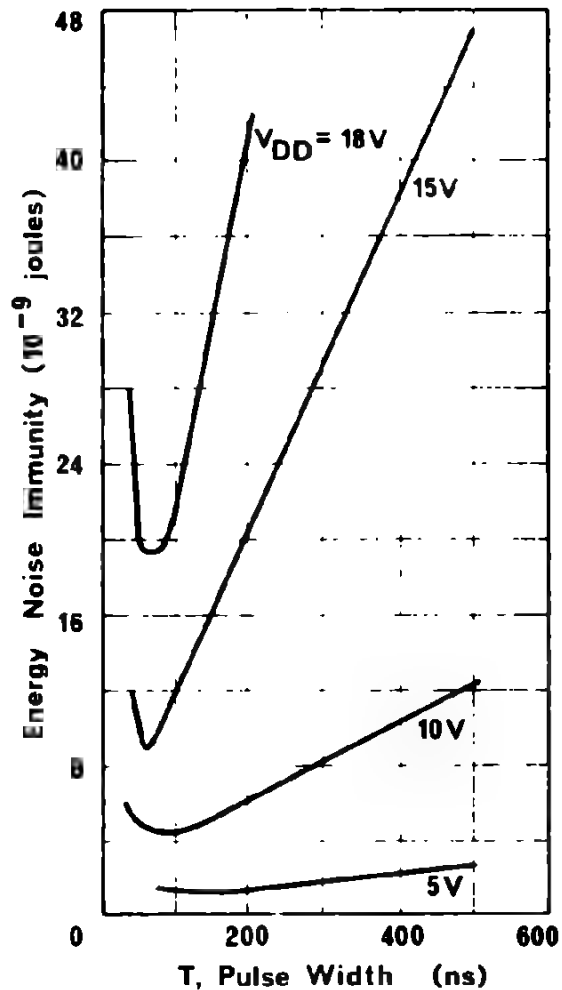
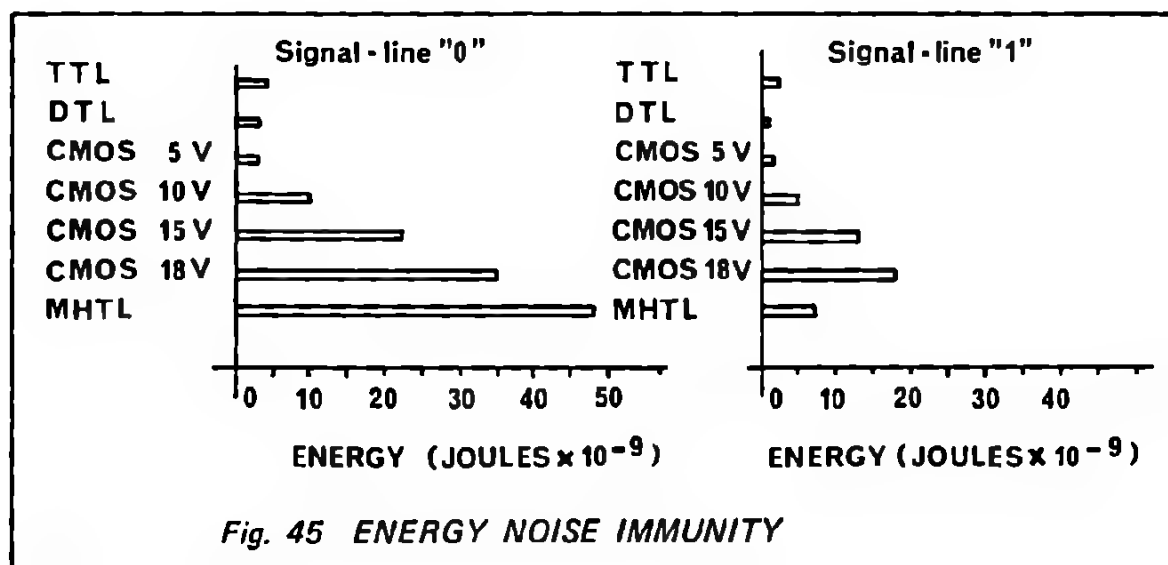


Fig. 44
ENERGY NOISE IMMUNITY
SIGNAL-LINE LOGICAL
"1" STATE

noise immunity for signal-line noise is shown in Figure 43 and 44. If these curves have a minimum which is considered to be, by definition, energy noise immunity for the corresponding V_{DD} .

is proportional to current, voltage and pulse width. In the graph, the rise on the right hand side from the minimum is due to the linear increase in pulse width when values for current and voltage are constant. The sharp rise at the left hand side from the minimum is due to the increase in current and noise voltage values.

The energy noise immunities for different logic families are compared in diagram in Figure 45.



In the Table 3 the basic operating characteristics of different types of logical families and their noise immunities are presented.

CMOS logic gates typically change state near 45% of the supply voltage; their transfer characteristic is very steep at the transition point so very high noise voltages are required to change or falsely switch the output logic state. For power supply voltages higher than 5V, signal-line energy noise immunity for logical "0" and logical "1" state is higher than for TTL and DTL families. HTL shows very high energy noise immunity only for signal-line "0" state. For signal-line "1" state at V_{DD} higher than 10V, CMOS circuits show higher values of energy noise immunity than all other types of logical circuits known. When comparing the noise immunity of different logic families, one should consider not only the noise immunity characteristics, but also the speed. From this point of view, CMOS, working at 15 to 18 volts, seems to be the best of all logic families.

TABLE 3 CHARACTERISTICS OF LOGIC FAMILIES

Defined at 30% of V_{DD} }
 * Defined at 70% of V_{DD} } D.C. resistance

Logic Family	Power Supply (Volts)	Typical Gate Quiescent Power Dissipation (mW)	Typical Propagation Delay (nS)	Typical Signal-Line D-C Noise Immunity (Volts)		Typical Signal Line Impedance (ohms)		Logic Voltage Swing (Volts)
				Low	High	Low	High	
DTL	5	8	30	1	3	50	1.7K	4.5
TTL	5	15	10	1	3	30	140	3.5
HTL	15	30	85	4.5	6	140	1.6K	13
ECL	-5.2	25	2	0.25	0.17	7	7	0.8
CMOS $V_{DD}=5V$	5	$5 \cdot 10^{-3}$	45	2.25	2.75	*600	**1.2K	5
CMOS $V_{DD}=10V$	10	$10 \cdot 10^{-3}$	16	4.5	5.5	*300	**600	10
CMOS $V_{DD}=15V$	15	$15 \cdot 10^{-3}$	12	6.75	8.25	*250	**450	15
CMOS $V_{DD}=18V$	18	$18 \cdot 10^{-3}$	11	8.1	9.9	*220	**430	18

D INPUT PROTECTION CIRCUITS

The gate electrode of a CMOS circuit is completely isolated from the substrate by a silicon dioxide layer, which forms the dielectric of the gate-to-substrate capacitor. The thickness of the oxide insulator between the gate and the substrate of a MOS device is about 1000 Å and has a typical breakdown voltage in the range of 100 to 120V.

If a voltage higher than the breakdown voltage is applied to the gate, the silicon dioxide beneath the gate will rupture. This can result in permanent damage of the device, causing a short between the gate metal and either the substrate or a P or N region. Because of the extremely high resistance of the gate oxide, even such a very low energy source as stray electrostatic charges, is capable of developing this breakdown voltage. Electrostatic charges can be generated by normal handling. The voltage of a static discharge could be tremendous (personnel walking across a waxed asphalt floor can generate static voltages in the range of 10,000 volts; this value depends on humidity, surface conditions, etc.). If the energy stored in the capacity (300 pF) of the human body at these voltage levels is discharged into the input of a CMOS device, it may destroy it.

The possibility that a CMOS device will be destroyed by static overvoltage exists only during the handling and testing. If the device is mounted in a circuit, normal circuit impedances and voltages render damage of this kind impossible. In order to avoid destruction of CMOS devices by static discharge, various input protection circuits were developed.

Static discharges will normally be very short. Tests show that the CMOS devices are fully protected against overvoltage of 100 – 150 volts applied for a maximum of 0.1 μs. (If overvoltage conditions last longer, then the safety margin is reduced according to energy considerations). This is usually sufficient to protect "in socket" overvoltage, but these voltages are one order of magnitude less than typically found in the handling environment. All CMOS data sheets alert users to this phenomenon by cautioning them to avoid application of any voltage higher than maximum device voltage ratings. It is sure that no practical protection circuit known will be able to protect the device against static discharges of the enormous voltages mentioned above, and some handling precautions are recommended for CMOS devices. (See chapter "Reliability".)

MOTOROLA provides input protection on all inputs of CMOS circuits. There are two protection systems used at the present on MOTOROLA CMOS devices: single diode protection, and resistor diode protection circuits. They are shown in Figure 46 and 49. Both protection systems involve the parasitic diodes.

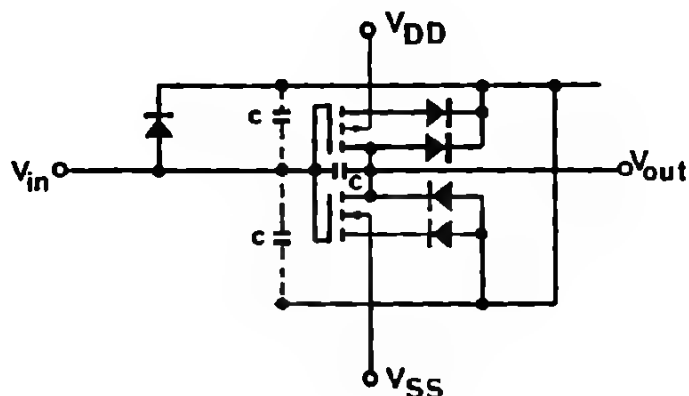


Fig. 46
SINGLE DIODE
PROTECTION CIRCUIT
SCHEMATICS

The single diode protection circuit diffusion cross section is shown in Figure 47. Since the P-tub and N substrate are highly doped, the junction breakdown is high, about 120V. Therefore, a heavily doped N^+ region and a highly doped P^+ region are used for the diodes. The junction between the two regions (N^+ and P^+) breaks down at about 30V which is well below the 100V gate-to-substrate breakdown. The single diode configuration provides protection by clamping excessive positive levels to V_{DD} . Negative protection is provided by the 30V reverse breakdown. The diode is designed to operate in the breakdown region without damage, provided currents are kept under 10 mA. The functional operation of a "single diode protection circuit" is demonstrated in Figure 48.

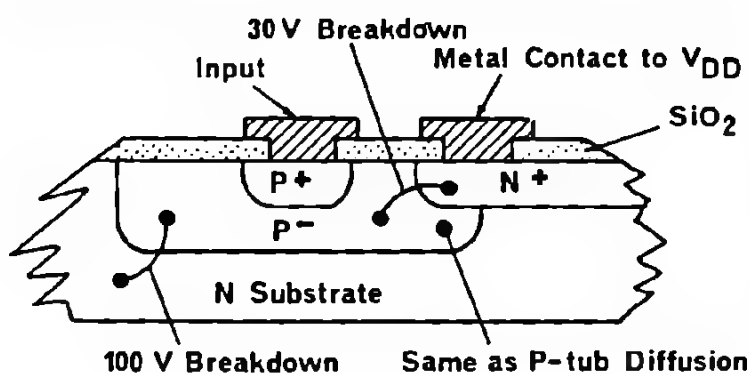


Fig. 47
SINGLE DIODE
PROTECTION CIRCUIT
DIFFUSION
CROSSSECTION

The second type of protection circuit is shown in Figure 49. It consists of a series isolation resistor R_S , whose average value is 1.5 $k\Omega$ and diodes D_1 and D_2 for clamping excess input voltages to the power supply pins, V_{DD} or V_{SS} . Diode D_3 is a distributed parasitic structure resulting from the diffusion fabrication of R_S .

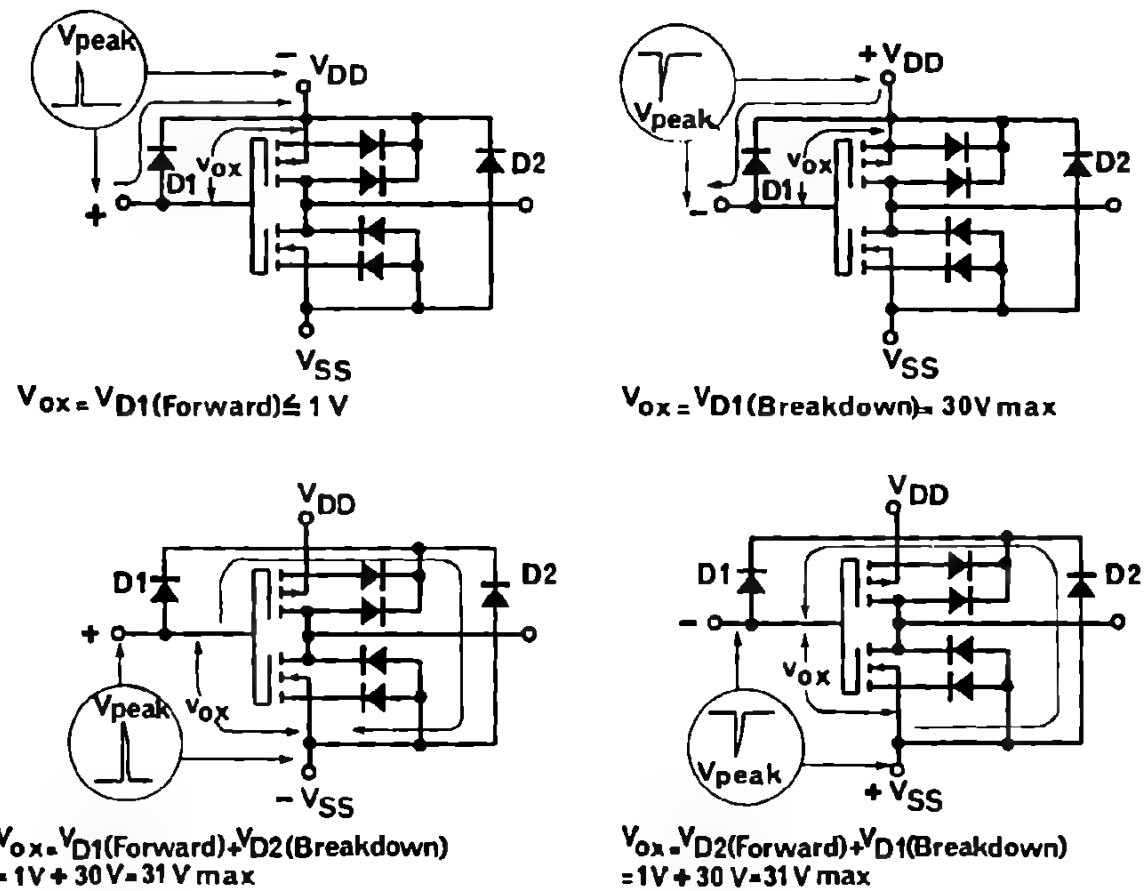


Fig. 48
GATE OXIDE PROTECTION BY SINGLE DIODE PROTECTION CIRCUIT

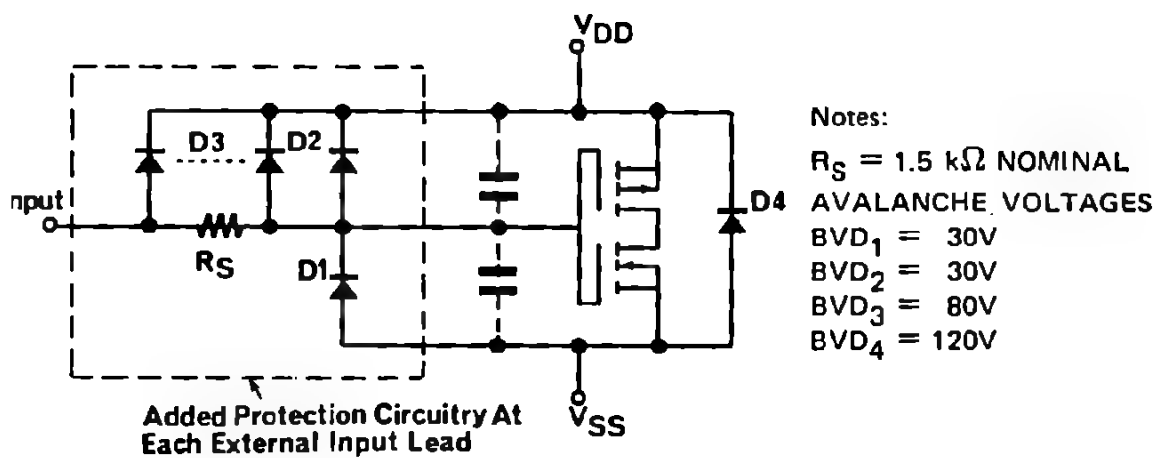


Fig. 49 DOUBLE DIODE PLUS RESISTOR PROTECTION CIRCUIT

Figure 50 shows the surface topology and a diffusion cross section of the protection circuit in its integrated form. An understanding of the physical structure and circuit arrangement will aid in the discussion of its protection capabilities.

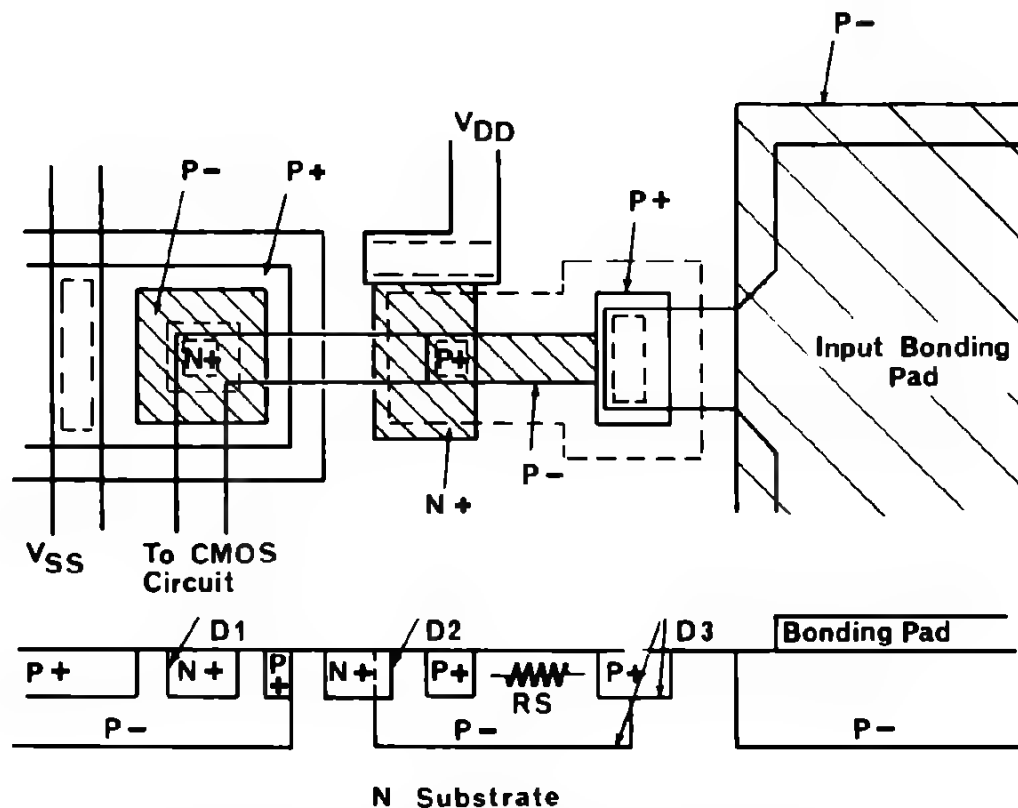


Fig. 50 TOPOLOGY AND DIFFUSION CROSSSECTION OF DOUBLE DIODE PLUS RESISTOR PROTECTION CIRCUIT

structure features:

P⁻ (low concentration of boron impurity ions) diffusion which is placed with the bonding pad to serve as additional protective isolation between pad metallization and N-type substrate. The oxide which is normally more than 1000 Å thick beneath the bonding pad, will only withstand voltages of 600 to 1000 V, well below the static discharge potentials which may be found in this environment.

The 1.5 kΩ series isolation resistor, R_S which is also formed using a P⁻ diffusion. This diffusion has a very large resistance of 1000 ohms per square of device area, which tends to minimize valuable chip surface area. A 1.5 kΩ resistor was chosen as a compromise between added circuit delay, and the need for the greatest possible insulation. For example, with a normal MOS gate capacitance of 5 pF, the 1.5 kΩ resistor will form a 7.5 ns time constant. All signals reaching the internal MOS devices, regardless of the external signal voltage and fall rate will therefore have been delayed and rounded sufficiently to prevent excess energy to be diverted through the protective diodes away from the sensitive MOS gate dielectric.

3. Diode D_1 which is formed by a N^+ enhancement diffusion into a P^- area and has a sharp 30–35V avalanche breakdown characteristic. D_1 limits the MOS gate substrate potential during positive input overvoltages to well below the critical gate dielectric rupture level.

4. Diode D_2 which has identical avalanche characteristics to D_1 . As shown in Figure 50, it is fabricated with the same N^+ to P^- junction and is included to maintain gate potentials within safe levels during negative input overvoltages.

5. Series diode resistance which is minimized by bringing power bus lines, V_{DD} and V_{SS} , as close to the diode junctions as manufacturing tolerances will allow. There are four protection categories for applying either a positive or negative overvoltage between

input pin and V_{DD} (Fig. 51a and b)

input pin and V_{SS} (Fig. 51c and d).

For each case, V_{ox} , the maximum steady potential which appears across the gate oxide dielectric, is listed. Both forward and reverse diode characteristics are used to maintain safe levels.

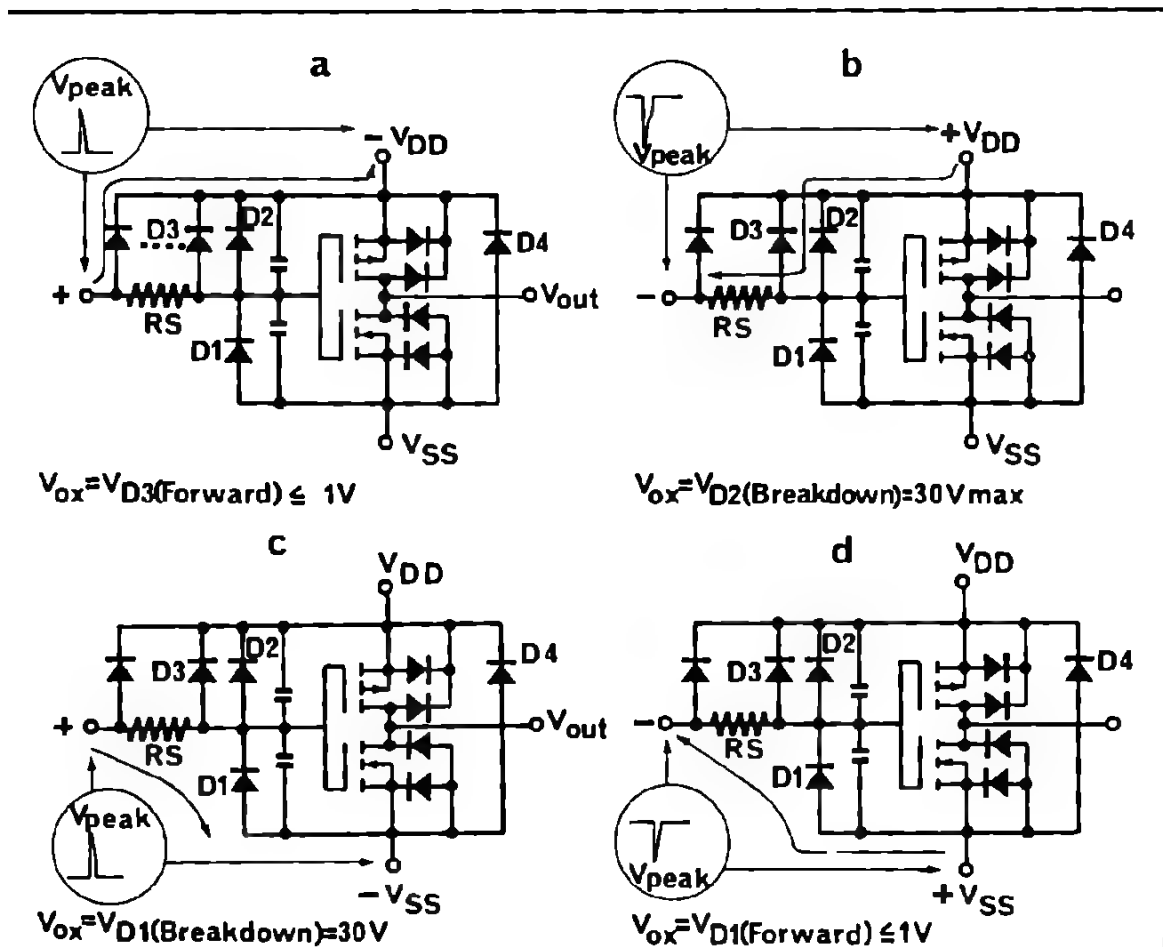
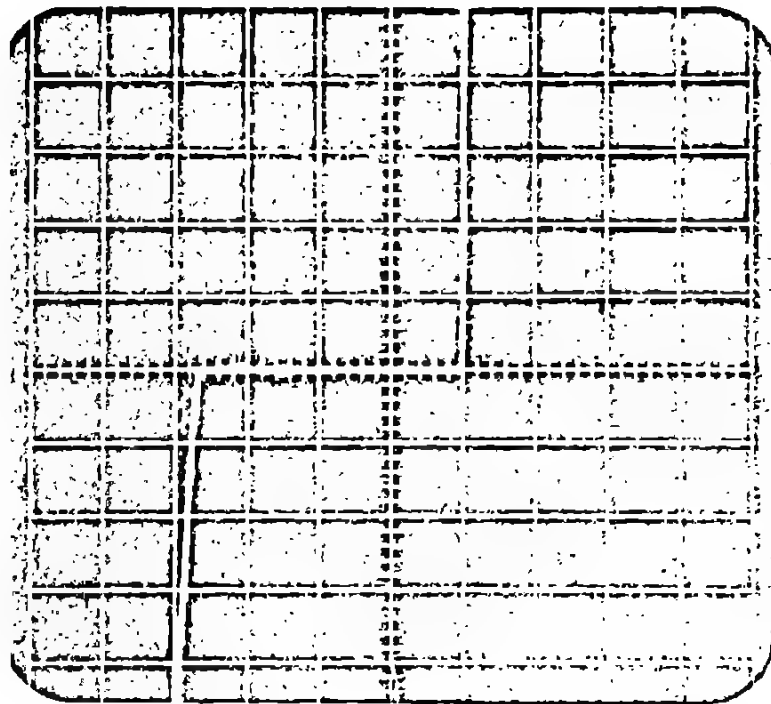


Fig. 51

GATE OXIDE PROTECTION BY RESISTOR DIODES PROTECTION CIRCUIT

The voltage current characteristics of both protection $V_{DD} = 10V$ ($V_{SS}=0V$) are shown in Figure 52 and diode protection circuit, clamping for negative pulses volts, which is well below the gate-to-substrate break For the double diode and resistor protection circuit, mately minus 1V.

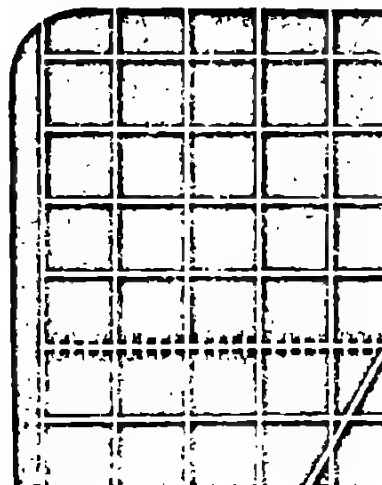
Both methods provide adequate input protection. Ho taken in handling the devices are still of great impor



$$X = 5V/cm$$

$$Y = 1mA/cm$$

Fig. 53
**DOUBLE DIODE
AND RESISTOR
PROTECTION
CIRCUIT**



E REFERENCES

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- [2] R.S.C. COBBOLD "Theory and applications of field-effect transistors" John WILEY and Sons, New York, 1970
- [3] J. McCULLEN "MOTOROLA Complementary MOS I/C's" MOTOROLA Semiconductor Products Inc. Application Note AN-538A
- [4] B. SCHMIDT "Using CMOS in system designs — Those all-important details" MOTOROLA Semiconductor Products Inc. Application Note AN-591.

Fundamental logic
configurations

FUNDAMENTAL LOGIC CONFIGURATIONS

FUNDAMENTAL LOGIC CONFIGURATIONS

1. COMBINATORIAL LOGIC FUNCTIONS

- 4.1.1. OR FUNCTION GENERATION
- 4.1.2. NOR FUNCTION GENERATION
- 4.1.3. AND FUNCTION GENERATION
- 4.1.4. NAND FUNCTION GENERATION
- 4.1.5. LOGICAL "SUM OF PRODUCT"
- 4.1.6. LOGICAL "PRODUCT OF SUM"
- 4.1.7. EXCLUSIVE OR
- 4.1.8. MULTIPLEXERS USED TO SOLVE COMBINATORIAL EQUATIONS
- 4.1.9. DECODER FUNCTIONS

2. SEQUENTIAL LOGIC FUNCTIONS

- 4.2.1. FLIP-FLOPS
- 4.2.2. LATCHES
- 4.2.3. SHIFT REGISTERS
- 4.2.4. COUNTERS

FUNDAMENTAL LOGIC CONFIGURATIONS

A proper understanding of the operation of the basic logic functions in the CMOS family is mandatory, in order to optimize the price/performance ratio of any system.

Therefore, in this chapter two main sections will be considered:

- The combinatorial logic functions
- The sequential logic functions.

Firstly, we will show several examples of combinatorial logic functions using CMOS circuits. Secondly, in the sequential logic function section, we will describe the flip-flops, latches and shift registers which are available. Finally, we will present in detail the operation of the counters available in the CMOS families.

It should be mentioned that in this chapter, practically no electrical performances will be discussed. For this information, reference should be made to the data sheets.

1. COMBINATORIAL LOGIC FUNCTIONS

This section indicates common logic diagrams which use standard combinatorial CMOS circuits.

For the combinatorial examples, two types of circuit configuration are shown:

- one type uses only CMOS gates mainly for low power applications.
- the other type also uses diode arrays in conjunction with CMOS gates. In this case a loss in voltage noise immunity (V_{NIL}) of about 0.6V as well as line noise immunity has to be considered and the additional power dissipation has also to be taken into account.

As shown, the usage of complementation of the logic variables usually allows to simplify the circuitry.

In Figure 4.1, the truth table of all fundamental logic functions commonly used is indicated. This table also allows an easy transformation of the functions from the positive logic into the negative logic and vice versa.

The equations shown are related to 3 logical variables.

L = low
H = high

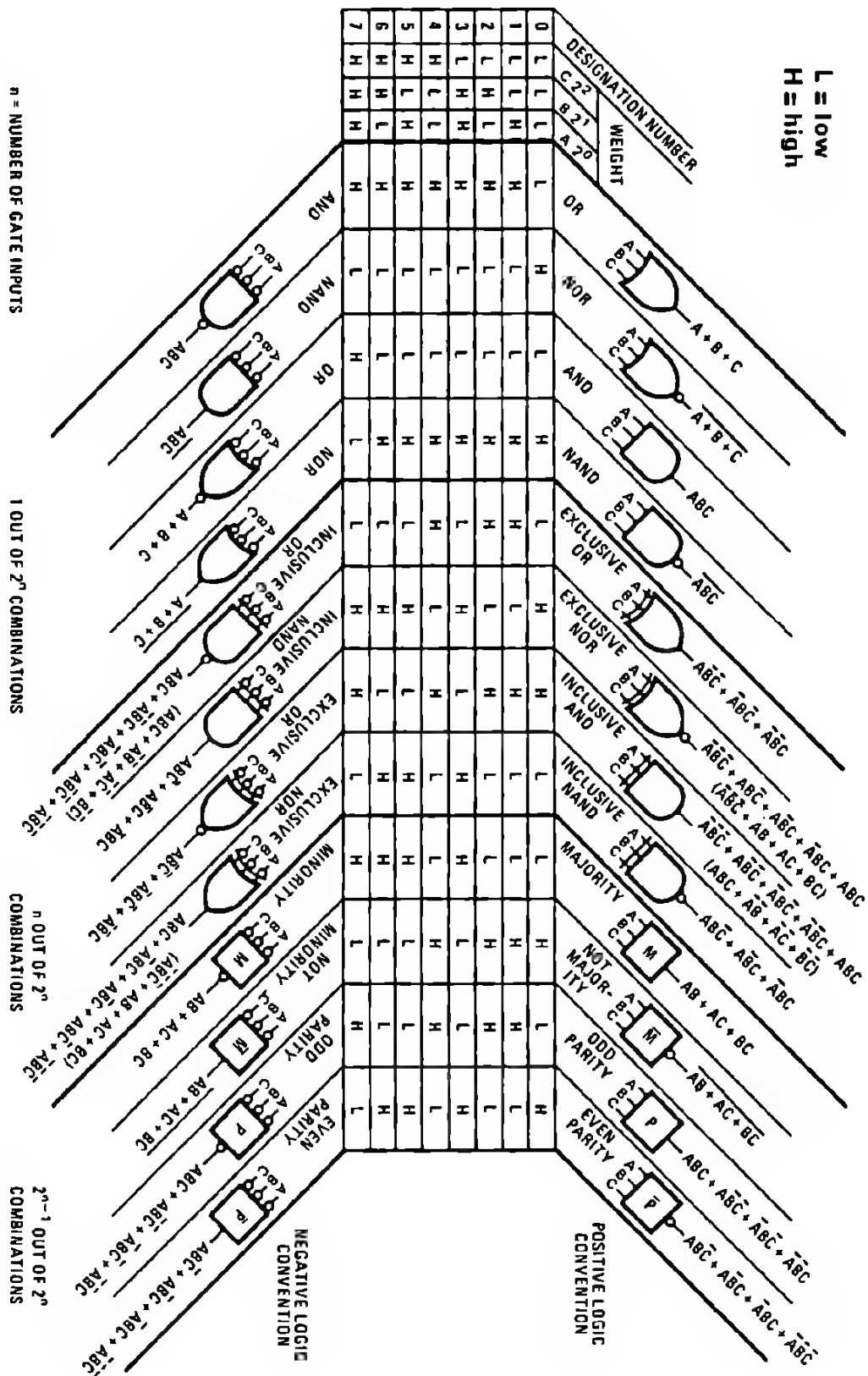
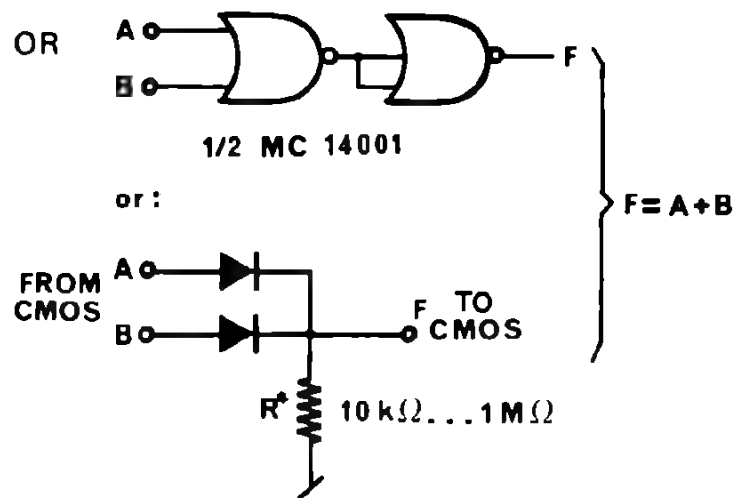


Fig. 4.1 FUNDAMENTAL LOGIC FUNCTIONS

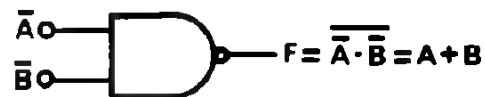
4. 1. 1. OR FUNCTION GENERATION

Examples:

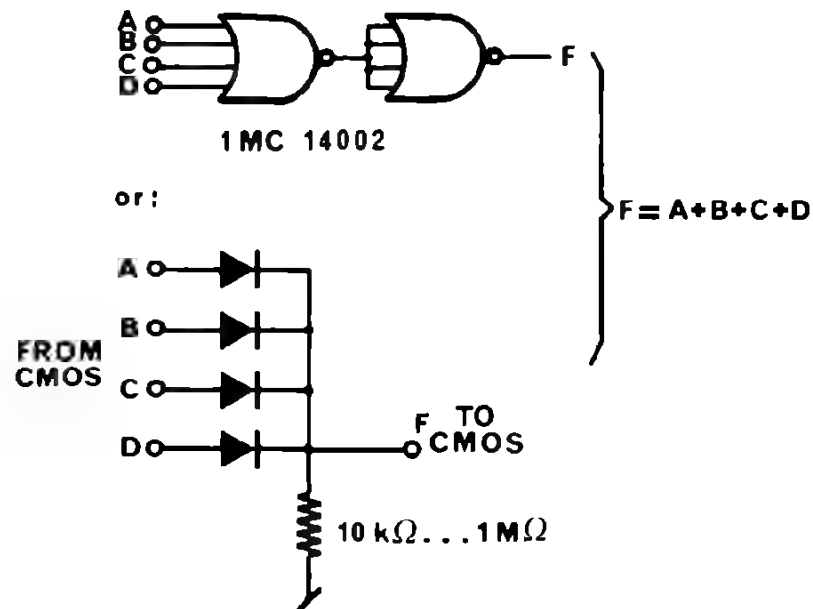
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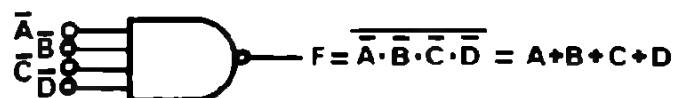
has to be chosen depending on switching speed requirements
if complements are available:



– 4 input OR

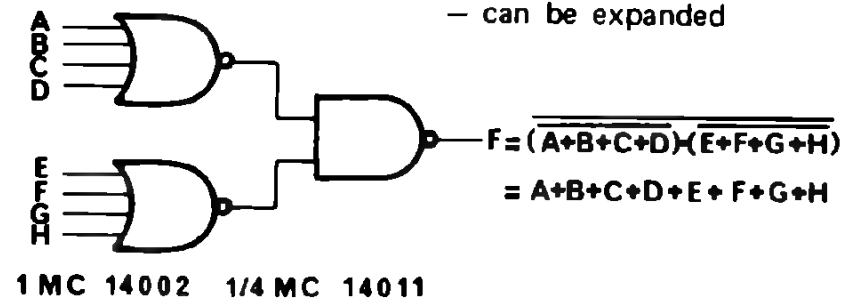


if complements are available:

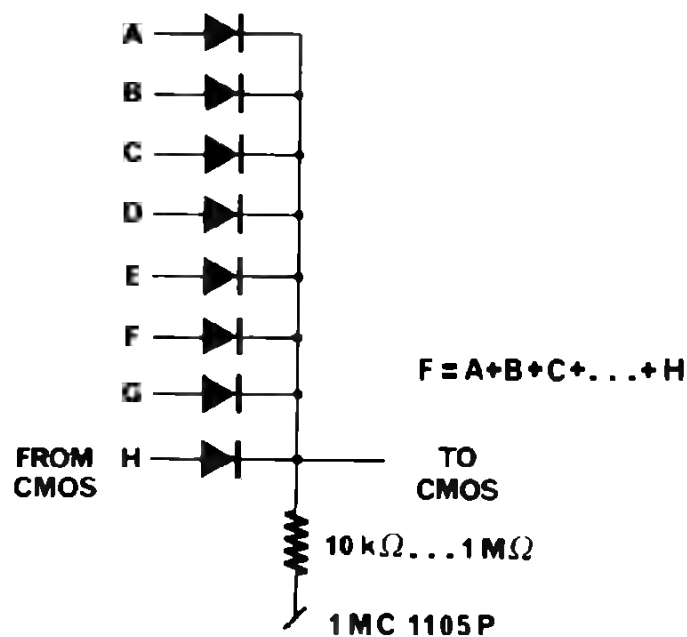


8 input OR

- most popular configuration
- can be expanded



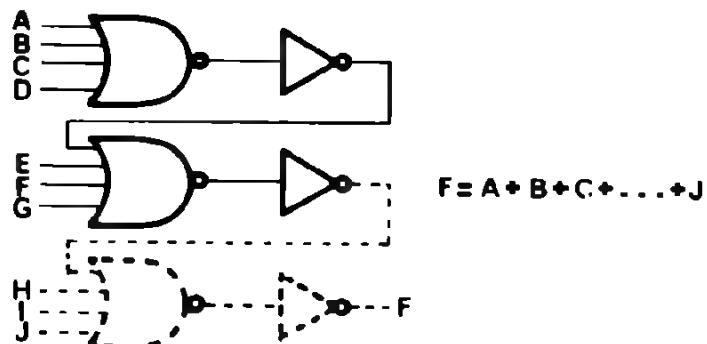
or:



complements are available:



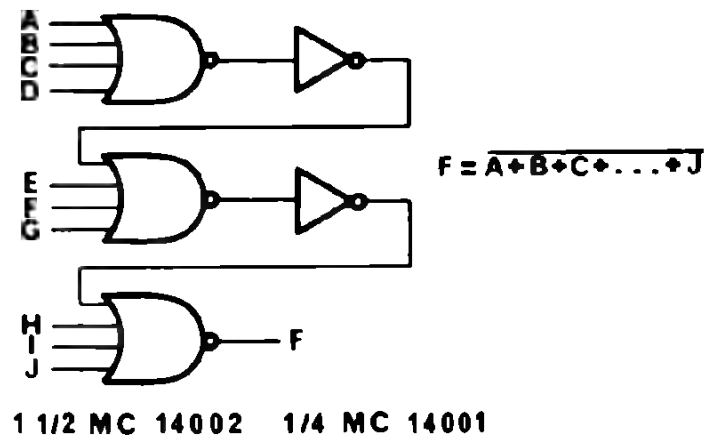
OR (more than 8 inputs)



4. 1. 2. NOR FUNCTION GENERATION

Examples:

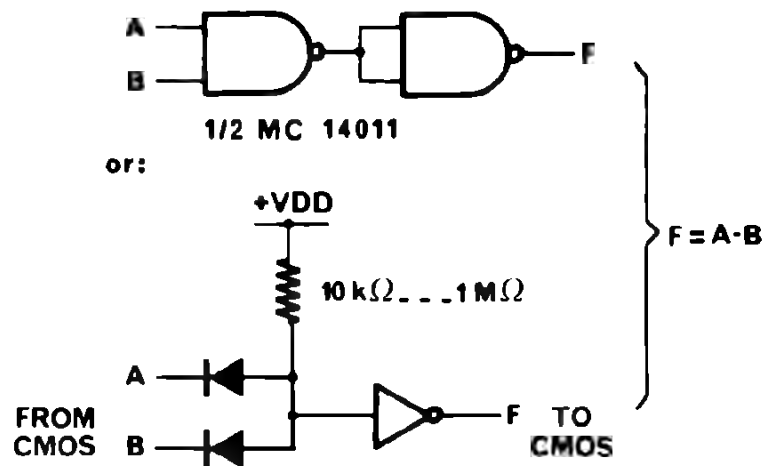
– NOR (more than 8 inputs)



4. 1. 3. AND FUNCTION GENERATION

Examples:

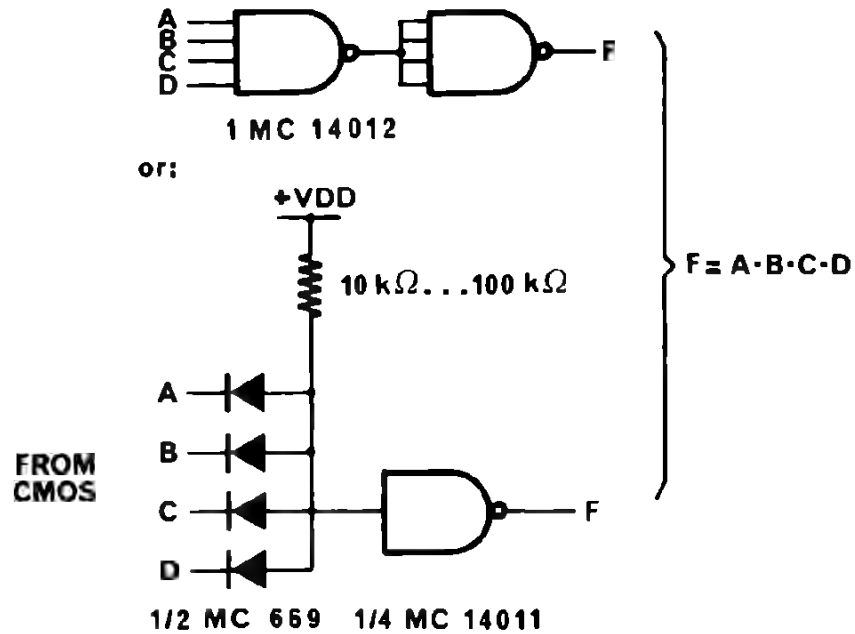
– 2 input AND



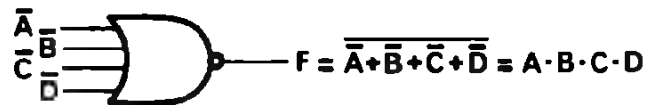
if complements are available:



– 4 input AND

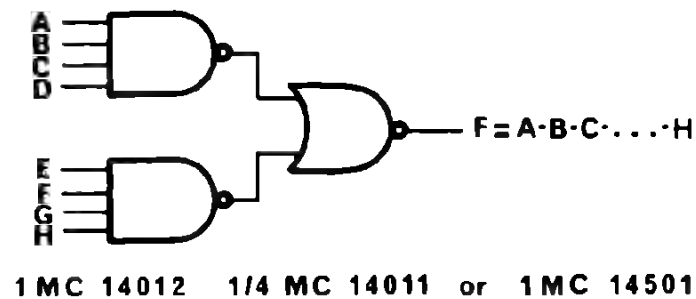


if complements are available:

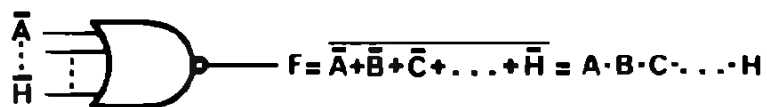


– 8 input AND

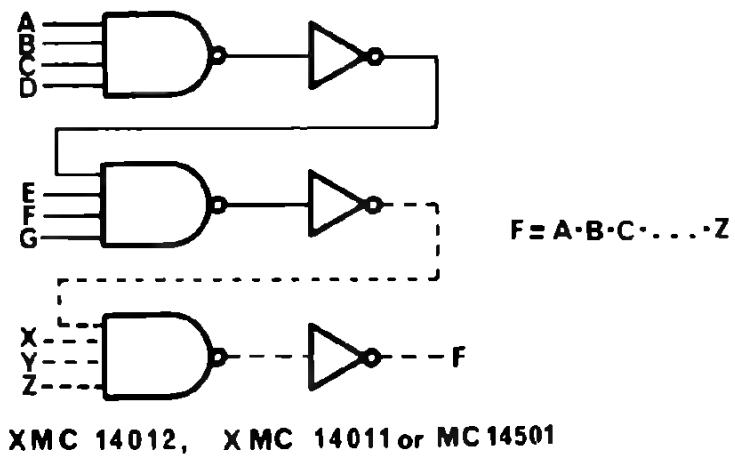
– most popular configuration
– can be expanded



if complements are available:

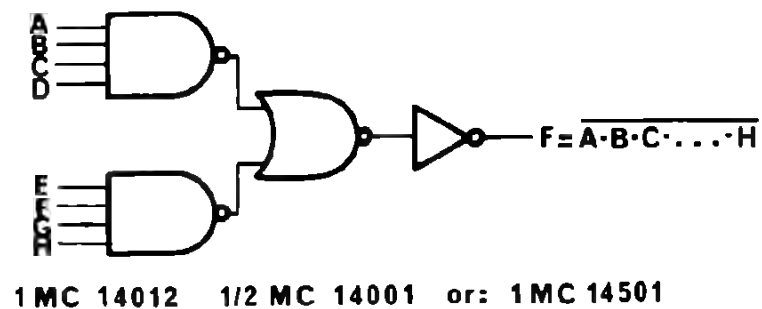


AND (more than 8 inputs)

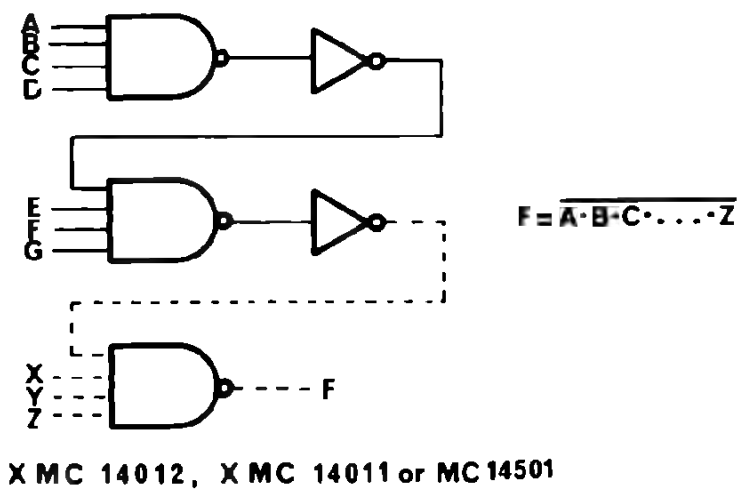


1. 4. NAND FUNCTION GENERATION

amples:
8 input NAND

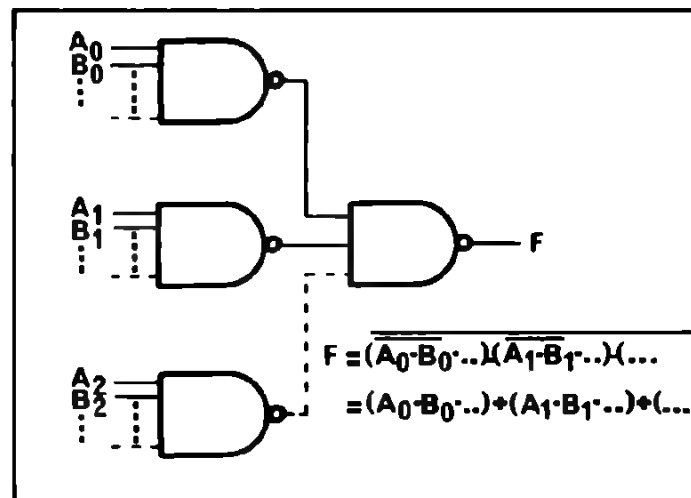


NAND (more than 8 inputs)



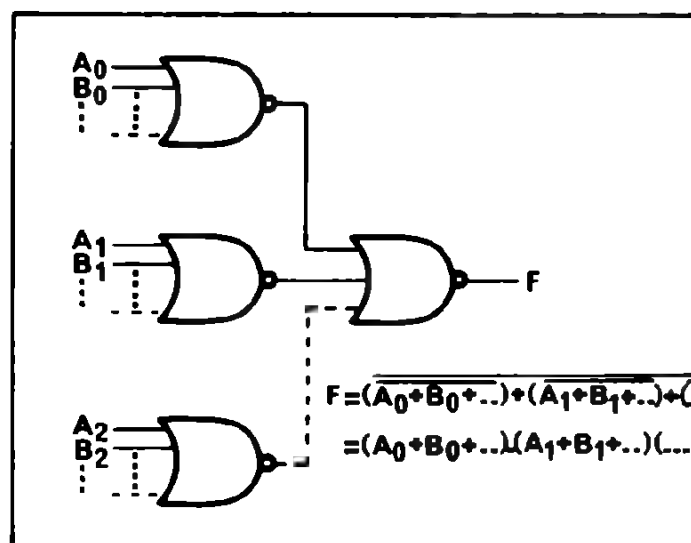
4. 1. 5. LOGICAL SUM OF PRODUCT

Example:
using only NAND gates.



4. 1. 6. LOGICAL PRODUCT OF SUMS

Example:
using only NOR gates

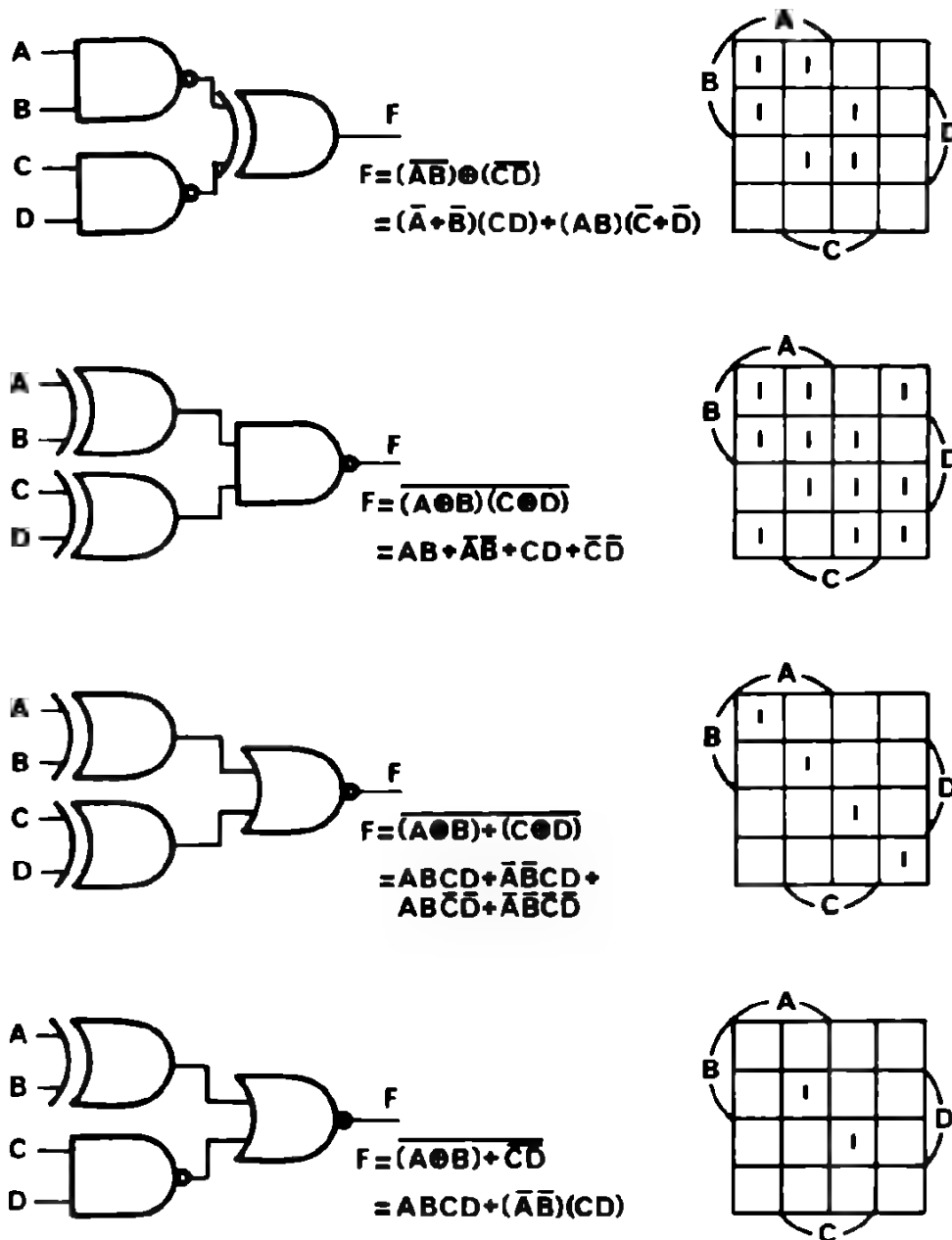


4. 1. 7. EXCLUSIVE "OR"

Besides the standard applications, such as adders and parity checkers, the usage of the exclusive OR function also allows in several cases a reduction of the number of logic modules in a system.

Below, a few examples showing how to solve logical equations with the use of exclusive OR gates, together with NAND and NOR gates are illustrated. The logic output equations and their representation in a Karnaugh map for 4 variables, are also represented.

Examples:



4. 1. 8. MULTIPLEXER USED TO SOLVE COMBINATORIAL EQUATIONS

In addition to the standard application of multiplexers in data conversion techniques, these circuits can also be used in generating logic functions, which in some cases reduces the package count.

In the CMOS families 3 multiplexer circuits for data routing applications should be mentioned:

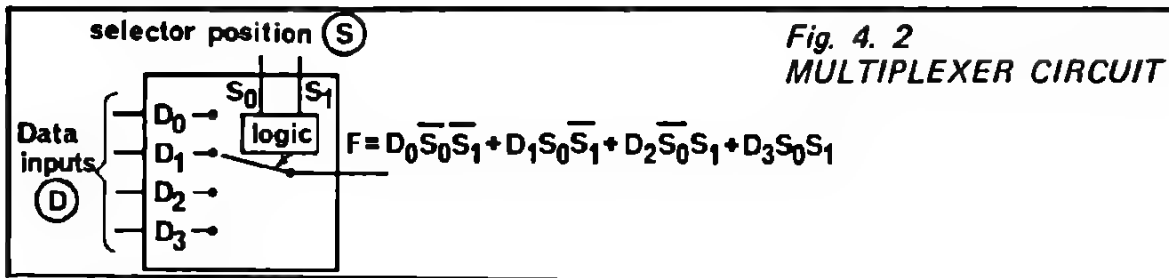
- A dual 4-channel data selector—MC 14539
- An 8 channel data selector—MC 14512
- and a quad 2-channel data selector—MC 14519

A multiplexer is a multiple position — single pole switch. One set of inputs selects the position of the switch. The second set of inputs collects the input data, which are transferred through the circuit to one output. The position of the switch is usually assigned by a binary code applied to the position selectors. Referring to Figure 4.2 the output equation in the case of a 4 channel multiplexer can be written:

$$F = D_0 \bar{S}_0 \bar{S}_1 + D_1 S_0 \bar{S}_1 + D_2 \bar{S}_0 S_1 + D_3 S_0 S_1$$

By using the selector inputs S and the data inputs D to which are connected the logic variables, it is possible to generate all the logic switching functions, at the output of the circuit.

On the selector inputs are connected N–1 logic variables, the remaining variable is always connected to the data input, shared value. The true or complement of this variable may be needed as well as some times "1" and "0" (N=number of logic variables).



Therefore:

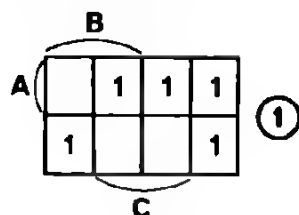
- a 4 channel multiplexer can handle 3 logic variables.
- a 8 channel " " " 4 logic variables.
- a 16 channel " " " 5 logic variables. etc.

First example:

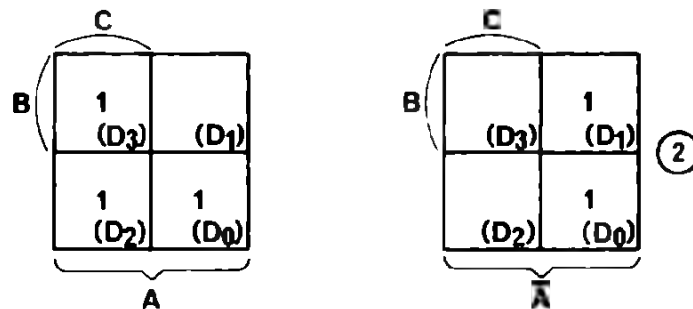
Solve the following logic equation:

$$F = A \bar{B} \bar{C} + \bar{A} \bar{B} \bar{C} + A B C + A \bar{B} C + \bar{A} B \bar{C}$$

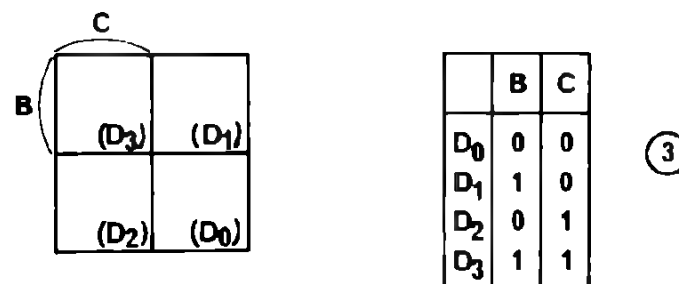
- on the Karnaugh map (3 variables), this function is represented as follows:



It is required to separate one logic variable from the function.
This may be done by splitting the above map into two maps of 2 variables.



Since there are 3 logic variables in the equations, it is required to use a 4 channel multiplexer. The variable B and C are connected to the selector inputs, the variable A to the data inputs. The position of the "selector", controlled by B and C, is represented by the Karnaugh map as:



By combining the tables (2) and (3) the data inputs become:

$$\begin{aligned} D_0 &= 1 \\ D_1 &= \bar{A} \\ D_2 &= A \\ D_3 &= A \end{aligned}$$

and the logic diagram of the 4 channel multiplexer becomes: (see Figure 4. 3.)

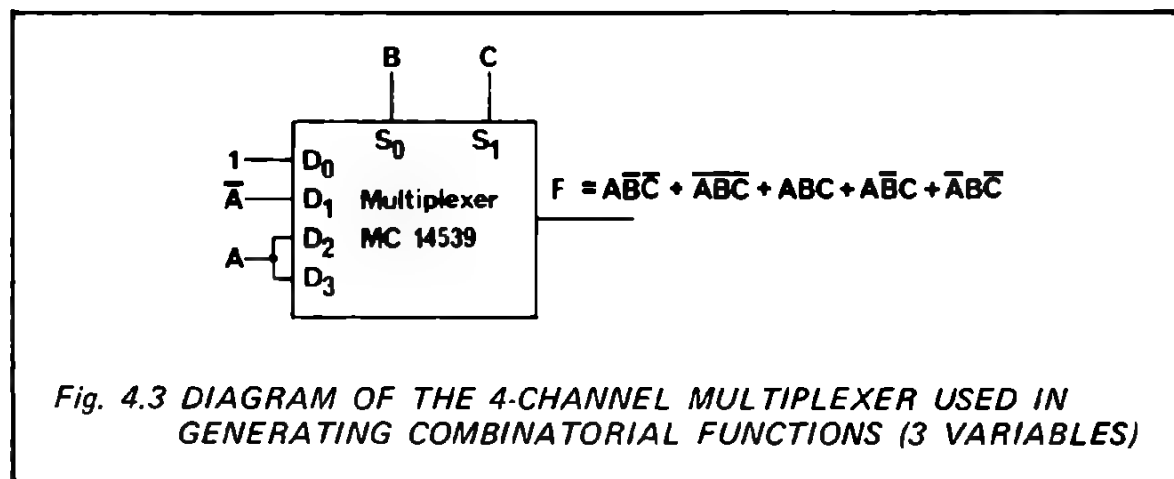
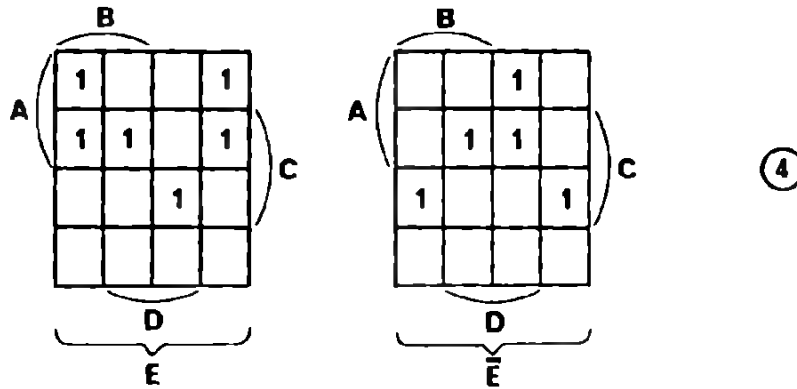


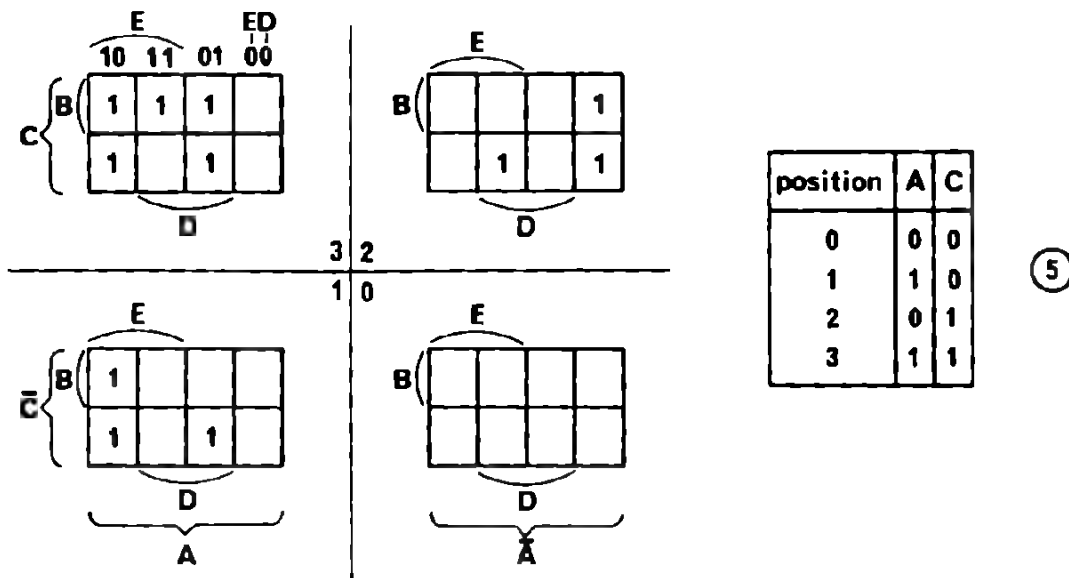
Fig. 4.3 DIAGRAM OF THE 4-CHANNEL MULTIPLEXER USED IN GENERATING COMBINATORIAL FUNCTIONS (3 VARIABLES)

Second example:

In this example it is assumed that a 5 variables logic equation is already reduced to the following Karnaugh map:



The above maps can be split into 4 maps of 3 variables each as follows:



Assuming that in this case 4 channel multiplexers are available, the variables D and E are then connected to the selector inputs of the first multiplexer level. The variables A and C are connected to the selector inputs of the second multiplexer level.

The variable B is connected to the data input of the first multiplexer. By proceeding as in the previous example and taking into account the maps (5) the logic circuit becomes (see Figure 4. 4.)

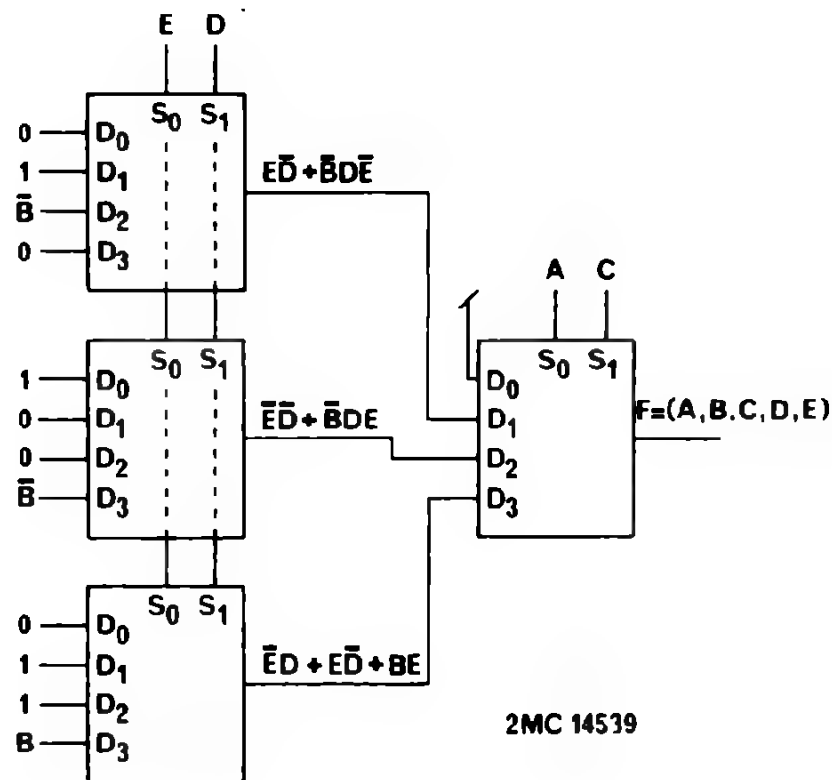


Fig. 4.4
DIAGRAM OF 4 MULTIPLEXERS USED IN GENERATING A
COMBINATORIAL FUNCTION (5 VARIABLES)

1. 1. 9. DECODER FUNCTIONS

Code converters, also called decoders, allow the translation of one logical word structure into another logical word structure, conserving the information content.

Decoder functions usually consist of combinatorial elements.

Since there exist numerous codes used throughout the industry, there are also numerous code converters. However, the most popular code converters in use are :

Binary to BCD and vice versa

Binary to Decimal and vice versa

BCD to Decimal and vice versa

Binary to octal and vice versa

BCD to 7 segments

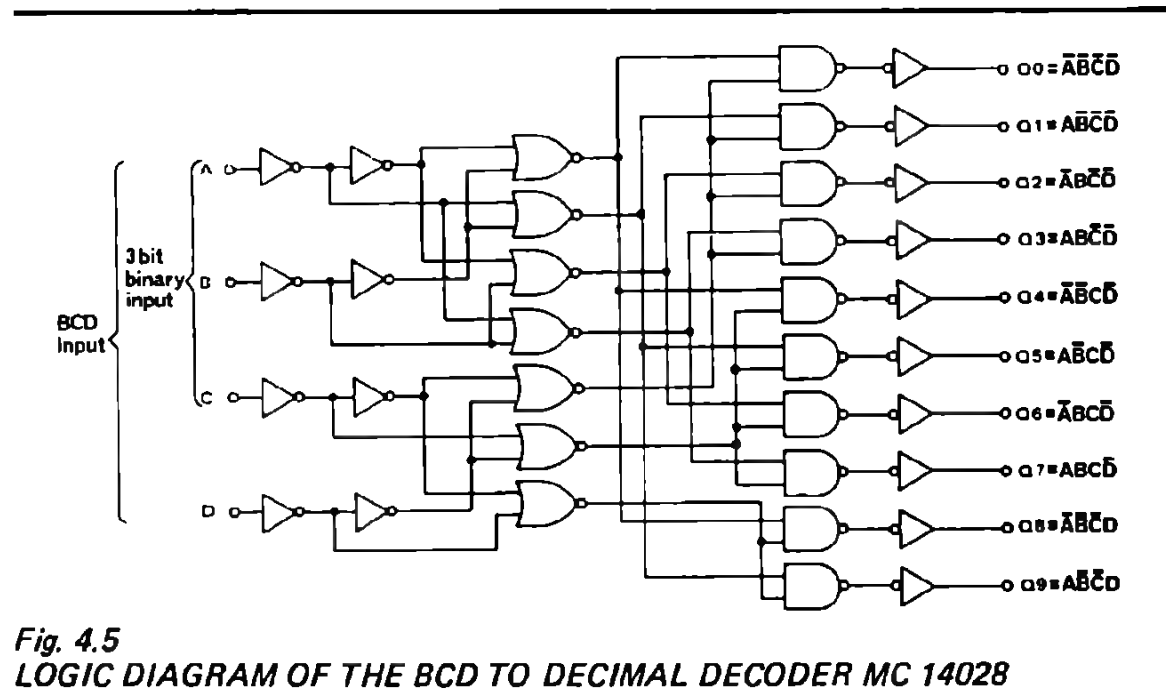
Various others are also found such as "Excess 3", ASCII code, GRAY code converters, etc.

In this section, the decoder functions available in the CMOS family will be briefly described. Further discussion may be found in the industrial Application section.

I. 1. 9. 1. BCD TO DECIMAL & BINARY TO OCTAL DECODER MC 14028

This decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0".

The logic diagram is represented in Figure 4.5.

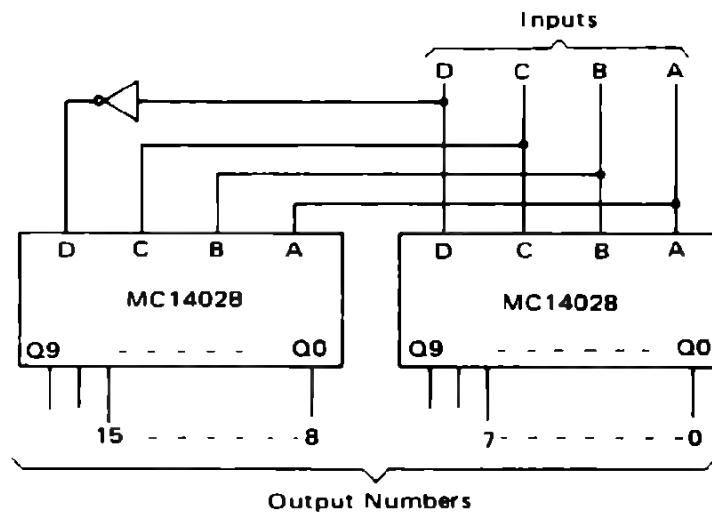


The truth table is :

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

This circuit finds its main application in decoding systems for numerical displays such as Nixie tube displays. It can also be efficiently used to expand decoding when required. The following 3 figures (4.6 - 4.7 - 4.8) show some examples of typical applications of the decoder circuit MC 14028.

Fig. 4.6
CODE CONVERSION
CIRCUIT



The truth table is :

INPUTS				OUTPUT NUMBERS																CODE AND REDEFINED OUTPUT NUMBERS						
																				Hexadecimal		Decimal				
																				4 Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221	
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4 Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0	
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2	
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3		
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4		
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3	4
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	4	3	1			
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2			
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5				
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5	
1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	10	12	7	9		6	
1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	11	13	8			5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6		
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7	
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8	
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9	

Fig. 4.7
SIX-BIT BINARY 1-OF-64 DECODER

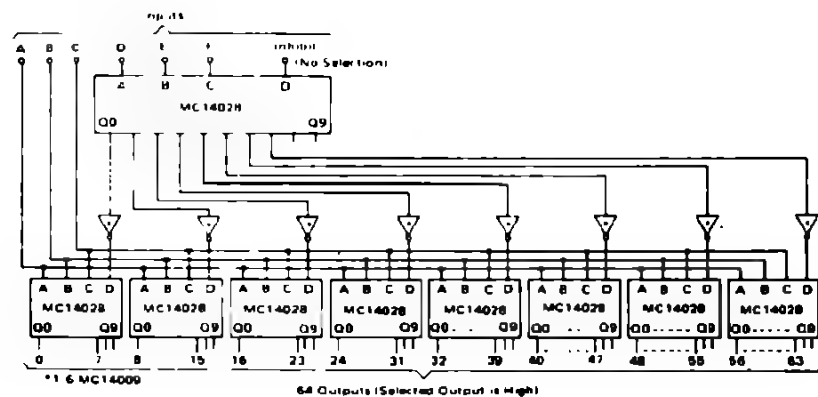
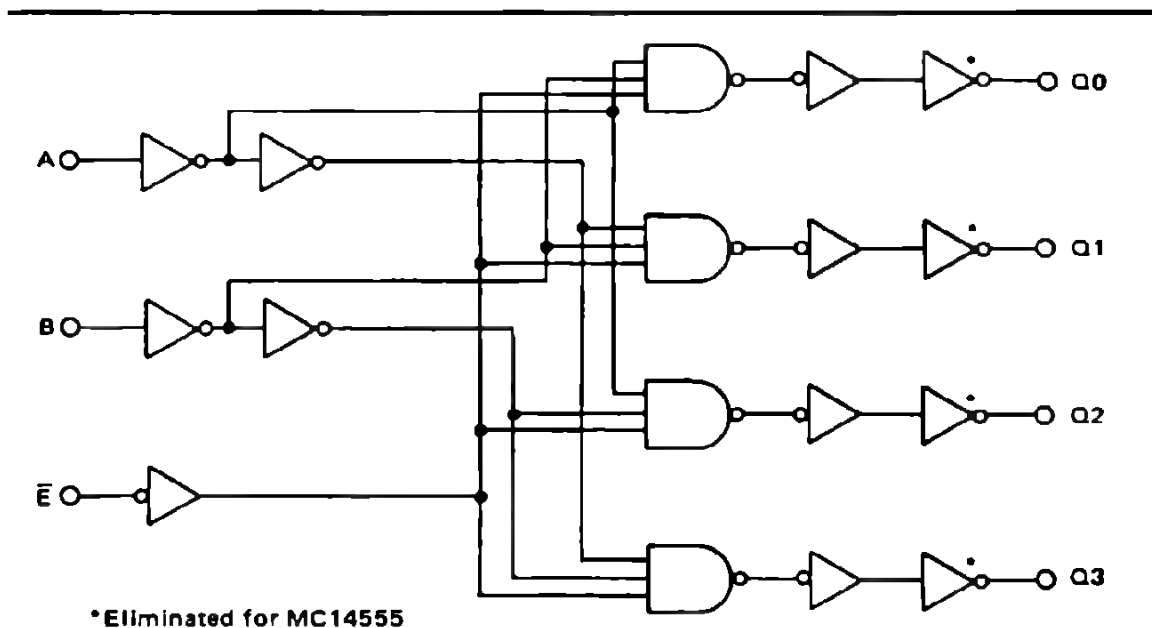


Fig. 4.8 DECIMAL DIGIT DISPLAY APPLICATION

**1. 9. 2. DUAL BINARY 1 OF 4 DECODER/DEMULTIPLEXER
MC 14555 - MC 14556**

This circuit is composed of two identical sections :
Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC 14555 (active high outputs) has a selected high state output and the MC 14556 (active low outputs) has a selected low state output.
The logic diagram represented by Figure 4.9 is valid for both type of circuits, however the device MC 14555 has only one output inverter.



**Fig. 4.9 LOGIC DIAGRAM OF THE DUAL BINARY 1 OF 4 DECODER
MC 14555 AND MC 14556**

he truth table for both devices is:

INPUTS			OUTPUTS				OUTPUTS			
ENABLE	SELECT		MC14555				MC14556			
\bar{E}	B	A	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X Don't Care

This circuit find its main application in code conversion, address decoding, and in demultiplexing circuit for data transmission systems. In this case, the enable input E is used as data input.

1. 1. 9. 3. BCD TO SEVEN SEGMENT LATCH DECODER DRIVER MC 14511

Specially developed to control 7 segments displays.

This circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to seven segment decoder, and an output drive capability. Lamp test (LT), blanking (B1), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The logic diagram is represented in Figure 4.10.

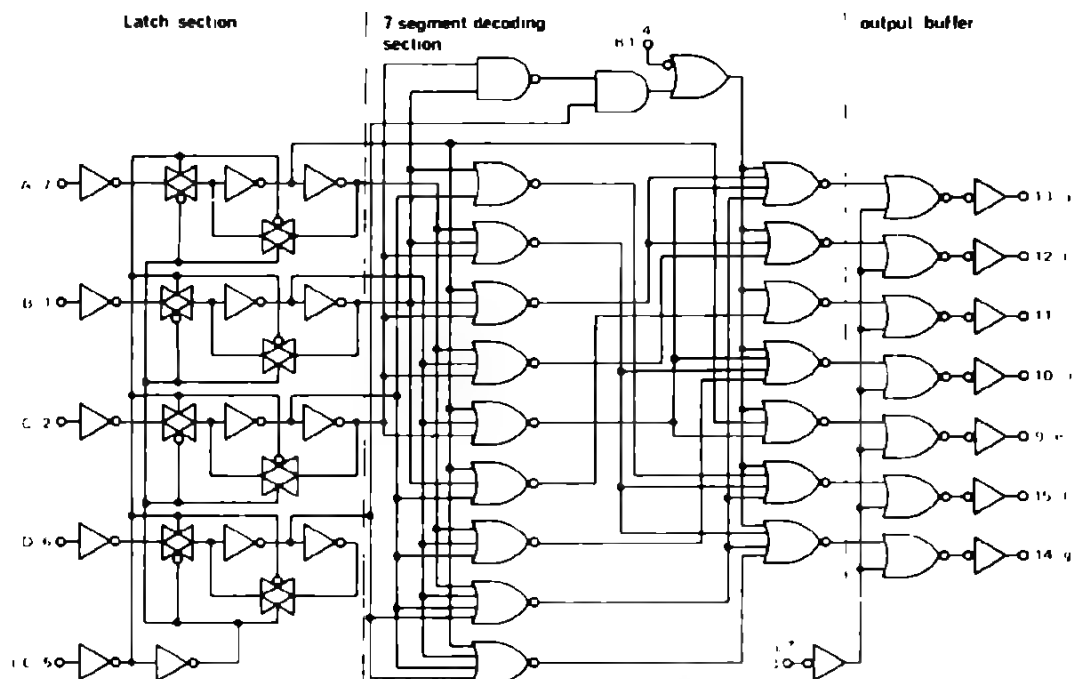


Fig. 4.10 LOGIC DIAGRAM OF THE BCD TO 7 SEGMENTS LATCH DECODER DRIVEN MC 14511

This circuit is composed of 3 main sections :

- The latch section composed of 4 CMOS gated latch flip-flops which stores the binary input data. The input is strobed by LE input.
- The 7 segments decoder section controlled by the blanking input $\overline{B1}$.
- The output buffers which are NPN bipolar transistors with high current sourcing capacity (25 mA). The \overline{LT} input allows to test all 7 segments.

The following truth table summarizes the operation of this device :

TRUTH TABLE

INPUTS							OUTPUTS						
LE	$\overline{B1}$	\overline{LT}	D	C	B	A	a	b	c	d	e	f	g
X	X	0	X	X	X	X	1	1	1	1	1	1	1
X	0	1	X	X	X	X	0	0	0	0	0	0	0
0	1	1	0	0	0	0	1	1	1	1	1	1	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0
0	1	1	0	0	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	1	1	1	1	0	0	1
0	1	1	0	1	0	0	0	1	1	0	0	1	1
0	1	1	0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	1	0	0	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1	1	1	1
0	1	1	1	0	0	1	1	1	1	0	0	1	1
0	1	1	1	0	1	0	0	0	1	1	1	1	1
0	1	1	1	0	1	1	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	1	0	0	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0	0	0	0
1	1	1	X	X	X	X	Latch						

X = Don't care

* Depends upon the BCD code applied during the 0 to 1 transition of LE.

DISPLAY

0	1	2	3	4	5	6	7	8	9
---	---	---	---	---	---	---	---	---	---



V_{DD} = Pin 16

V_{SS} = Pin 8

The application of this circuit is mainly in the instrumentation field, such as counter, D.V.M. and general numerical display control (7 segments).

Figure 4.11 indicates the connection mode to various displays readouts, like LED's, incandescent lamps, fluorescent lamps, gas discharge tubes, or liquid crystal readouts.

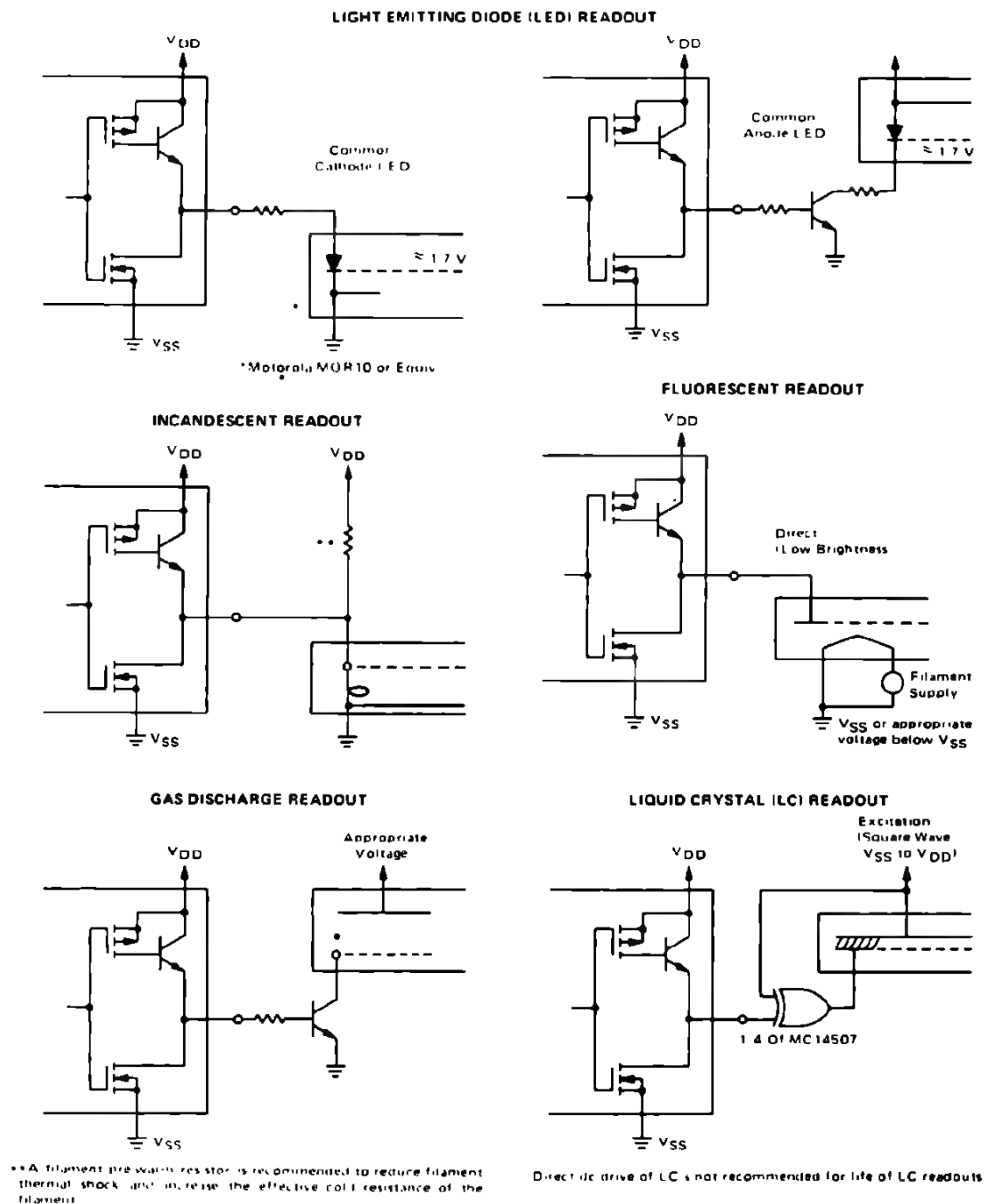


Fig. 4.11 CONNECTIONS TO VARIOUS DISPLAY READOUTS

2. SEQUENTIAL LOGIC FUNCTIONS

A sequential circuit is a network in which the output status is related to the previous input status, which has been memorized, as well as to the present input conditions. Flip-flops, shift registers, counters are all sequential circuits.

In this section, we will first describe the standard CMOS flip-flops with some typical applications, then we consider the latches and shift registers, and finally the counters and timers will be analyzed.

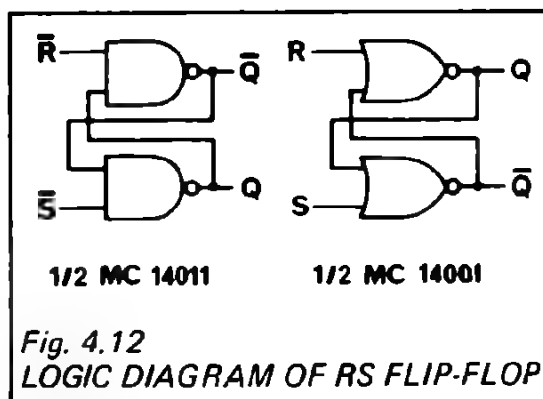
4. 2. 1. FLIP-FLOPS

4. 2. 1. 1. Standard flip-flop configurations

RS FLIP-FLOP (RESET AND SET F.F.)

The simplest flip-flop uses only two cross coupled NOR or NAND gates. It memorizes any logic state applied to either of the inputs, R or S.

The logic diagrams are represented in Figure 4.12 which shows two types of flip-flop, one using NOR gates, the other NAND gates.



Truth tables becomes for:

NOR GATES				NAND GATES			
R	S	Q	\bar{Q}	\bar{R}	\bar{S}	Q	\bar{Q}
0	0	Q	\bar{Q}	0	0	1(U)	1(U)
1	0	0	1	1	0	1	0
0	1	1	0	0	1	0	1
1	1	0(U)	0(U)	1	1	Q	\bar{Q}

U = Undetermined

It should be noted that: with NOR gate, the information remains memorized by $R=S=0$; with NAND gates, the information remains memorized by $\bar{R}=\bar{S}=1$.

GATED RS FLIP-FLOP

Additional gates to the R and S inputs of a RS flip-flop form a gated RS flip-flop. This flip-flop allows the memorization of a logic input state, only when required, by controlling the input gates. Figure 4.13 represents the logic diagram of a gated RS flip-flop which uses NOR gates.

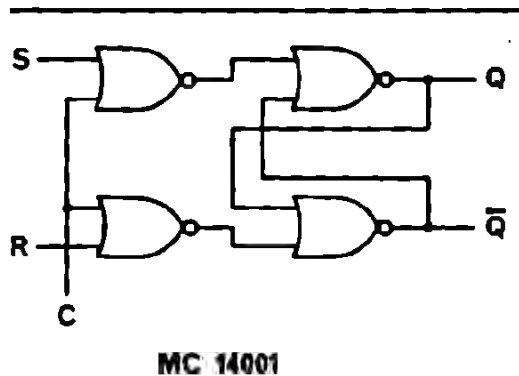


Fig. 4.13
GATED RS FLIP-FLOPS USING
NOR GATES

The truth tables becomes:

C	R	S	Q	\bar{Q}
0	0	0	0(U)	0(U)
0	1	0	0	1
0	0	1	1	0
0	1	1	Q	\bar{Q}
1	X	X	Q	\bar{Q}

X = don't care

The logic diagram of a CMOS gated flip-flop is presented in Figure 4.14. This configuration uses the transmission gate in conjunction with the NOR gate, and represents the basic CMOS circuit used in the master/slave flip-flops and in many latches and registers. The use of the transmission gate requires that both the clock function and its complement be available on the chip.

When the clock is low, the transmission gate TG1 is "on"

• TG2 is "off" and Q follows the complement of the input \bar{D} .

When the clock is high, the transmission gate TG1 is "off"

• TG2 is "on" and the information is memorized.

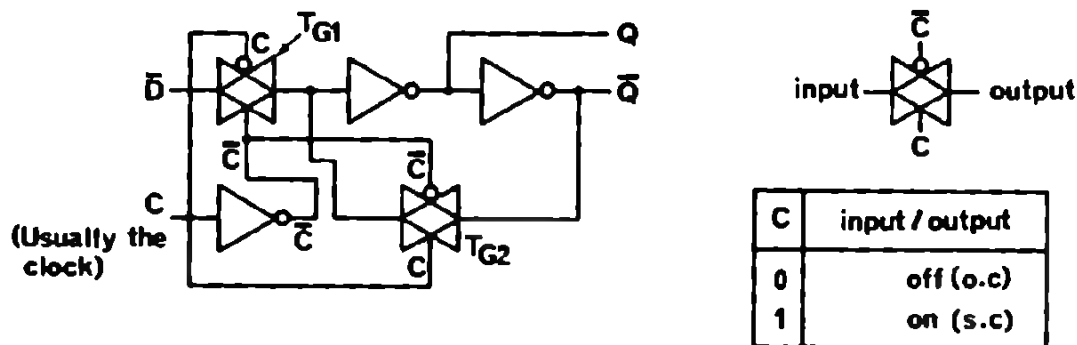


Fig. 4.14 BASIC LOGIC DIAGRAM OF A CMOS GATED FLIP-FLOP USED IN MASTER SLAVE FLIP-FLOP

C	\bar{D}	TG1	TG2	Q	\bar{Q}
0	0	on	off	1	0
0	1	on	off	0	1
1	X	off	on	Q	\bar{Q}

X = don't care

The truth table summarizes the operation of the CMOS gated flip-flop.

This type of flip-flop is also called a "D" latch flip-flop.

D" MASTER-SLAVE FLIP-FLOP MC 14013

The cascading of two CMOS gated flip-flops forms a master-slave "D" flip-flop structure, which is useful in applications such as shift registers or counters.

In principle, the "data" applied to the "D" input is delayed before appearing at the output by one clock cycle (hence the "D" meaning delayed).

The logic diagram of the D flip-flop ($1/2$ MC 14013) is represented in Figure 4.15.

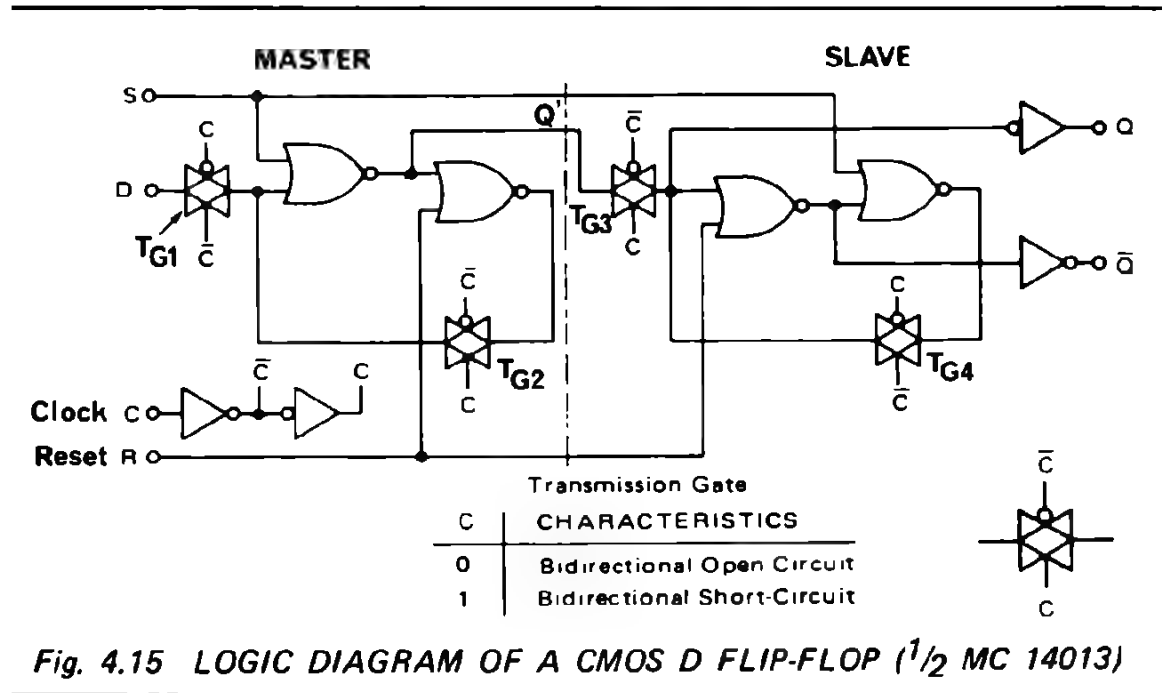


Fig. 4.15 LOGIC DIAGRAM OF A CMOS D FLIP-FLOP ($1/2$ MC 14013)

The operation of this flip-flop is best explained by studying the transmission gates.

When the clock input is low, the transmission gates are in the following states:

- TG1 → on
- TG2 → off
- TG3 → off
- TG4 → on

This means that the output Q' of the master always adopts the complement of the 'D' input.

The output Q of the slave remains memorized and therefore unchanged.




When the clock input goes high, the transmission gates are then in the following states:

- TG1 → off
- TG2 → on
- TG3 → on
- TG4 → off

The result is that the master (Q') memorizes the complement of the "D" input which is thus directly applied to the slave output (Q). In other words the data input "D" value is transferred to the Q output on the positive transition of the clock.

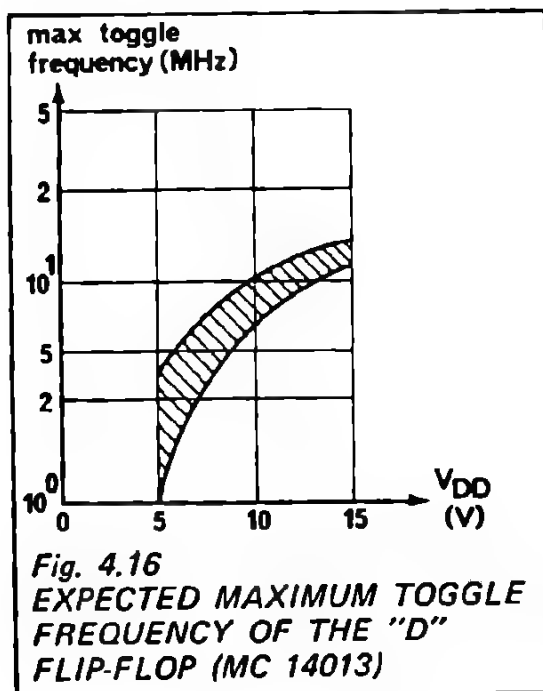
This flip-flop has also direct set and reset features for operation in asynchronous mode.

The truth table of the "D" flip-flop is:

		INPUTS				OUTPUTS	
		CLOCK	DATA	RESET	SET	Q	\bar{Q}
Synchronous mode	}		0	0	0	0	1
			1	0	0	1	0
			X	0	0	Q	\bar{Q}
Asynchronous mode	}	X	X	1	0	0	1
		X	X	0	1	1	0
		X	X	1	1	.	.

X = Don't Care
• = Invalid Condition

No Change



Apart from the well known features of the CMOS flip-flops, some additional parameters such as maximum operation frequency and maximum clock transition time to assure a proper operation of the flip-flop are important.

Figure 4.16 indicates the maximum toggle frequency as a function of the supply voltage V_{DD} .

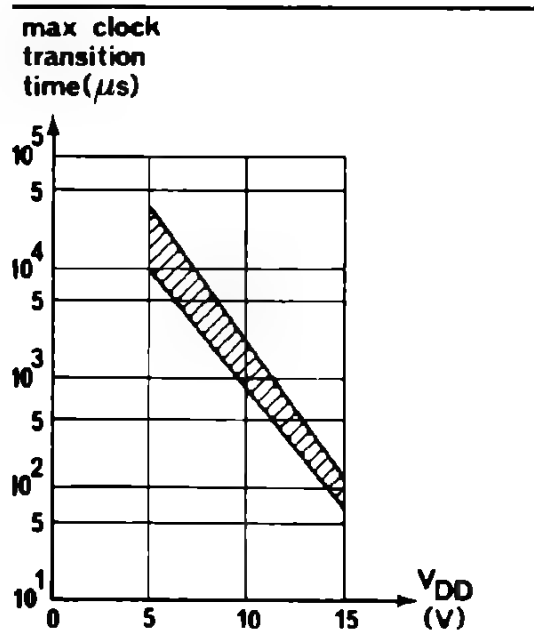


Figure 4.17 shows the maximum clock transition time which assures proper operation of the flip-flop as a function of the supply voltage, for V_{DD} equal to 5, 10, 15V. This information is particularly useful when the clock signal is generated directly by a circuit without any shaping network.

Fig. 4.17
EXPECTED MAXIMUM CLOCK
TRANSITION TIME REQUIRED
BY "D" FLIP-FLOP (MC14013)
AS A FUNCTION OF V_{DD}

J.K. MASTER-SLAVE FLIP-FLOP MC 14027

In principle, the J.K. flip-flop is a modified "D" master-slave flip-flop. It also is composed of two cascaded CMOS "gated flip-flops", with the difference that the "D" input is expanded by additional gates to form two inputs, called J and K. This circuit is very useful in sequential logic applications such as counters, as well as in control logic.

The logic diagram of the J.K. flip-flop ($1/2$ MC 14027) is shown in Figure 4.18.

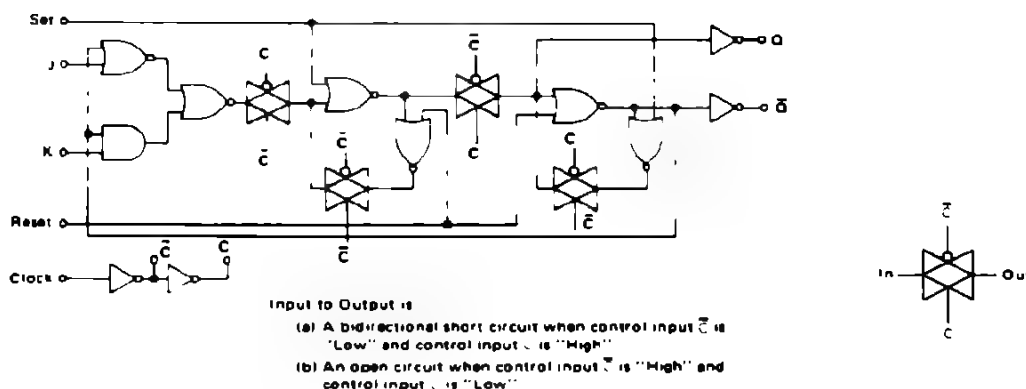


Fig. 4.18 LOGIC DIAGRAM OF A CMOS J.K. FLIP-FLOP ($1/2$ MC 14027)

The operation of the master-slave J.K. flip-flop is very similar to the "D" flip-flop. Dependant on the J.K. input state, the data is first transferred to the master while the clock is in the low state. The content of the slave remains memorized. When the clock is in the high state the content of the master remains memorized and its value is transferred to the slave. This flip-flop has also direct set and reset inputs for the asynchronous operative mode.

Considering both the J and K inputs, the truth table is :

TRUTH TABLE

Synchronous mode				Asynchronous mode			
J	K	Q_n	Q_{n+1}	R	S	Q	\bar{Q}
0	0	Q_n	Q_n	1	0	0	1
1	0	0	1	0	1	1	0
1	0	1	1	1	1	1	1
0	1	0	0				
0	1	1	0				
1	1	0	1				
1	1	1	0				

It should be noticed that, when $J = K = 1$,

the next state of Q (i.e. Q_{n+1}) is always complemented so that

if $Q_n = 0 \rightarrow Q_{n+1} = 1$

if $Q_n = 1 \rightarrow Q_{n+1} = 0$

This introduces immediately the operation of dividing-by-two, in the synchronous mode. J.K. flip-flops with the J and K inputs connected to "1" are also called toggle flip-flops.

The Figure 4.19 indicates the maximum toggle frequency for the J.K. flip-flops as a function of V_{DD} .

Figure 4.20 indicates the maximum clock transition time to ensure proper operation of the J.K. flip-flop.

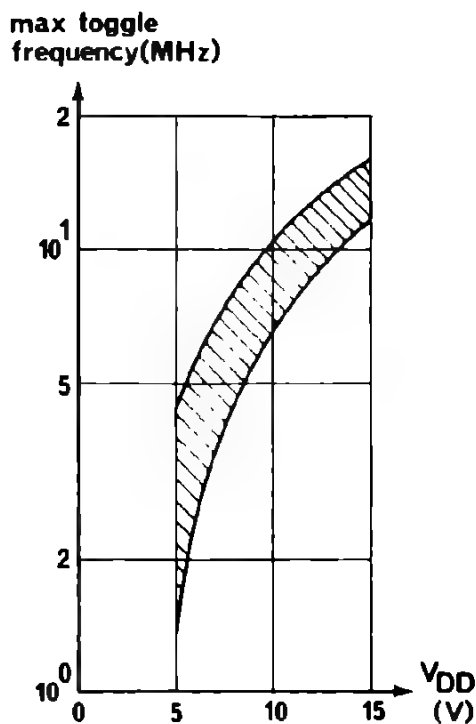


Fig. 4.19
EXPECTED MAXIMUM TOGGLE
FREQUENCY RANGE OF CMOS
J.K FLIP-FLOP (MC 14027) AS A
FUNCTION OF V_{DD}

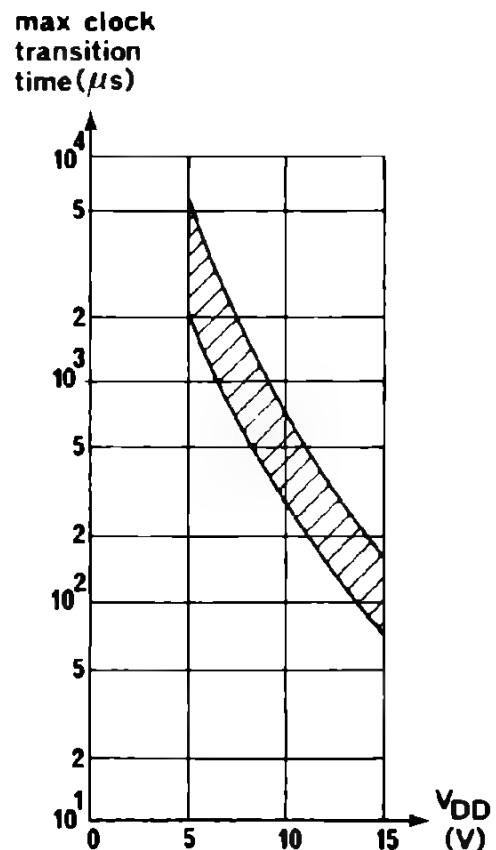


Fig. 4.20
EXPECTED LONGEST CLOCK
TRANSITION TIME REQUIRED
BY FLIP-FLOP (MC 14027)

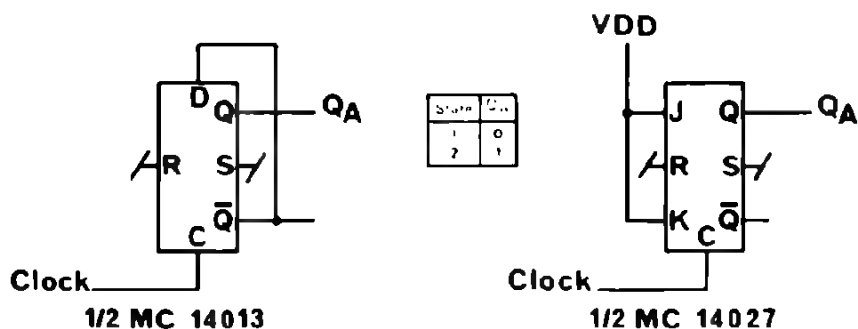
2. 1. 2. Flip-flop applications

ainly used in sequential systems, the D and J.K. flip-flops find their principal application in synchronous and asynchronous up, down, and up/down counters. The following schematics show some typical examples : of course for more complicated counters complex functions can be used.

YNCHRONOUS UP COUNTER

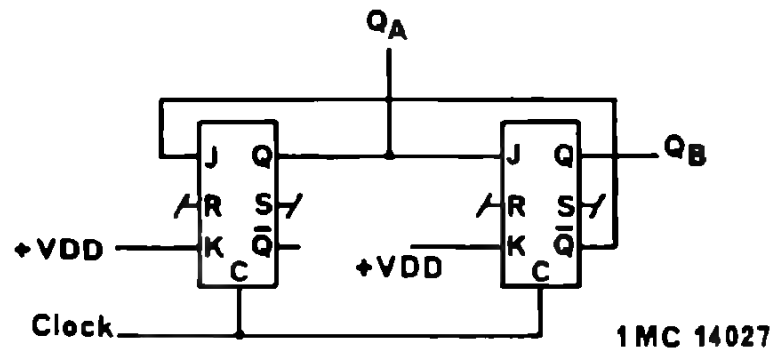
Example :

Divide by 2 Up counter



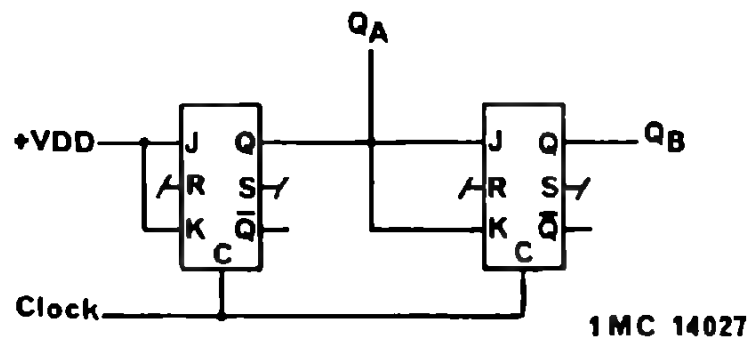
Divide by 3 Up counter

State	Q _A	Q _B
1	0	0
2	1	0
3	0	1



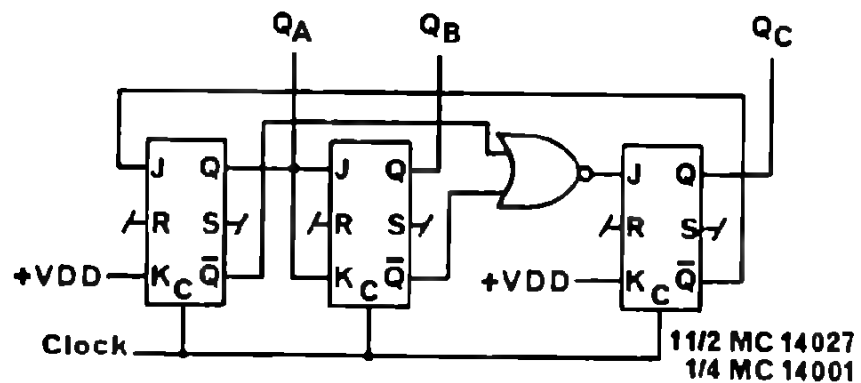
Divide by 4 Up counter

State	Q _A	Q _B
1	0	0
2	1	0
3	0	1
4	1	1

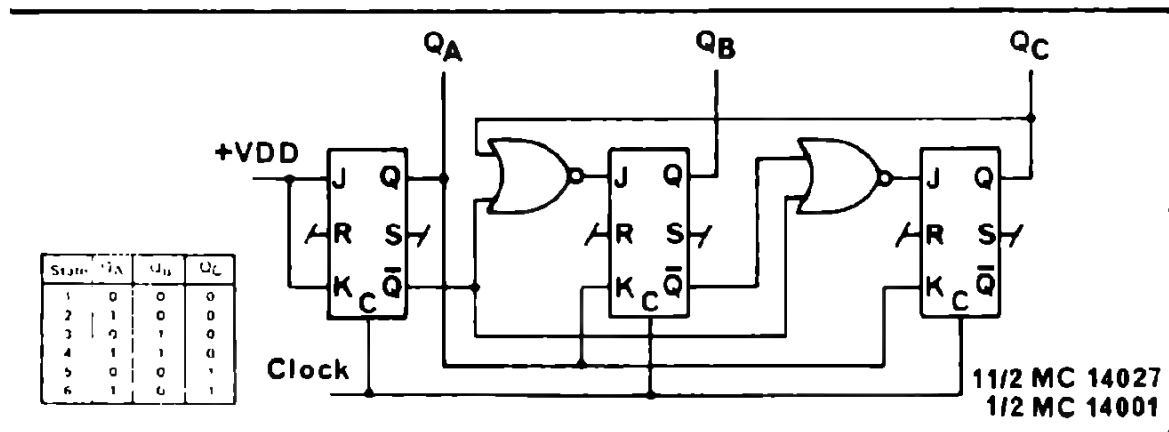


Divide by 5 Up counter

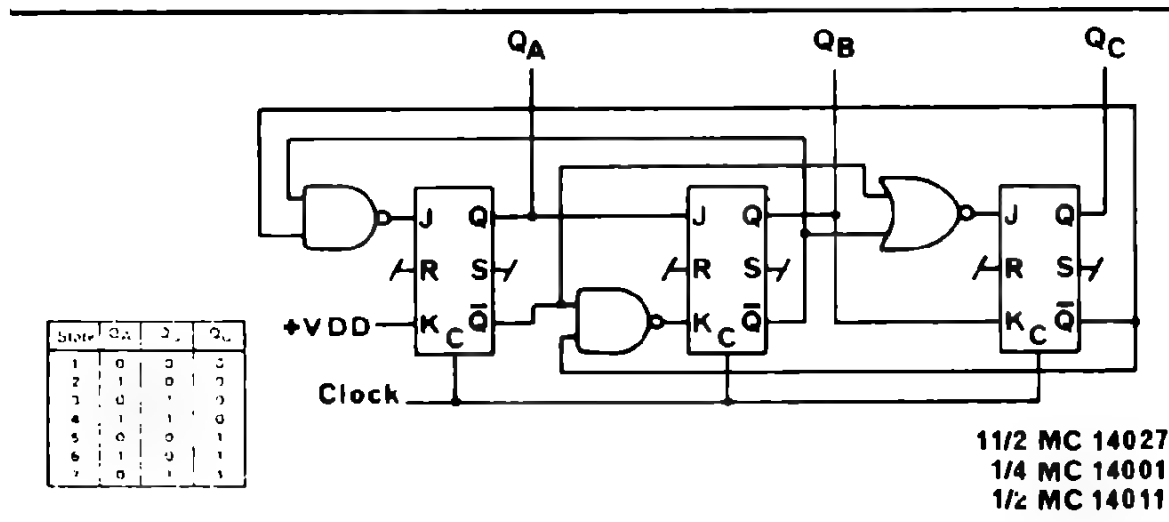
State	Q _A	Q _B	Q _C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1



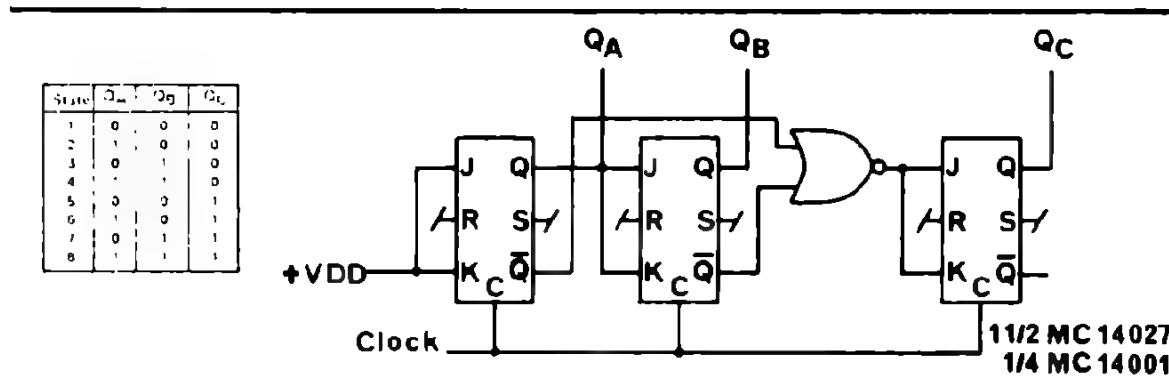
– Divide by 6 Up counter



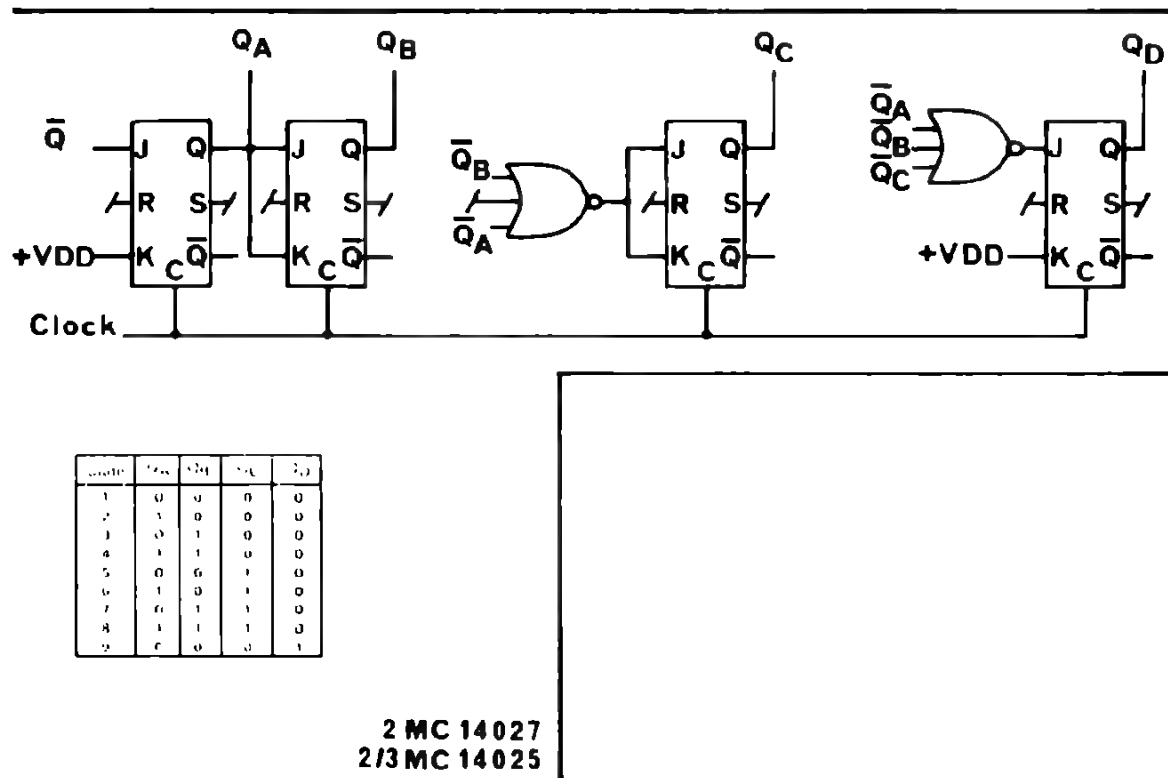
– Divide by 7 Up counter



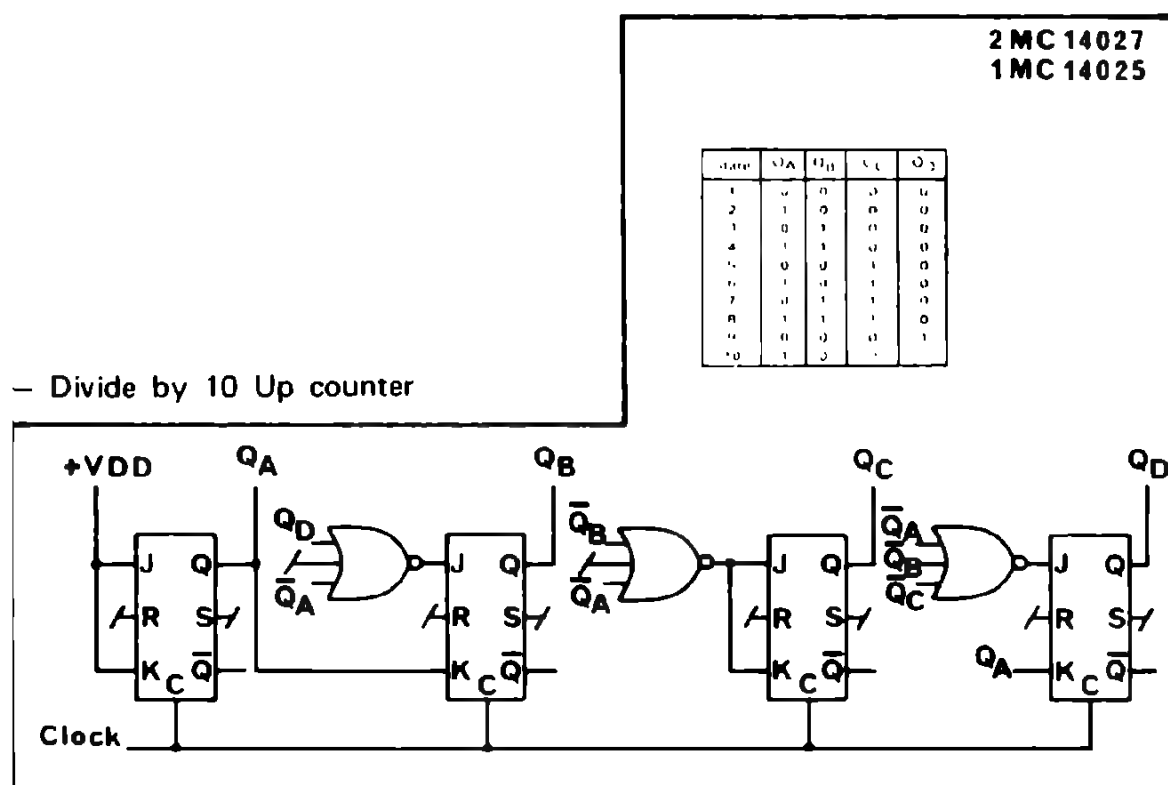
– Divide by 8 Up counter



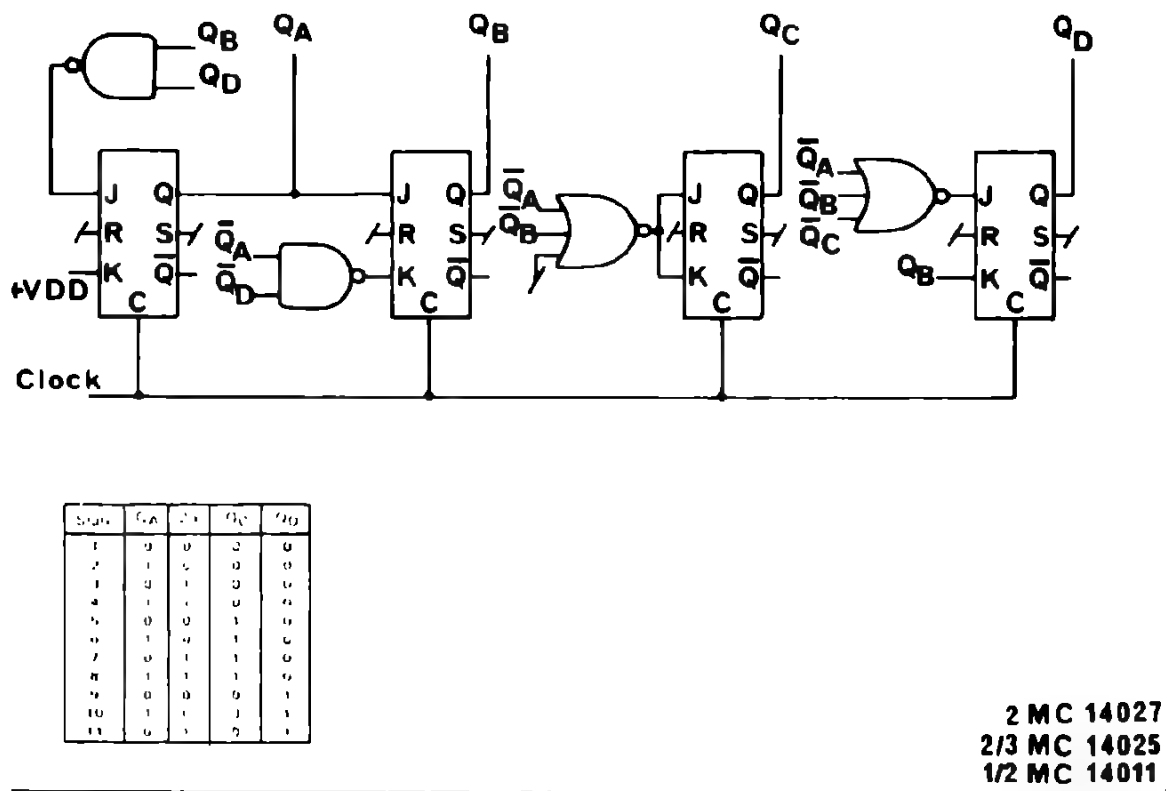
- Divide by 9 Up counter



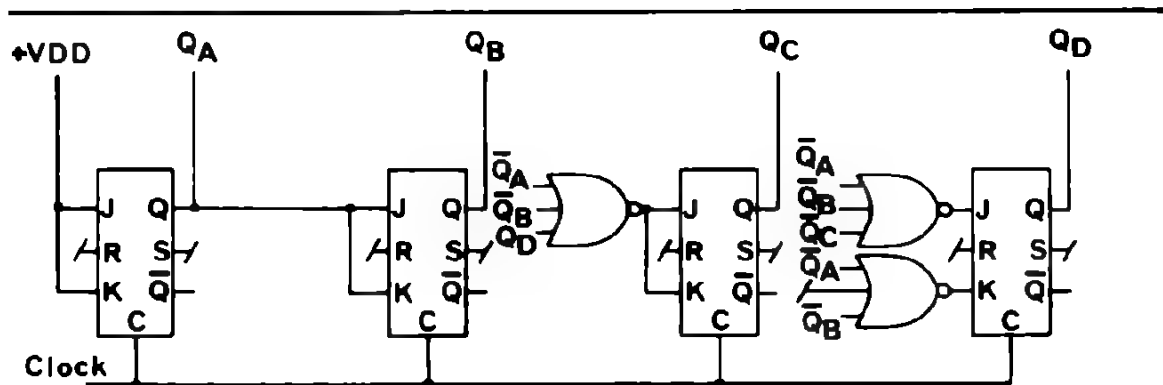
- Divide by 10 Up counter



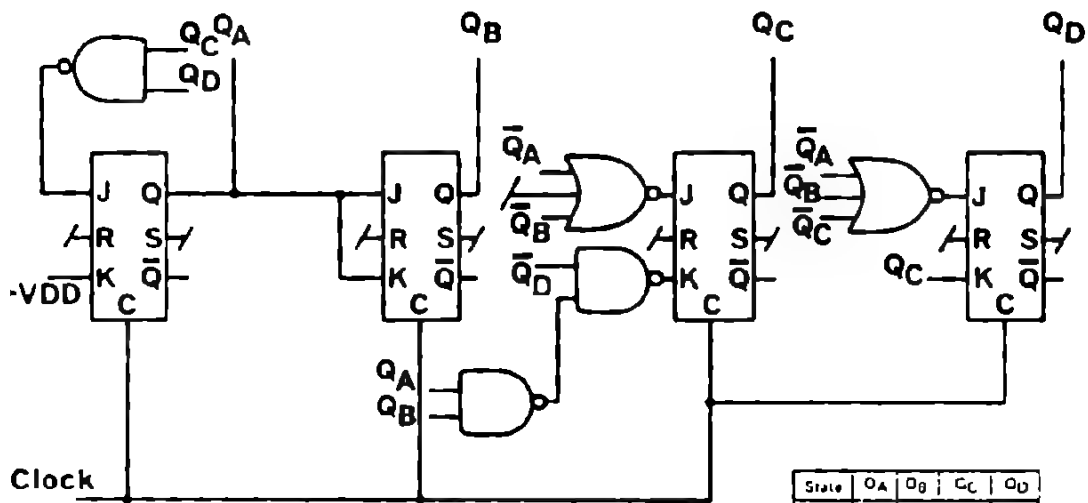
– Divide by 11 Up counter



– Divide by 12 Up counter



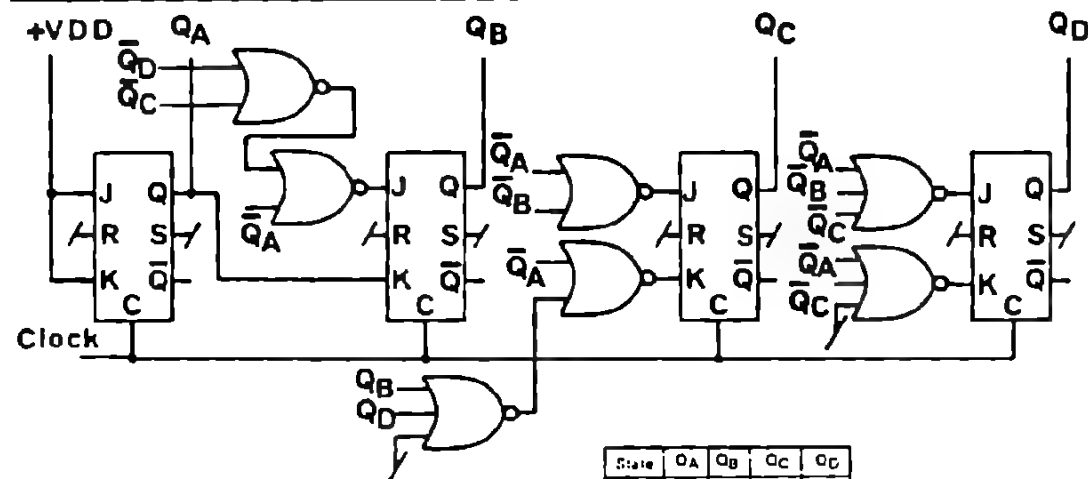
- Divide by 13 Up counter



State	QA	QB	QC	QD
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	0	1

2 MC 14027
2/3 MC 14025
3/4 MC 14011

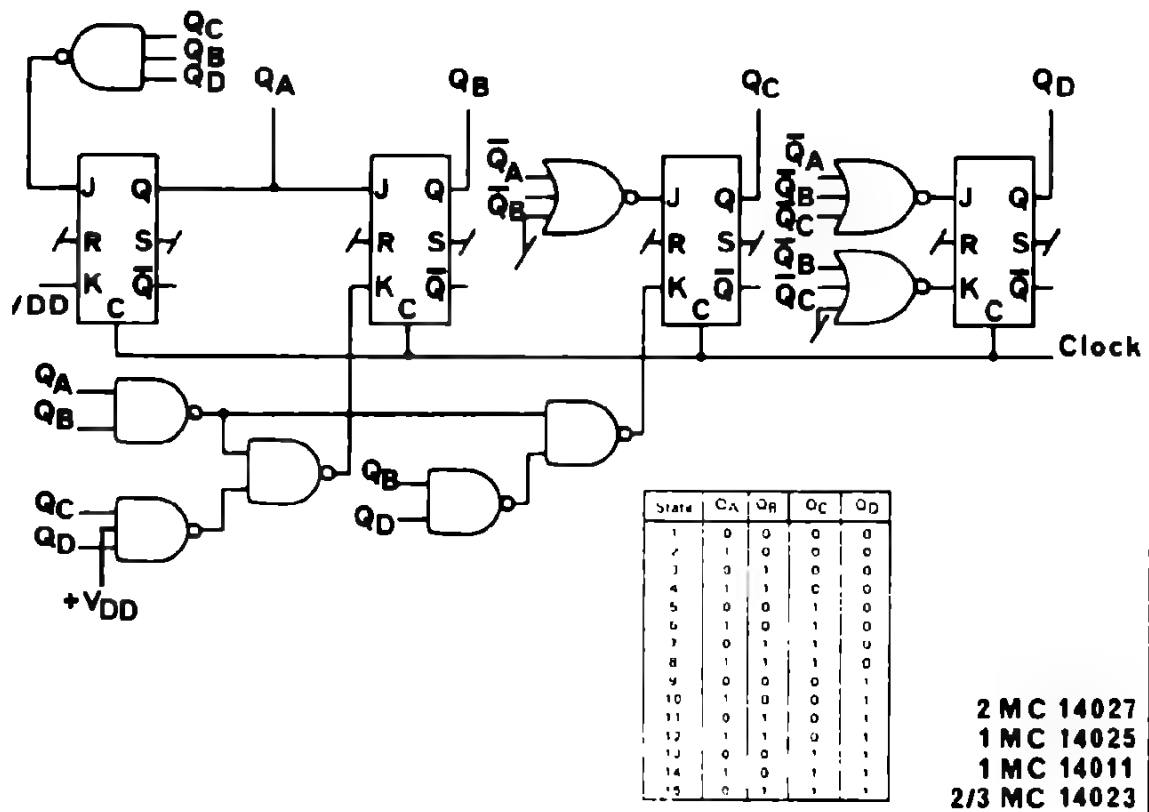
- Divide by 14 Up counter



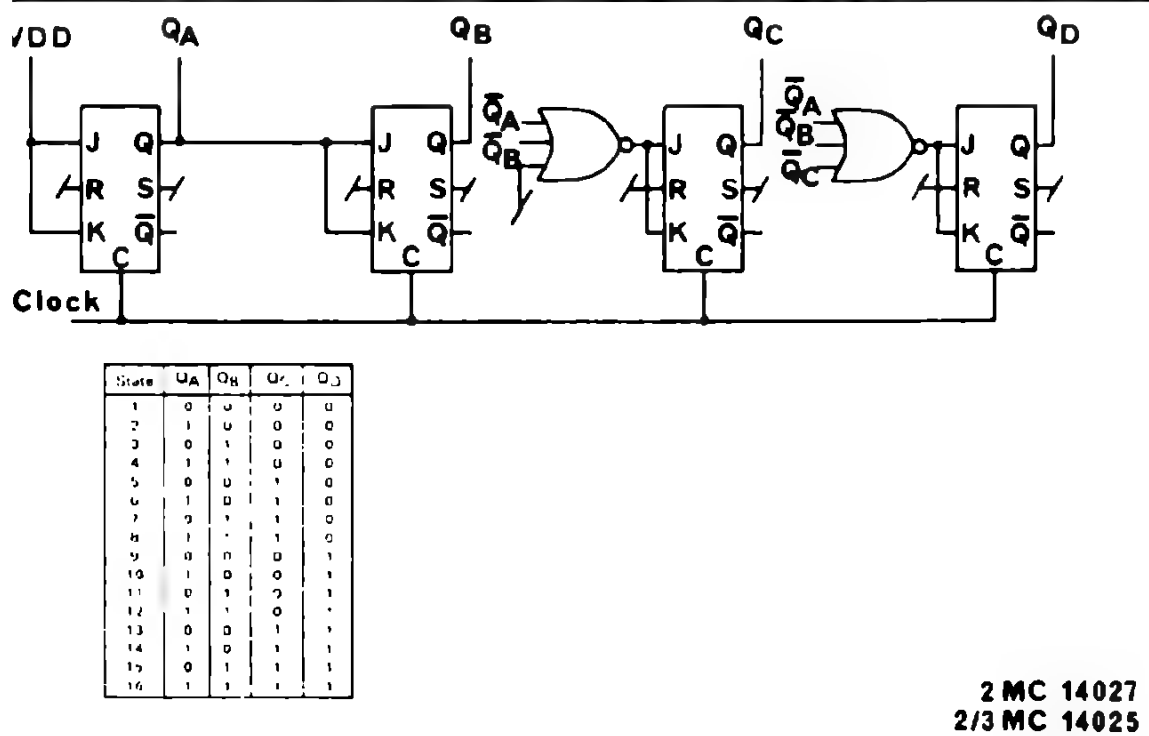
State	QA	QB	QC	QD
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1

2 MC 14027
1 MC 14025
1 MC 14001

Divide by 15 Up counter

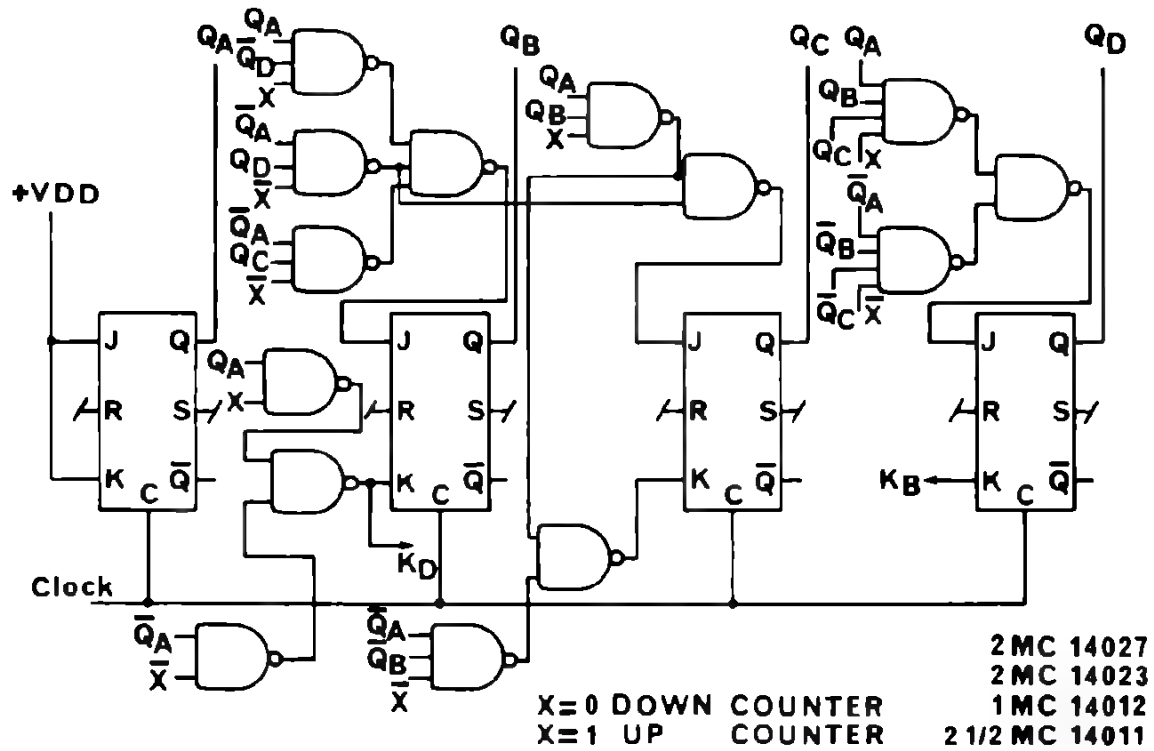


Divide by 16 Up counter

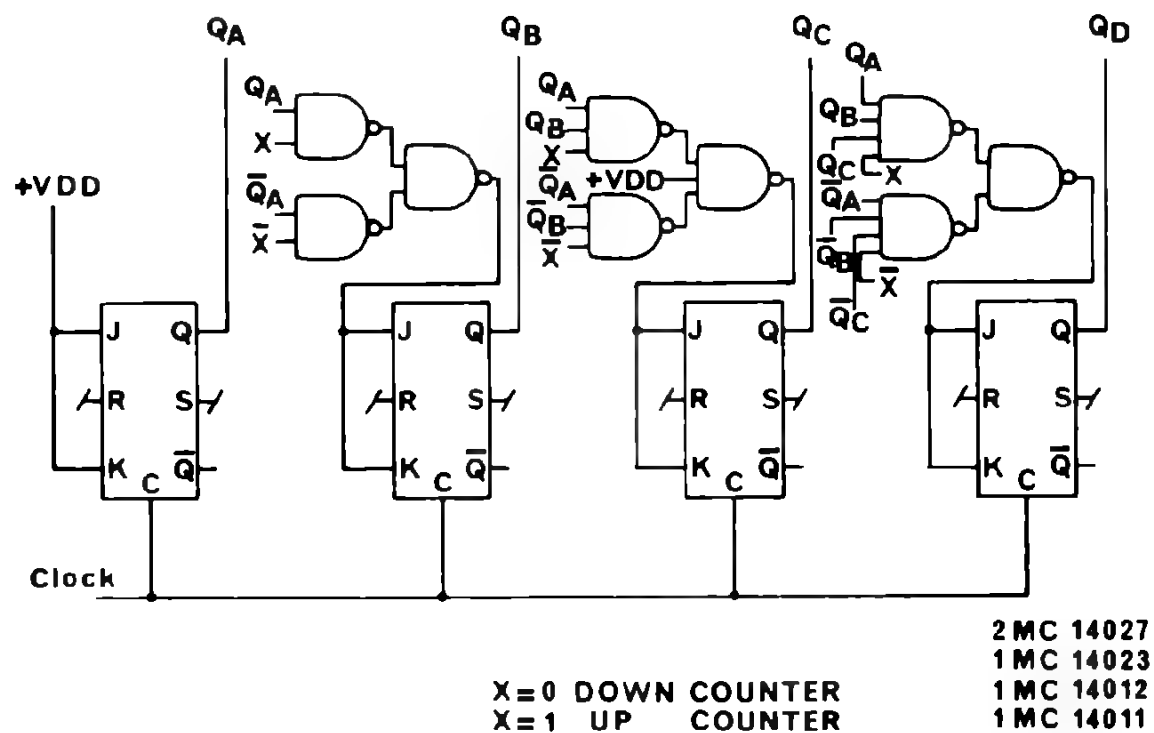


SYNCHRONOUS UP/DOWN COUNTER

– Divide by 10 Up/Down counter



– Divide by 16 Up/Down counter

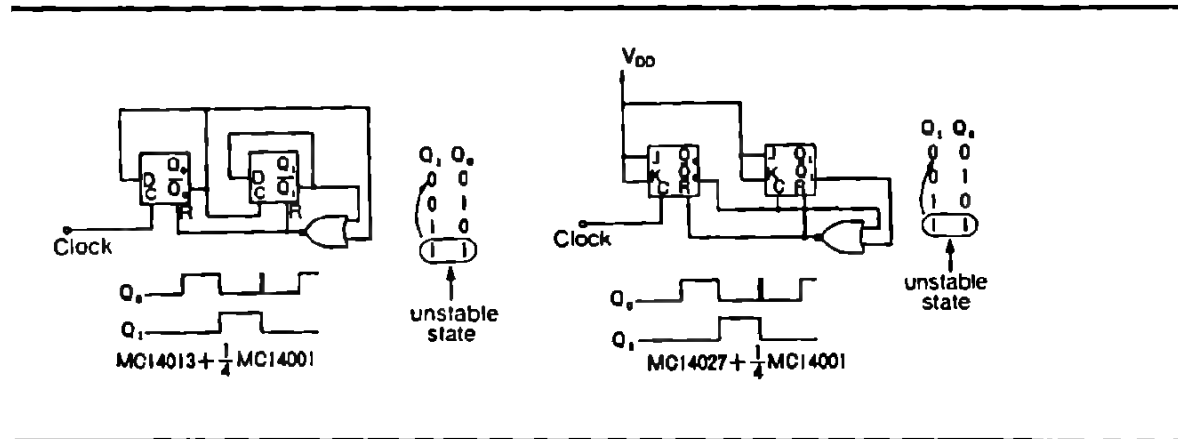


ASYNCHRONOUS UP COUNTER :

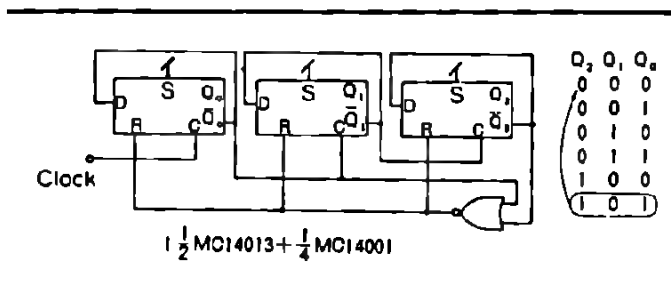
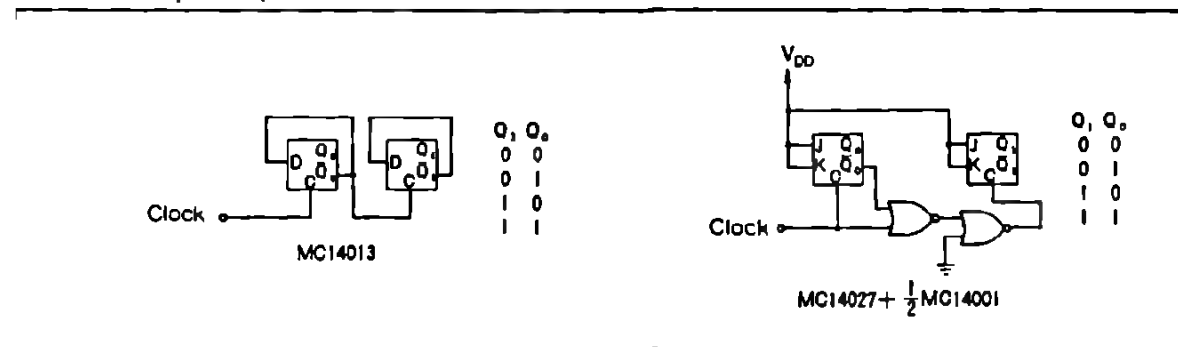
Usually asynchronous counters require fewer additional gates to perform the specified operations.

Example :

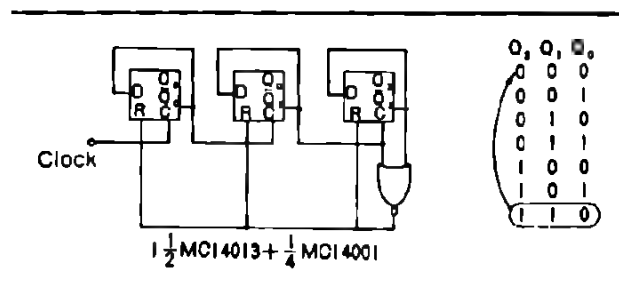
- Divide by 3 Up counter



- Divide by 4 Up counter

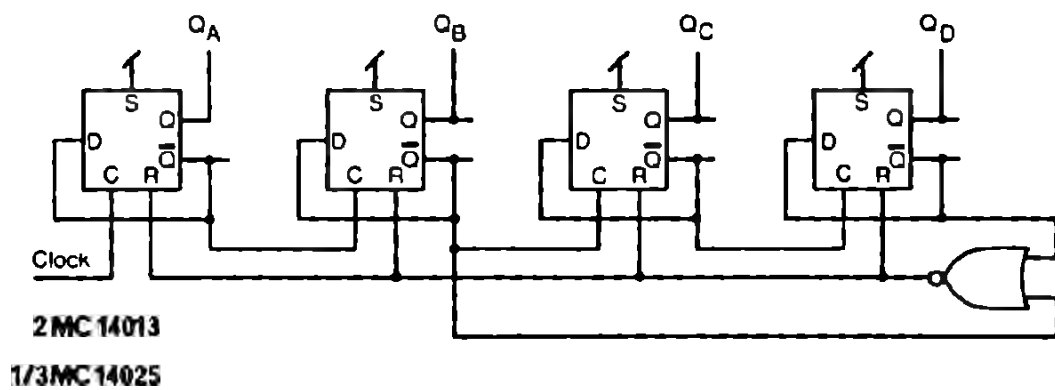


– Divide by 5 Up counter



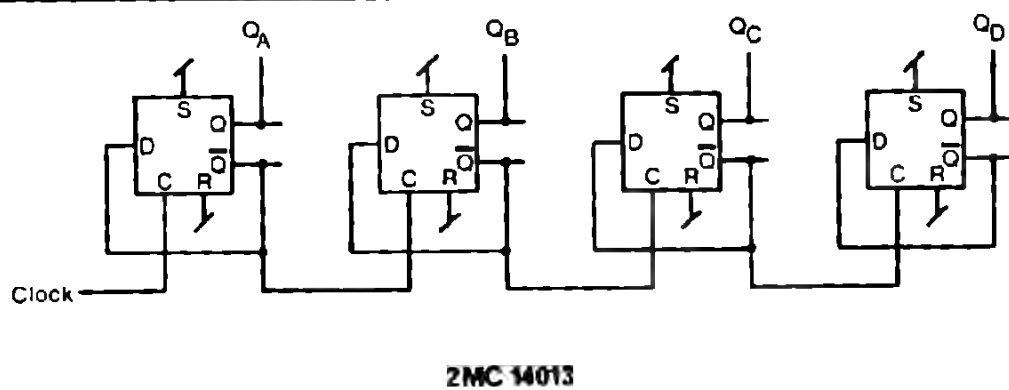
- Divide by 6 Up counter

Divide by 10 Up counter



Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1

Divide by 16 Up counter



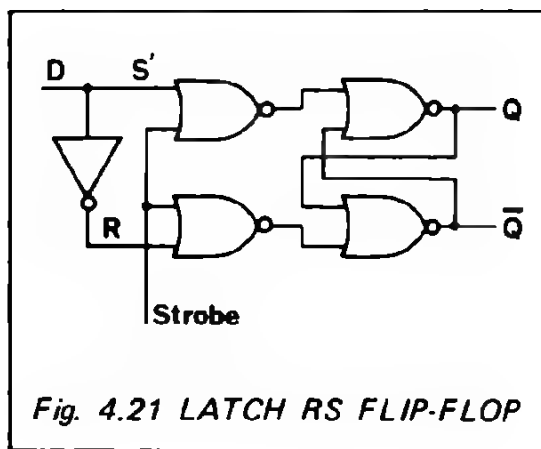
4. 2. 2. LATCHES

The latch function allows the storage of logic information when required. The information to be stored can be enabled by additional control input.

In the CMOS family latches are used mainly :

- as latch function itself
 - as latch decoder function
 - as latch "store" in complex functions such as 3 digit counters, memories etc.
- Distinction should be made between two types of basic latch configuration: the latch RS flip-flop and the CMOS gated flip-flop.

In this section, these functions will be briefly described. The description of a dual 4-bit latch, a quad clocked "D" latch and a 4-bit latch/decoder will follow.



4. 2. 2. 1. Latch RS flip-flop

This circuit is very similar to the gated RS flip-flop in 4.13. The main difference here is that the input state of R and S can never be "1" or "0" simultaneously. This is enforced by connecting an inverter between the R and S inputs.

Figure 4.21 represents a latch RS flip-flop which uses NOR gates.

Because of the above mentioned connections, the truth table is simplified and becomes:

D	Strobe	Q
0	0	0
1	0	1
X	1	Q

X don't care

From this table it can be seen that the latch changes its content as long as the strobe input is low, "0". When the strobe goes high, "1", the information applied to D remains memorized.

4. 2. 2. 2. CMOS gated flip-flop

Figure 4.14 illustrated a CMOS gated flip-flop. This structure is also very often used as a latch in CMOS digital circuits. The main advantage is that it requires fewer gates than the latch RS flip-flop, which results in a saving of space on the CMOS chip. The truth table is equivalent to the truth table of the latch RS flip-flop.

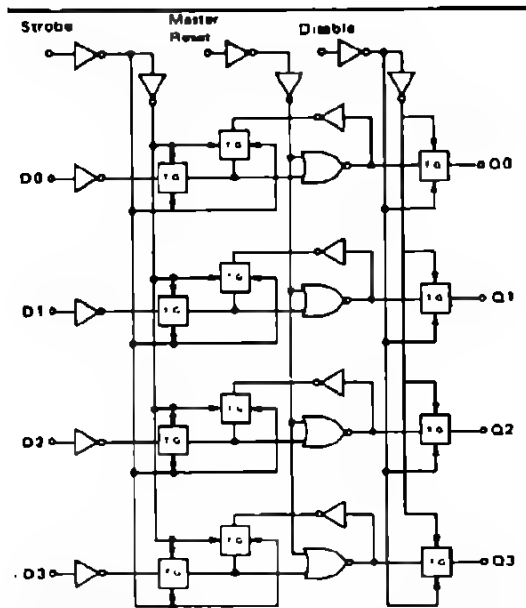


Fig. 4.22
LOGIC DIAGRAM OF THE 4-BIT
LATCH (1/2 MC 14508)

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	1	1
0	1	0	0	1	0	0	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0
0	1	0	0	1	1	1	0	1	1	1
0	1	0	1	0	0	0	1	0	0	0
0	1	0	1	0	0	1	1	0	0	1
0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	1	1	0	1	1
0	1	0	1	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1	1	0	1
0	1	0	1	1	1	0	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1
0	0	0	x	x	x	x	LATCHED			
1	x	0	x	x	x	x	0	0	0	0
x	x	1	x	x	x	x	HIGH IMPEDANCE			

MR: Master reset

ST: Strobe

It should be noted that when the strobe is high (1) data can be transferred to the latches; conversely when the strobe is low (0) data is stored. The high impedance tristate status is controlled by the state of the disable input pin which is activated by applying a "1". Typical applications, which are self explanatory, of 4-bit latches are illustrated in Figure 4.23 and 4.24.

4.2.2.3. Dual 4-bit latch — MC 14508

This circuit is composed of two identical sections. Each section includes the CMOS gated flip-flop latch described above and has tristate output features. Figure 4.22 shows the logic diagram of one section of the dual 4-bit latch (1/2 MC 14508).

Each section has its own strobe, master reset, and disable (tristate) inputs. All the data inputs are buffered assuring therefore maximum noise immunity. The logic operation of this circuit is summarized in the following truth table.

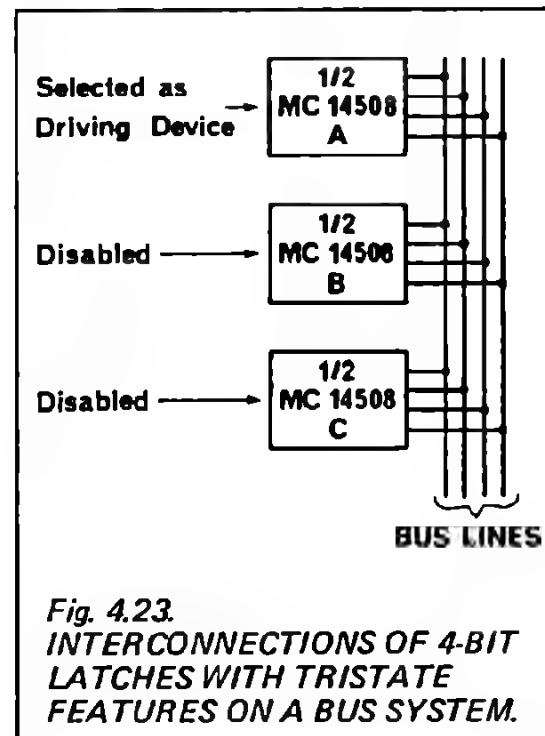


Fig. 4.23
INTERCONNECTIONS OF 4-BIT
LATCHES WITH TRISTATE
FEATURES ON A BUS SYSTEM.

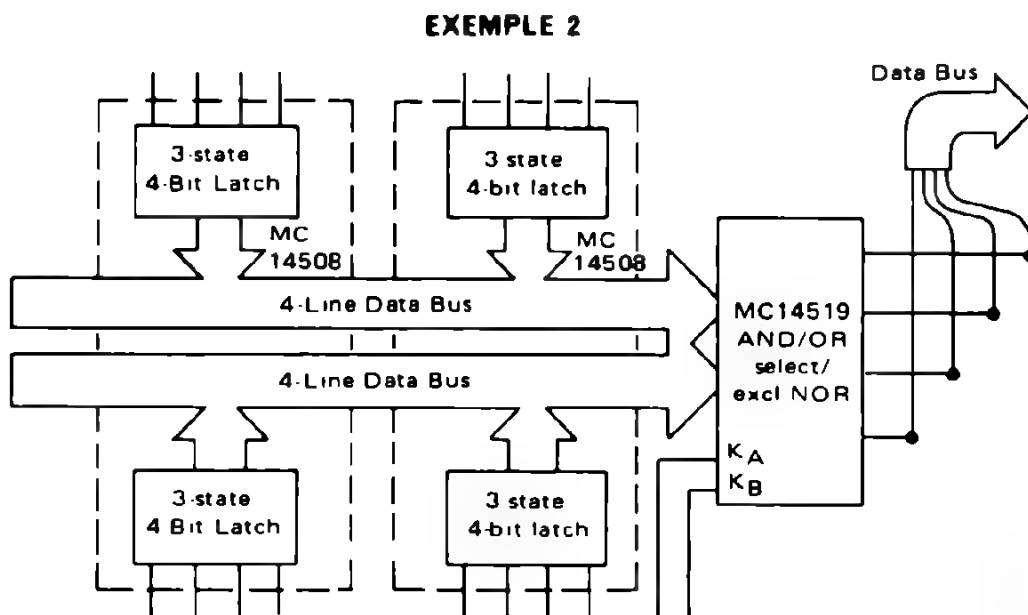
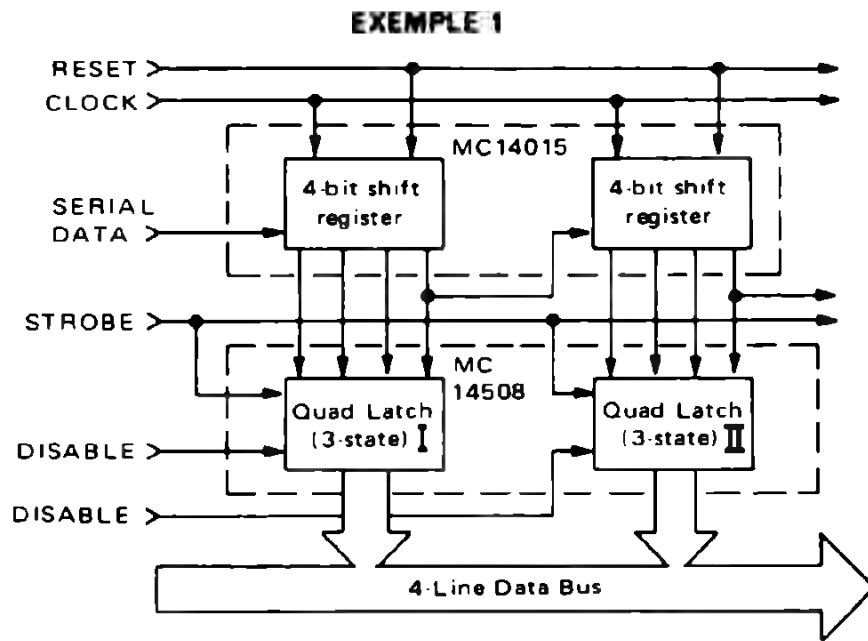


Fig. 4.24 DATA TRANSFER ON A BUS SYSTEM WITH STORAGE USING THE DUAL 4-BIT LATCH MC 14508

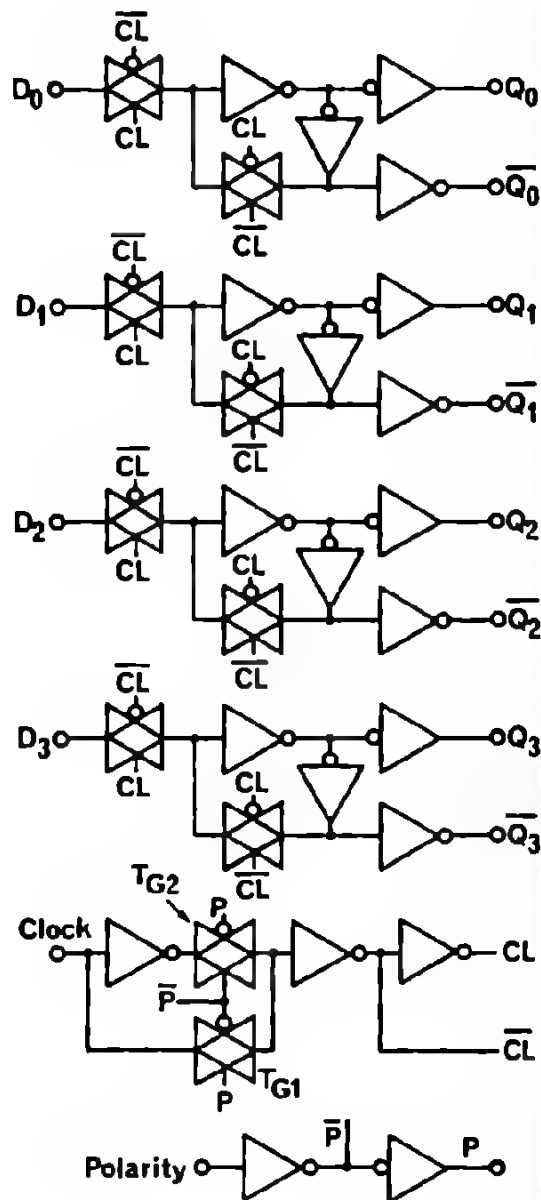


Fig. 4.25
LOGIC DIAGRAM OF THE QUAD
CLOCKED "D" LATCH - MC 14042

The truth table is:

This quad clocked "D" latch finds application in data storage , registers, parallel/serial data conversions and in data multiplexing systems.

4. 2. 2. 5. 4-Bit latch/4-to-16 line decoder MC 14514 and MC 14515

This circuit is composed of two sections:

- the input section consisting of 4 latch RS flip-flops allowing the storage of the input data, when the strobe input is at "0".
- the output section, a 4 bit binary to 1 of 16 decoder stage.

Two options are provided:

- the circuit MC 14514 generates a "1" at the decoded output stage.
- the circuit MC 14515 generates a "0" at the decoded output stage.

The logic diagram is represented in Figure 4.26.

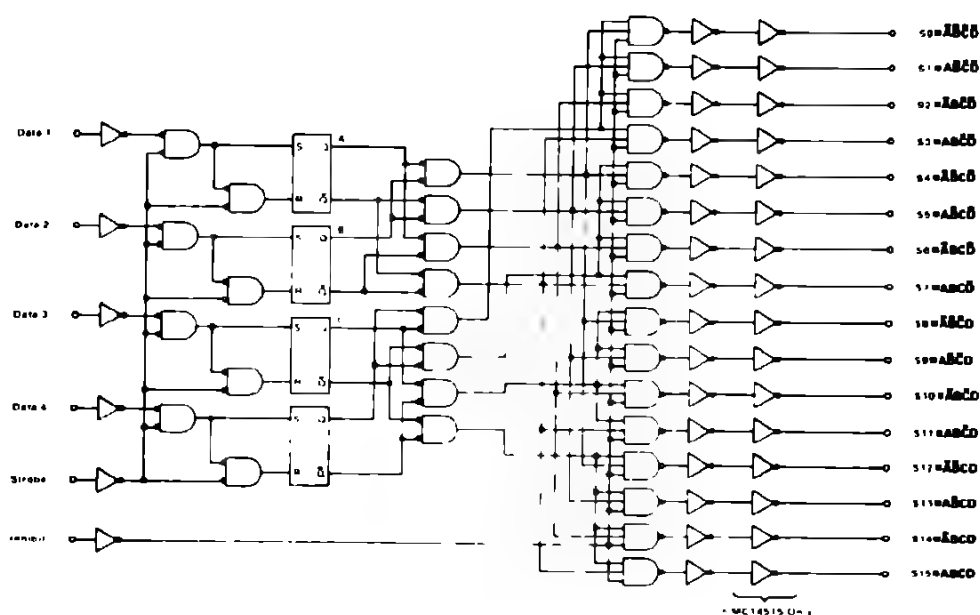


Fig. 4.26 LOGIC DIAGRAM OF THE 4 BIT LATCH/4 TO 16 LINE DECODER MC 14514/15

The truth tables become
for MC 3454

[illegible]

X = don't care
for stroke = 'i' → Latch

FOR MAC 14315

[illegible]

It doesn't care
for stroke = 0 - Latch

MC 14512 eight-channel data selectors are used with the MC 14514 four-bit decoder to effect a complex data routing system. A total of 16 input data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way initial data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

is placed into the routing scheme via the eight inputs on both MC 14512 selectors. One register is assigned to each input. The signals on A0, A1, A2 choose one of eight inputs for transfer out to the 3-state data bus. A signal, labelled Dis, disables one of the MC 14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 to 16, the rate of transfer of the initial information can also be varied. That is, if the MC 14512 were used at a rate that is eight times faster than the shift frequency of the registers, the most significant bit (MSB) from each register could be used for transfer to the data bus. Therefore, all of the most significant bits of all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC 14514 four-bit decoder. Using the four-bit address, D1 to D4, the information on the data line can be transferred to the addressed output line to the desired output registers, A to P. This distribution of data bits to the output registers.

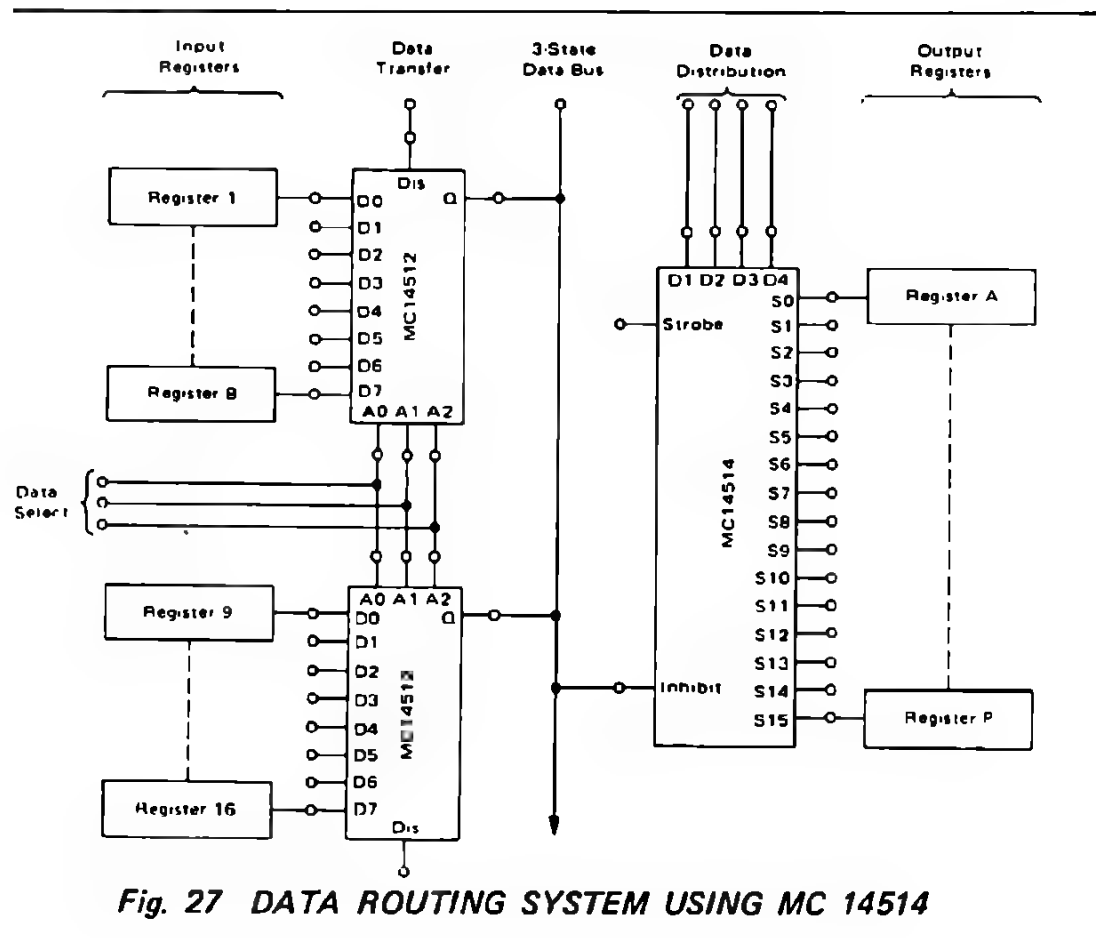


Fig. 27 DATA ROUTING SYSTEM USING MC 14514

can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

The latch/decoder find its main application in data routing systems. Figure 4.27 present an application where the latch/decoder circuit is used officiently.

4. 2. 3. SHIFT REGISTERS

Universally used, shift registers find their main applications in arithmetic logic units, in parallel to serial and serial to parallel data conversions, in pseudo random cycle generators, in general logic, and in storage circuits.

The MOTOROLA CMOS shift register program can be divided into two categories:

- the standard shift register with constant or variable word length, used mainly as a temporary storage element.

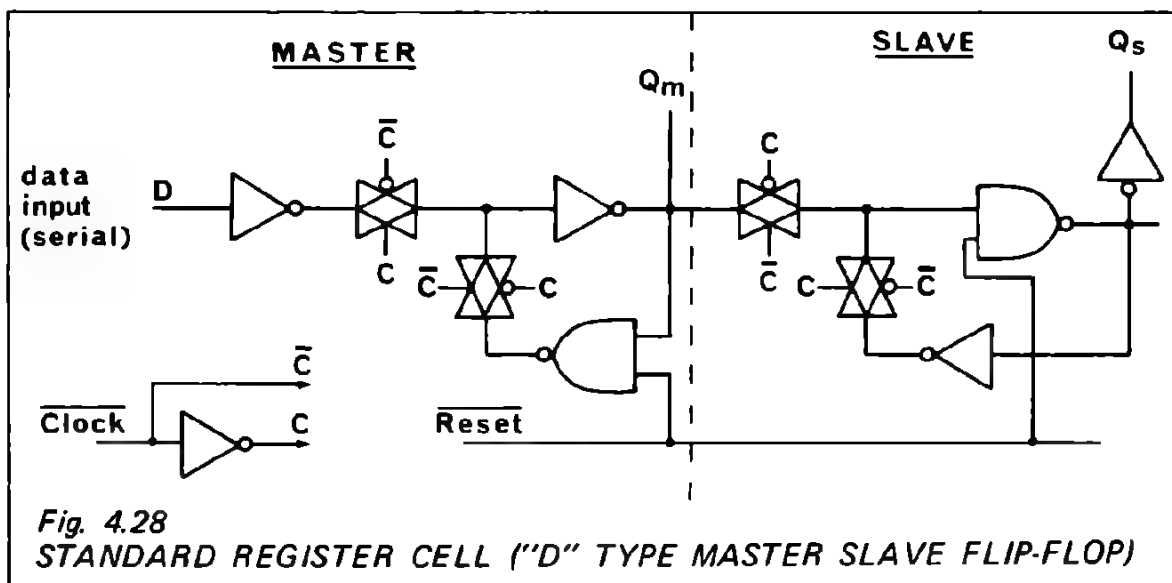
These shift registers usually feature single serial input and output and in some cases an n-bit parallel input/and output.

- the universal bus shift register usually featuring bidirectional data flow.

All MOTOROLA CMOS shift registers are of a static nature. In this section, first, we will describe briefly the basic register cell used in shift registers, then we will describe in some detail the MOTOROLA shift registers.




4. 2. 3. 1. Basic register cells used in static shift register

The basic register cell configurations used in static shift registers are represented in Figure 4.28 and 4.29.












This cell is the standard register cell.

Clock	D	Q _m (master)	Q _s (slave)
	0	0	0
	1	1	1
	X	X	Q _n

The truth table, including the parallel/serial control input is :

parallel/serial P/S	Clock	data D _s	data D _p	Q _m (master)	Q _s (slave)
0		0	X	0	0
0		1	X	1	1
0		X	X	X	Q _n
1		X	0	1	1
1		X	1	0	0
1		X	0	1	Q _n (1)
1		X	1	0	Q _n (0)

2. 3. 2. Dual 4-bit static shift register MC 14015

This module is composed of two identical and independent static shift registers of 4-bits each.

Each register has an independent data clock and reset input, with serial input, and serial/parallel output features.

The register cells used in this circuit are described in the previous section and are of the type "D" master slave flip-flop. The data applied is shifted from one stage to the next on the positive going clock transition.

Reset is achieved by applying a high level signal to the reset input.

Figure 4.30 represents the logic diagram of the whole module. It should be mentioned that all inputs and outputs are buffered which results in maximum noise immunity. This circuit has no tristate (disable) output control.

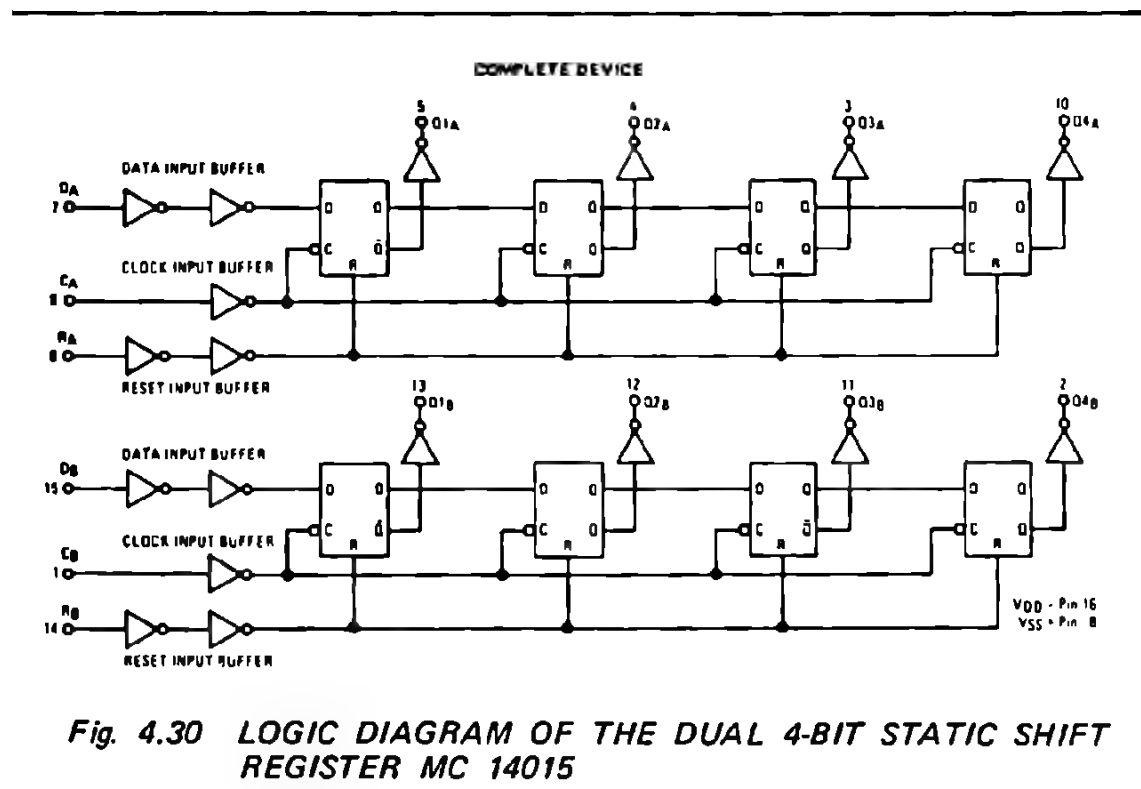


Fig. 4.30 LOGIC DIAGRAM OF THE DUAL 4-BIT STATIC SHIFT REGISTER MC 14015

The truth table of each register is as follows :

Clock	R	D	Q1 first register	Qn
	0	0	0	Q_{n-1}
	0	1	1	Q_{n-1}
	0	X	Q_1	Q_n
X	1	X	0	0

X = don't care

No change

Typical applications of this static shift register are, in serial/parallel data conversion, in pseudo random number generators and in data storage.

4. 2. 3. 3. 4-Bit parallel in/parallel out static shift register MC 14035

Built up from four register cells with the parallel input feature, this static shift register allows the following operations :

- serial input/serial output
- serial input/parallel output
- parallel input/parallel output
- parallel input/serial output

On the "D" input of the first register cell there are additional gatings which convert it into a J and \bar{K} flip-flop. This feature saves external gating when the register is used as a counter or sequence generator. All register cells can be reset by applying a high level to the common reset input.

The parallel/serial operating mode is controlled by the P/S input. This circuit has also a "true/complement" control input, which allows the complementation of the output by generating the "true" or the "complement" values at the register outputs.

Figure 4.31 represents the logic diagram. This circuit has no tristate (disable) output control.

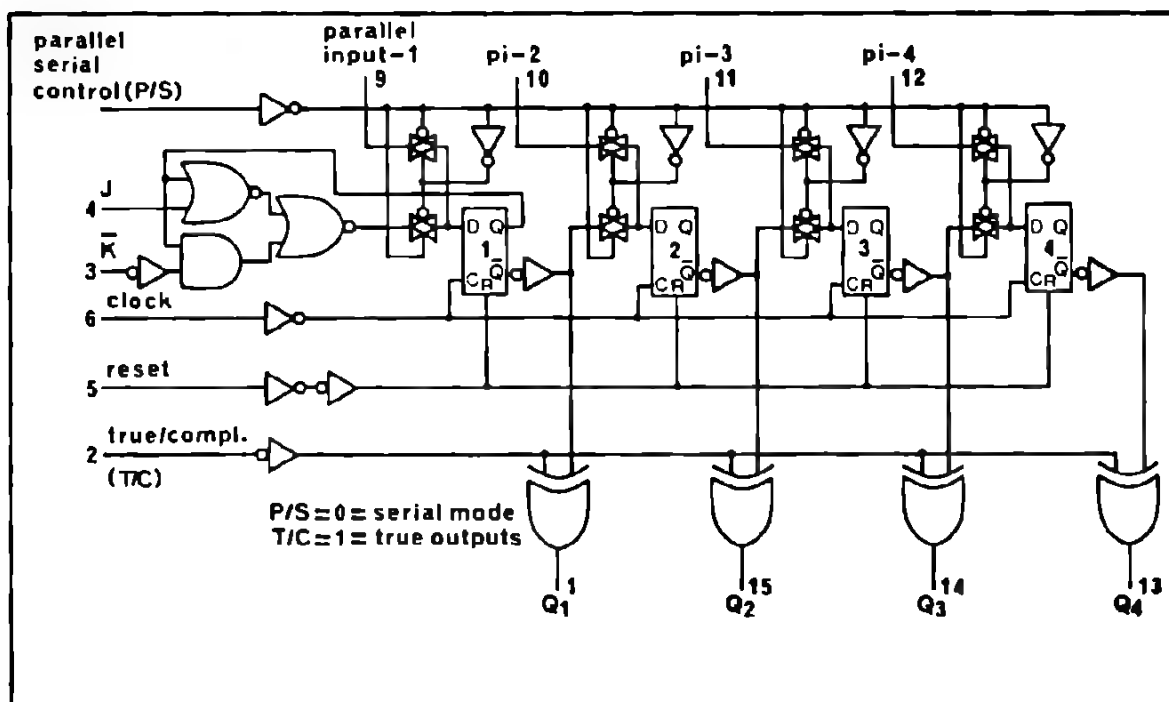


Fig. 4.31 LOGIC DIAGRAM OF THE 4-BIT PARALLEL IN/PARALLEL OUT STATIC SHIFT REGISTER - MC 14035

This circuit finds its main application in sequence generation, code conversion, counters, serial to parallel and parallel to serial conversion.

Figure 4.32, 4.32a and 4.33 show typical applications of the 4-bit parallel in/parallel out shift registers.

The truth tables for the synchronous (clocked mode) and asynchronous (direct mode) operation are:

ynchronous operations :

Clock	R	J	\bar{K}	Q_1	
				Q_{n-1}	Q_n
	0	0	X	0	0
	0	1	X	0	1
	0	X	0	1	0
	0	1	0	Q_{n-1}	\bar{Q}_{n-1}
	0	X	1	1	1
	0	X	X	Q_{n-1}	Q_{n-1}

Asynchronous operation :

R (reset)	True/ Complement T/C	Q_n
0	0	\bar{Q}_n
1	0	1
0	1	Q_n
1	1	0

Parallel / Serial

P/S	Mode
0	Serial
1	Parallel

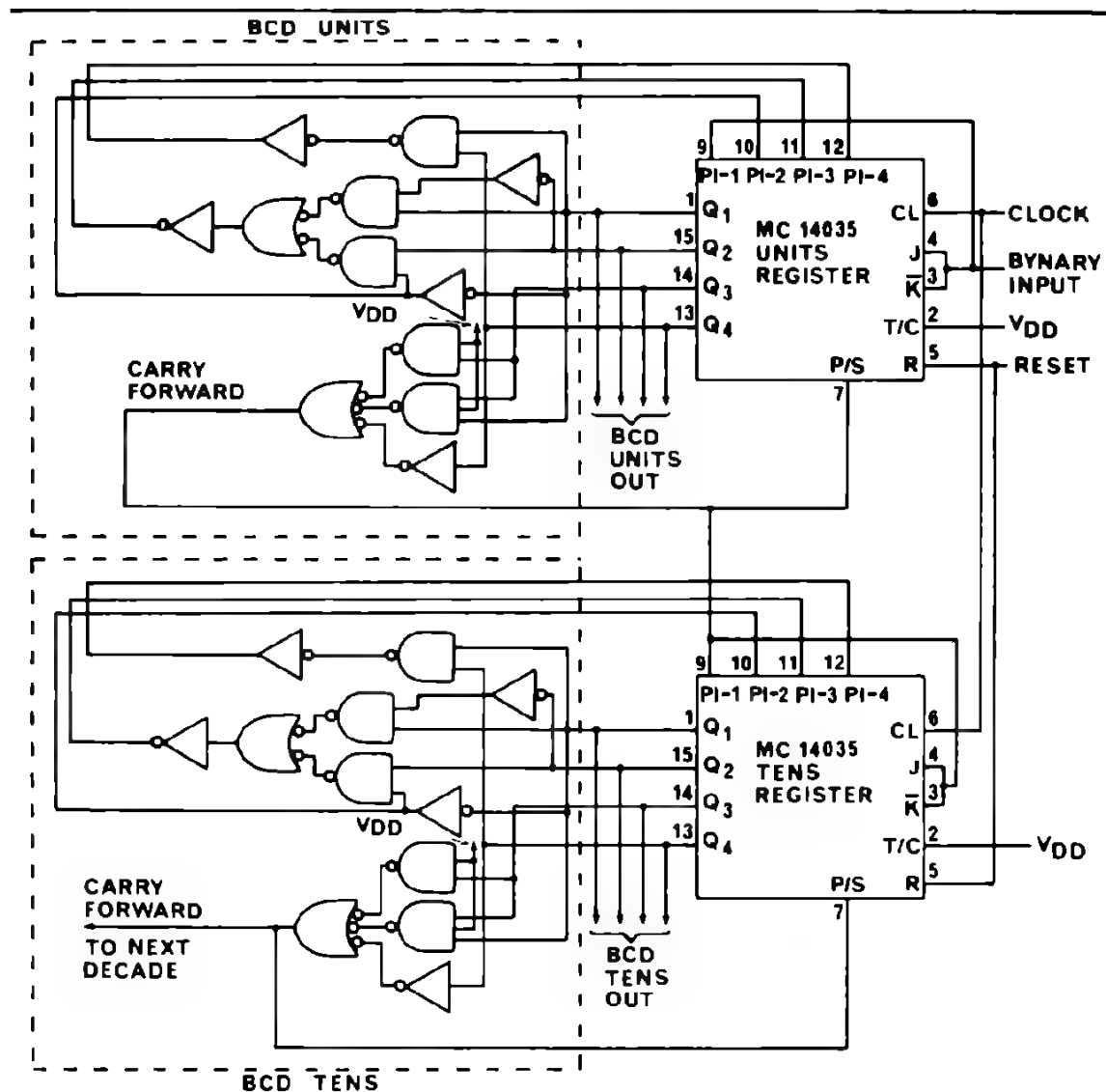


Fig. 4.32 BINARY TO BCD CODE CONVERTER

4. 2. 3. 4. 8-Bit static shift register – MC 14021

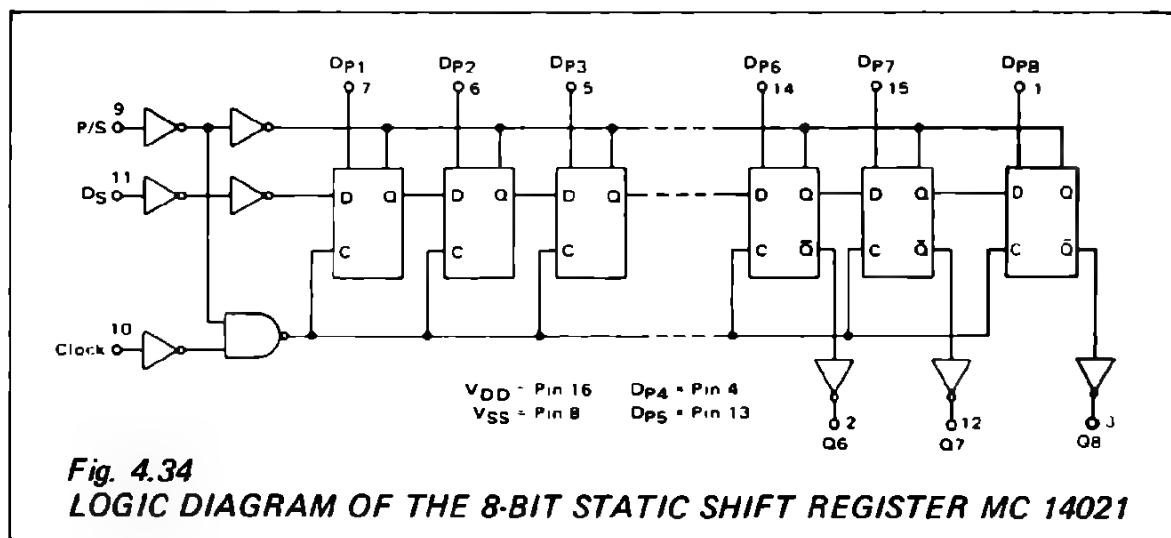
Composed of 8 register cells each with parallel input, this register was mainly designed for applications of serial in/serial out and parallel in/serial out conversions.

Only the outputs 6, 7, 8 are available.

The parallel/serial input controls the parallel/serial operation mode.

Each cell can be set directly through the parallel input : $D_{p1}...D_{p8}$. The register cells used in this circuit are "D" master slave flip-flops. The serial inputs and all outputs are buffered for maximum noise immunity.

The logic diagram is shown in Figure 4.34.



This circuit has no tristate (disable) output control.

The truth tables for both parallel and serial operations are

– serial mode :

t	CLOCK	D _S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

– parallel mode :

CLOCK	D _S	P/S	D _m	*Q _m
X	X	1	0	0
X	X	1	1	1

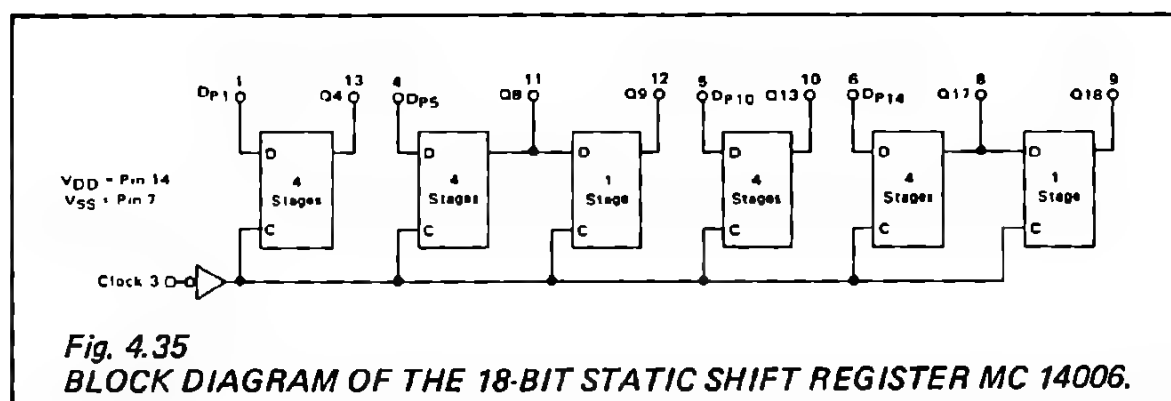
*Q6, Q7, & Q8 are available externally

"X" = Don't Care

4. 2. 3. 5. 18-Bit static shift register – MC 14006

This shift register is composed of four separate register sections sharing a common clock : two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs.

This circuit uses, as register cell, the "D" master slave flip-flop previously described. The serial input and all outputs are buffered. The data transfers occur on the falling edge of the clock pulse. The block diagram is illustrated in Figure 4.35.



The truth table is (per register cell):

D _p	Clock	Q _{n+1}
0		0
1		1
X		Q _n

This circuit is particularly designed for the serial in/serial out operation and finds its main application in time delay circuits. Longer shift register configurations are possible by using several MC 14006 connected in cascade.




4. 2. 3. 6. Dual 64-bit static shift register MC 14517

This dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods and also permits bus logic to be used.

The block diagram is represented in Figure 4.36 (half section).

ig. 4.36 EXPANDED BLOCK DIAGRAM OF THE DUAL 64-BIT STATIC SHIFT REGISTER MC 14517 - (ONE SECTION SHOWN ONLY).

This functional truth table is:

Clock	Write/Enable	Data	Q ₁₆	Q ₃₂	Q ₄₈	Q ₆₄
0	0	X	Q ₁₆	Q ₃₂	Q ₄₈	Q ₆₄
	0	0	← shift n+1 →			
	0	1				
1	0	X	Q ₁₆	Q ₃₂	Q ₄₈	Q ₆₄
	0	X	Q ₁₆	Q ₃₂	Q ₄₈	Q ₆₄
X	1	X	← high impedance →			

X= don't care

This register finds usage in temporary storage for visual displays in applications such as CRT or LED displays matrix etc.

2. 3. 7. Variable length 64-bit static shift register MC 14557
(preliminary information)

This register is a programmable length static shift register for serial in/serial out applications. It consists of 7 shift register sections of binary related length which can be connected together by control logic.

A 6-bit program word controls the section combination thus making 2⁶ (64) possible register lengths.

Each control bit has binary weighting and the register length is equal to the sum of the weighted control bits.

The following table defines the register length:

CONTROL WORD (A)						REGISTER LENGTH (Bits)
A ₁	A ₂	A ₄	A ₈	A ₁₆	A ₃₂	
0	0	0	0	0	0	—
1	0	0	0	0	0	1
0	1	0	0	0	0	2
1	1	0	0	0	0	3
0	0	1	0		0	4
1	0	1	0			5
0	1	1	0			6
1	1	1	0			7
0	0	0	1			8
1	0	0	1			9
0	1	0	1			10
1	1	0	1			11
0	0	1	1			12
1	0	1	1	0		13
0	1	1	1	0		
			1	0		
			0	0		
			0	1		
			0			
			0			
			0			
			0			
			0			
			0			
			1			
1	1	1	1	1	1	64

In addition, this circuit provides two serial data inputs Y and Z, either of which can be selected by the control input Y/Z.

Through the \bar{Q} output, the complement of the output is also available.

A master reset allows all stages to be set to "0" regardless of the clock state. All inputs/outputs are buffered.

This circuit finds its main application in programmable delay-lines, programmable counters, organ circuits, etc..

1.2.3.8. 128-Bit static shift register — MC 14562 (preliminary information)

The 128-bit static shift register is mainly designed for data serial in/serial out applications. 8 outputs are available which are:

Q₁₆ — Q₃₂ — Q₄₈ — Q₆₄ — Q₈₀ — Q₉₆ — Q₁₁₂ — Q₁₂₈

and which provide a large usage flexibility. The pin diagram is represented in

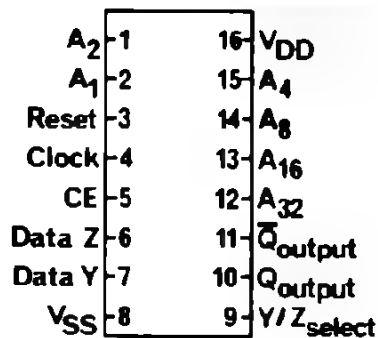


Fig. 4.37
PIN DIAGRAM (PRELIMINARY)
OF THE VARIABLE LENGTH
64-BIT STATIC SHIFT REGISTER
MC 14557

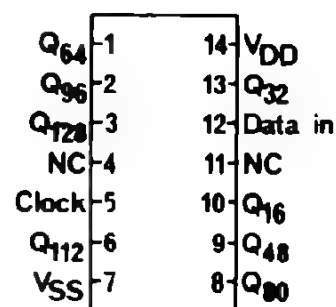


Fig. 4.38
128-BIT STATIC SHIFT REGISTER
MC 14562

2. 3. 9. 8-bit universal bus register MC 14034

Probably one of the most interesting shift registers belonging to the second category of register, is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allow a bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. In addition the serial data input allows data to be entered in a shift/right mode, while shift/left can be accomplished by hard-wiring each parallel output to the previous parallel input bit.

As shown in Figure 4.39 this circuit is, in principle, composed of 8 register cells connected in cascade with additional control logic.

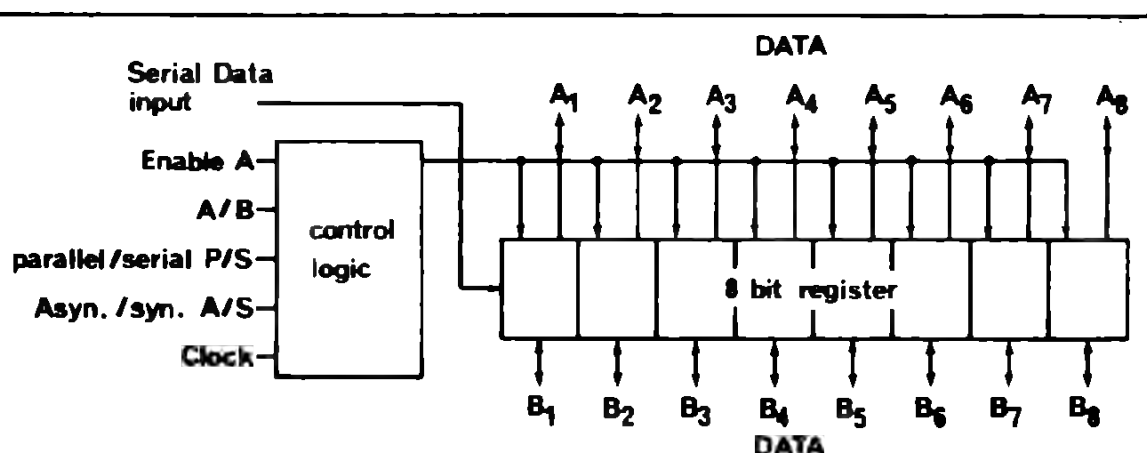


Fig. 4.39
BLOCK DIAGRAM OF THE 8-BIT UNIVERSAL BUS REGISTER MC 14034

Each register cell is composed of one "D" master slave flip-flop with separate internal clock and with, in addition, two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides 4 different features :

A ENABLE INPUT :

when high, this enables the bus A data lines

A/B INPUT (Data A or B) :

this input controls the direction of data flow :

when "high" the data flows from bus A to bus B;

when "low" the data flows from bus B to bus A.

P/S INPUT (PARALLEL/SERIAL):

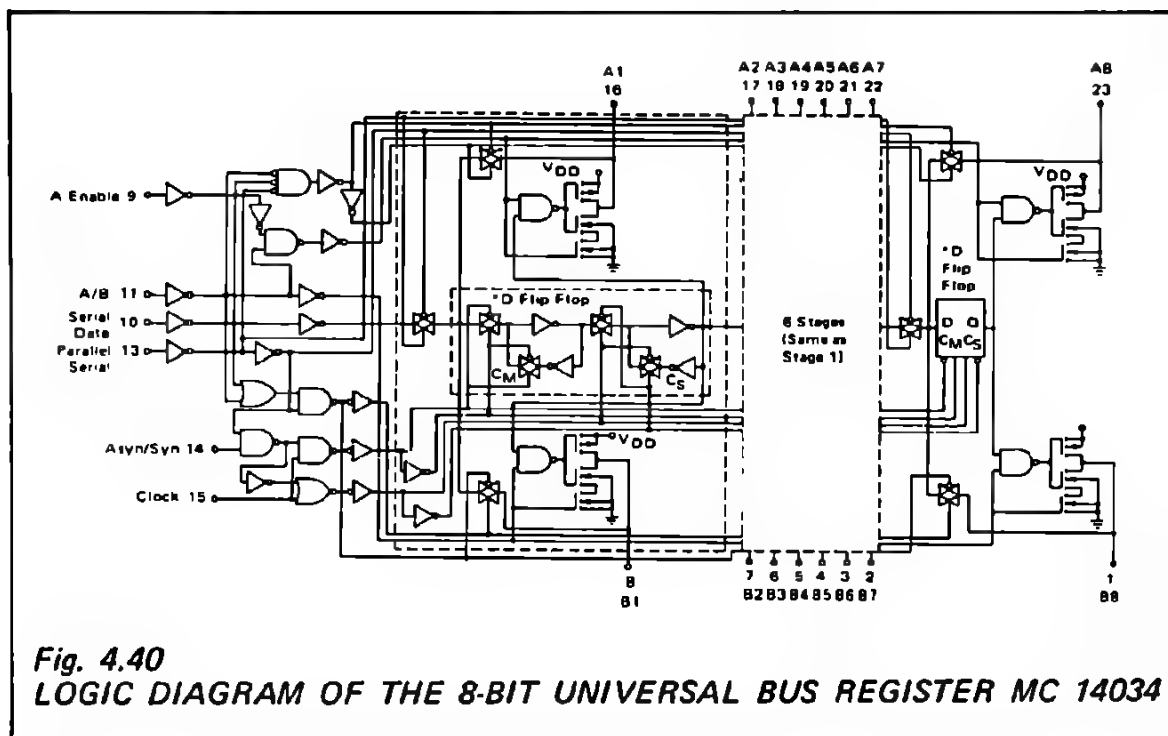
This input controls the data input mode (parallel or serial).

- when "high", the data is transferred to the register in an asynchronous mode (positive clock transition).
- when "low", the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S INPUT (ASYNCHRONOUS/SYNCHRONOUS TO THE CLOCK):

- when "high", the data is transferred independently from the clock rate.
- when "low", the clock is enabled and the data is transferred synchronously.

Figure 4.40 represents the logic diagram of the 8-bit universal bus register.



The following truth table of the control logic summarizes the operation of the register.

TRUTH TABLE					
"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A Parallel data inputs disabled, B Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B Parallel data output.

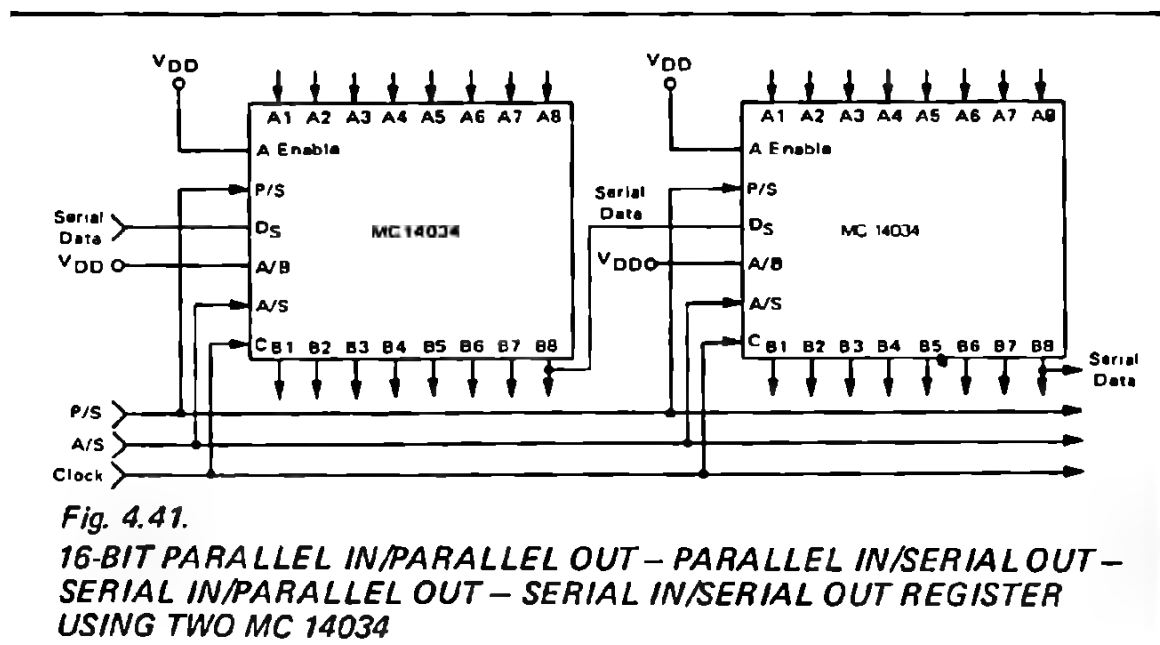
X = Don't Care

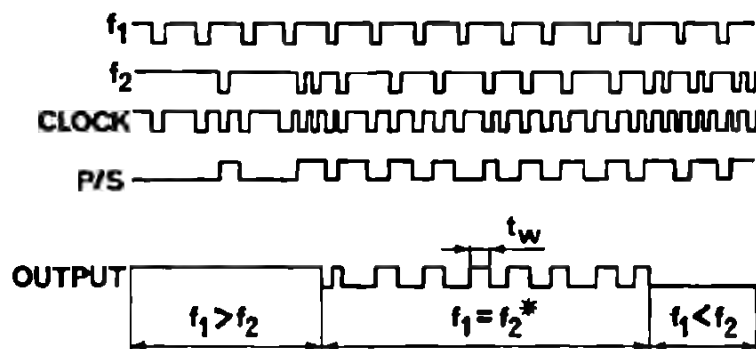
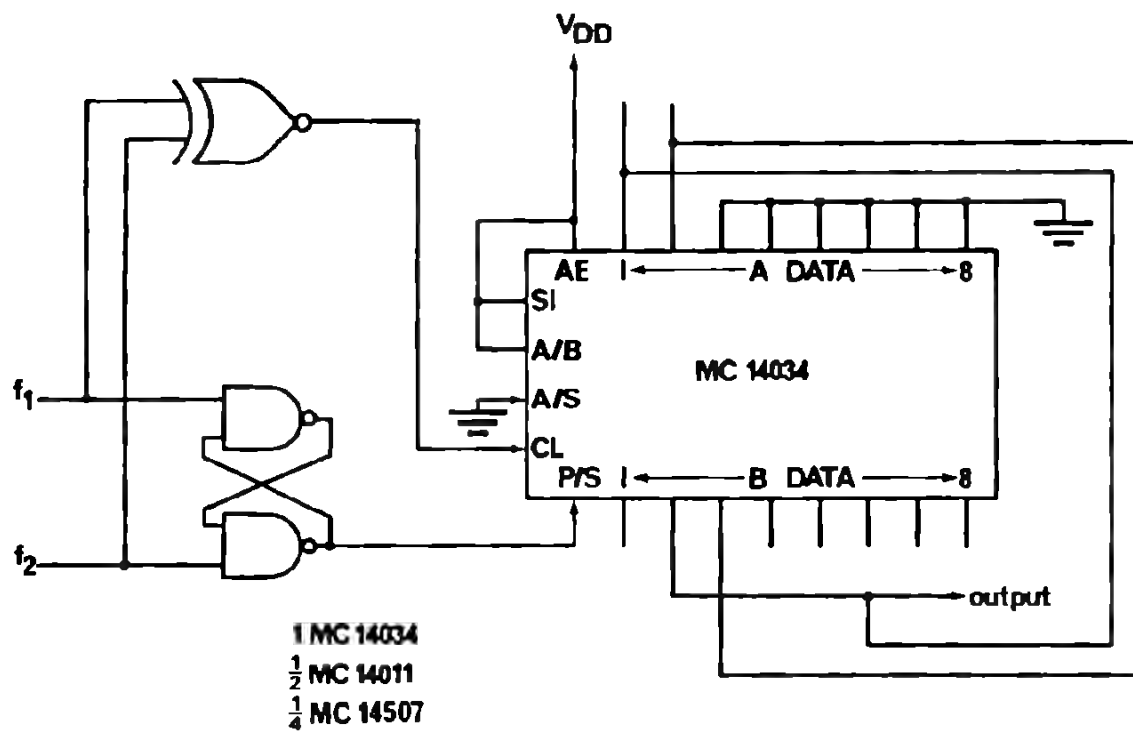
† Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

Useful applications of this register include:

pseudo random code generation, sample and hold register, frequency and phase comparator, code conversion, serial to parallel and parallel to serial conversion.

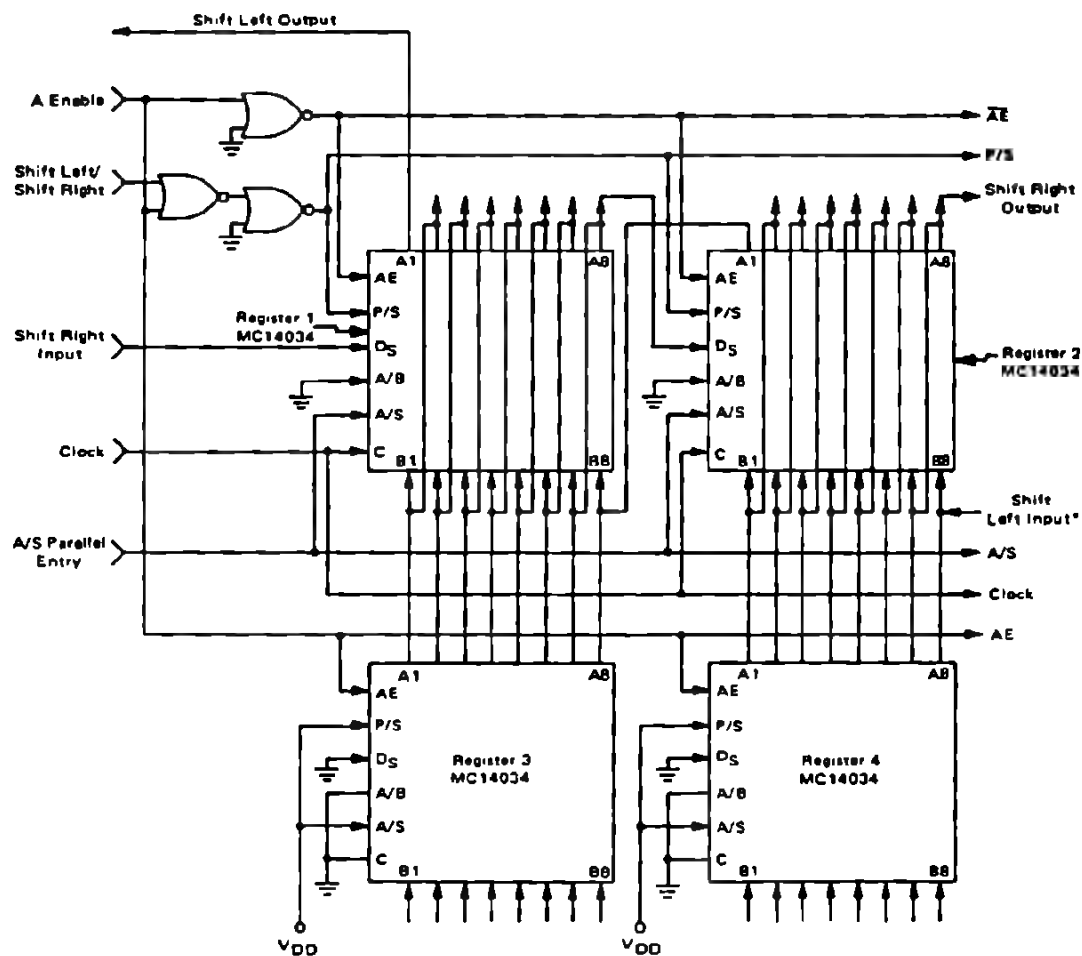
The following three Figures (4.41 – 4.42 – 4.43) show some typical applications of the 8-bit universal bus register.





*When $f_1 = f_2$, t_w is proportional to the phase of f_1 with respect to f_2

Fig. 4.42 FREQUENCY AND PHASE COMPARATOR USING MC 14034



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

Fig. 4.43
16-BIT SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUT REGISTER
USING 4 x MC 14034

4. 2. 4. CMOS COUNTERS & TIMERS

The MOTOROLA CMOS range of counters/timers will be presented here in four different sections.

First, we discuss general counter characteristics and the terminology used in counter specifications.

Next some basic CMOS counter cells will be analyzed. In a separate section, the synchronous counter range will be presented. Particular attention will be given to the problem of cascading counters.

Finally, the asynchronous counters/timers will be discussed.

4. 2. 4. 1. Introduction to counters & timers

Probably the most useful MSI functions available in the CMOS family, counters and timers can be classified according to the table shown in Figure 4.44.

This classification is related to two main variables which are:

- the operating code of the counters
- the operation mode of the counters

In standard counters, usually 3 types of operating codes are used:

- the binary code
- the binary coded decimal code (BCD)
- the Johnson code, octal or decimal.

CODE	BCD	BINARY			JOHNSON	
Type	BCD	Binary counter	Ripple		Octal counter	Decimal counter
Function	counter		counter	timer		
UP	MC 14518	MC 14520	MC 14020 MC 14024 MC 14040	MC 14521 MC 14536	MC 14022	MC 14017
DOWN	MC 14522*	MC 14526				
UP/DOWN	MC 14510**	MC 14516**				

* programmable

** presettable

*Fig. 4.44. CLASSIFICATION TABLE OF CMOS COUNTERS & TIMERS
ACCORDING TO THEIR FUNCTION*

Figure 4.45 represents the truth tables of the codes previously mentioned. The binary code is a weighted code and gives the minimum number of counting cells in a counter system. The number of counting cells, N, in a counter, can be calculated by the following equation:

$$N = 3.322 \log_{10} X$$

where X is the maximum count state of a system, and, of course N is always an integer.

BINARY Code					BCD Code					JOHNSON Code (Octal)					JOHNSON Code (Decimal)					
variables					variables					variables					variables					
state	A	B	C	D	state	A	B	C	D	state	A	B	C	D	state	A	B	C	D	E
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0
2	0	1	0	0	2	0	1	0	0	2	1	1	0	0	2	1	1	0	0	0
3	1	1	0	0	3	1	1	0	0	3	1	1	1	0	3	1	1	1	0	0
4	0	0	1	0	4	0	0	1	0	4	1	1	1	1	4	1	1	1	1	0
5	1	0	1	0	5	1	0	1	0	5	0	1	1	1	5	1	1	1	1	1
6	0	1	1	0	6	0	1	1	0	6	0	0	1	1	6	0	1	1	1	1
7	1	1	1	0	7	1	1	1	0	7	0	0	0	1	7	0	0	1	1	1
8	0	0	0	1	8	0	0	0	1	0	0	0	0	0	8	0	0	0	1	1
9	1	0	0	1	9	1	0	0	1						9	0	0	0	0	1
10	0	1	0	1	0	0	0	0	0						0	0	0	0	0	0
11	1	1	0	1																
12	0	0	1	1																
13	1	0	1	1																
14	0	1	1	1																
15	1	1	1	1																
0	0	0	0	0																

Fig. 4.45 STANDARD CODES USED IN COUNTERS

In practice the maximum capacity of a counter is limited by economic considerations and by the number of available pins in a package.

One disadvantage of the binary code is that, when advancing from one state to the next, several logic variables can change simultaneously. If not used correctly these effects during decoding, can generate unwanted transients (sometimes called "glitches").

The BCD code is also a weighted code and is particularly used in arithmetic logic and in decimal counting systems. The restrictions for the binary code apply also to the BCD code. The number of counting cells in a BCD counter is always 4 per digit.

The Johnson code has the feature that only one logic variable changes when the counter advances to the next state. Whatever the capacity of a counter, this code allows use of a very simple structure for the decoding stages and presents no glitches. The disadvantage of the Johnson code is that it requires more counting stages. The number of counting stages is given in this case by:

$$N = \frac{x}{2}$$

This means that for $x = 8$: a 4 stage counter is required (octal); for $x = 10$: a 5 stage counter (decimal) is required.

A counter is called an up counter when its contents increment by one or more units at each clock pulse.

For example, a BCD up counter has sequential states: 0,1,2,3,...8,9,

A counter is called a down counter when its content decrements by one or more units at each clock pulse:

For example a BCD down counter has sequential states: 9,8,7,...2,1,0, Some circuits can operate in either mode and these are then called up/down counters.

Two additional characteristics which are found in some counters are:

- the preset feature
- the programmable feature

The preset feature allows the counter content to be set to a pre-determined value. This feature is used particularly in programmable counters, which in some cases require additional external gating.

The programmable feature allows the counting cycle length to be determined by a variable applied to the preset inputs. The programmable counters are usually down counters which by means of the preset enable input introduces the preset variable into the counter in parallel mode as soon as the counter content reaches '0'. These counters do not need external gating because it is already provided internally. In some particular cases like timers, programming is achieved by means of logic connected at the output of the counting chain. A binary word may then select the required counting factors. These modules are mainly used as programmable frequency dividers.

4. 2. 4. 2. Basic counter cells

There are three different basic counter cells :



- the "D" master-slave flip-flop with direct reset input. This is mainly used in up/down counters.
- the toggle flip-flop. This is mainly used in ripple counters & timers.
- the toggle enable flip-flop with direct set input controlled by the preset enable input and with direct reset input control. This flip-flop is mainly used in presettable and programmable counters.

"D" MASTER SLAVE FLIP-FLOP:

The D master slave flip-flop used in counters is, in principle, composed of two cascaded CMOS gated flip-flops.

Figure 4.46 illustrates the logic diagram of the D master slave flip-flop. It should be mentioned that usually the reset function is achieved by forcing a logical "1" into the output of the feedback inverters.

The general truth table of the "D" master slave flip-flop is as follows if the input is equal to D_n :

clock	master Q'	slave Q
	$D_n(\text{stored})$	D_n
	$D_n + 1$	$D_n(\text{stored})$

It should be noted that the data input value is transferred to the Q output at the positive clock transition.

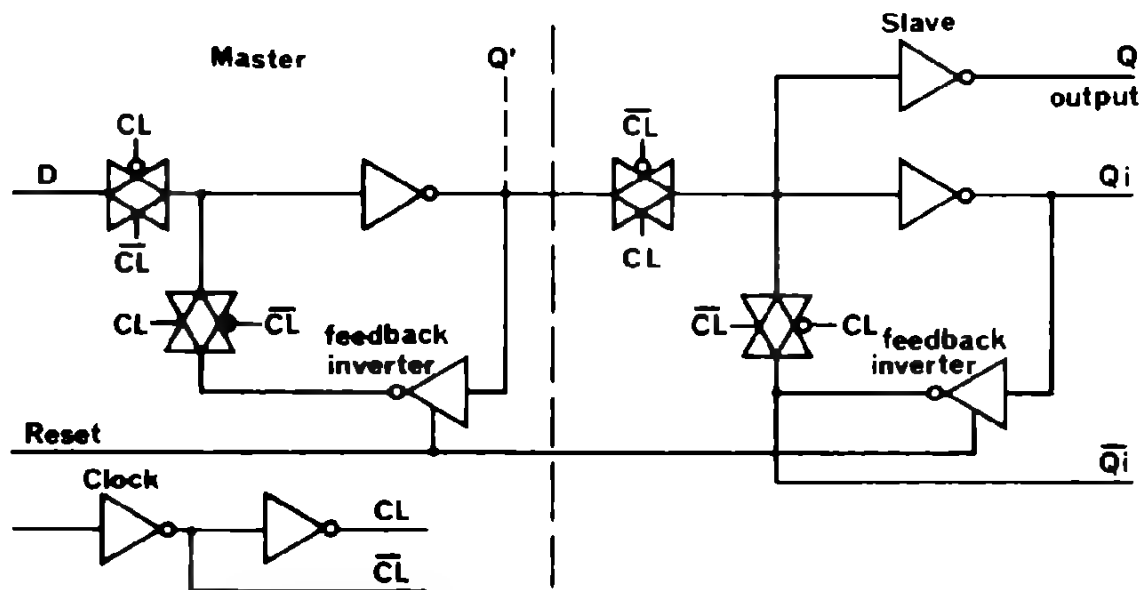


Fig. 4.46 LOGIC DIAGRAM OF A "D" MASTER SLAVE FLIP-FLOP USED IN COUNTERS

TOGGLE FLIP-FLOP :

A toggle flip-flop structure is realized by interconnecting the "D" input to the \bar{Q}_i output of a "D" master slave flip-flop. The clock controls all the transmission gates of the flip-flop. This interconnexion ensures that the Q output at the $n+1$ clock pulse is always the complement of the D_n input. Therefore :

$Q_{n+1} = \bar{Q}_n$, which confirms that the toggle flip-flop does provide a divide-by-2 function.

Figure 4.47 represents the logic diagram of the toggle flip-flop.

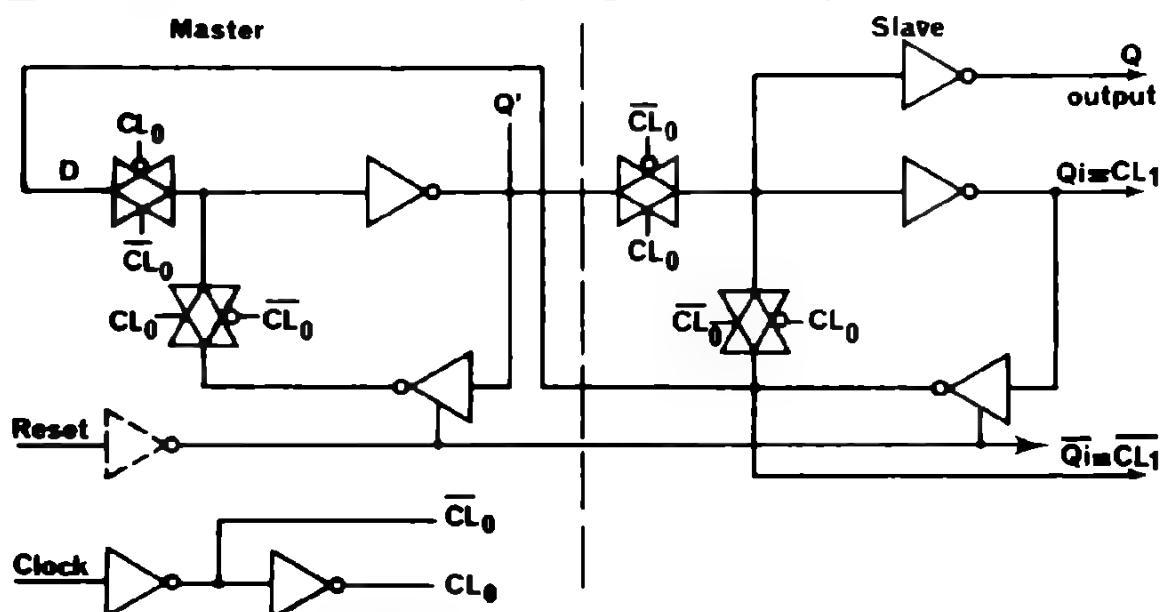


Fig. 4.47 LOGIC DIAGRAM OF THE TOGGLE FLIP-FLOP USED IN RIPPLE COUNTER

The Q_i and \bar{Q}_i outputs form the phases of the clock, which may be applied to the next divider stage in case of a ripple counter structure. The main reset input forces a "1" into the feedback inverters.

TOGGLE ENABLE FLIP FLOP :

The toggle enable flip-flop is of similar configuration to the standard toggle flip-flop. The main difference here is that the clock input is additionally gated by a toggle enable input, which, depending on its logic value, controls the clock signal applied to the transmission gate of the flip-flop. This configuration is preferably used for the flip-flops in presettable and programmable counter structures, because it requires fewer external gates.

Figure 4.48 illustrates the logic diagram of a toggle enable flip-flop.

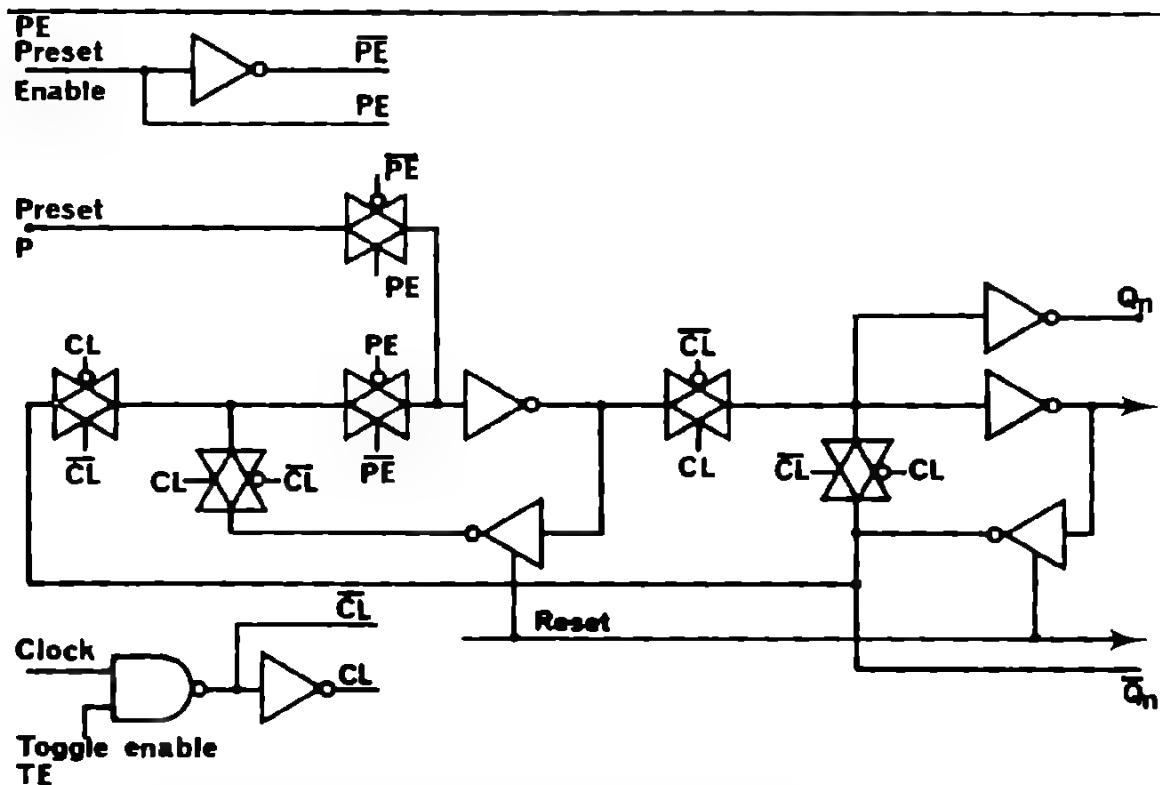





Fig. 4.48 LOGIC DIAGRAM OF A TOGGLE ENABLE & PRESET FLIP-FLOP USED IN PROGRAMMABLE COUNTERS

It should also be mentioned that usually this flip-flop structure has preset and reset enable control, which allows the flip-flop to be preset by means of additional gating.

The main reset control is similar to the previously described flip-flops.

The functional truth table is :

FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	TOGGLE ENABLE	Q_{n+1}
1	X	X	Parallel In
0		0	Q_n
0		1	Q_n
0		X	Q_n

X = Don't Care

When the toggle enable input is high, the truth table indicated for the toggle flip-flop also applies here.

2. 4. 3. Synchronous counters - Dual B C D UP Counter MC 14518 and Dual Binary Up Counter MC 14520.

Each counter module consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition, as required, when cascading multiple stages. Each counter can be cleared by applying a high level on the reset line.

Figure 4.49 and 4.50 show the logic diagram of the counters MC 14518 and MC 14520 respectively :

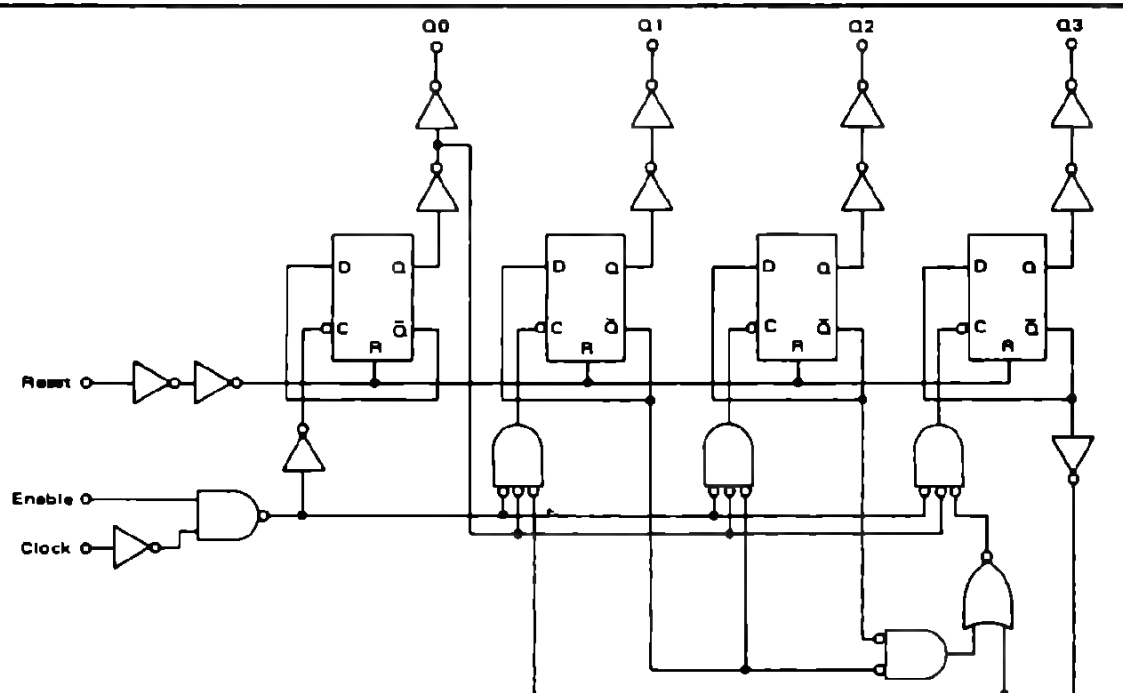
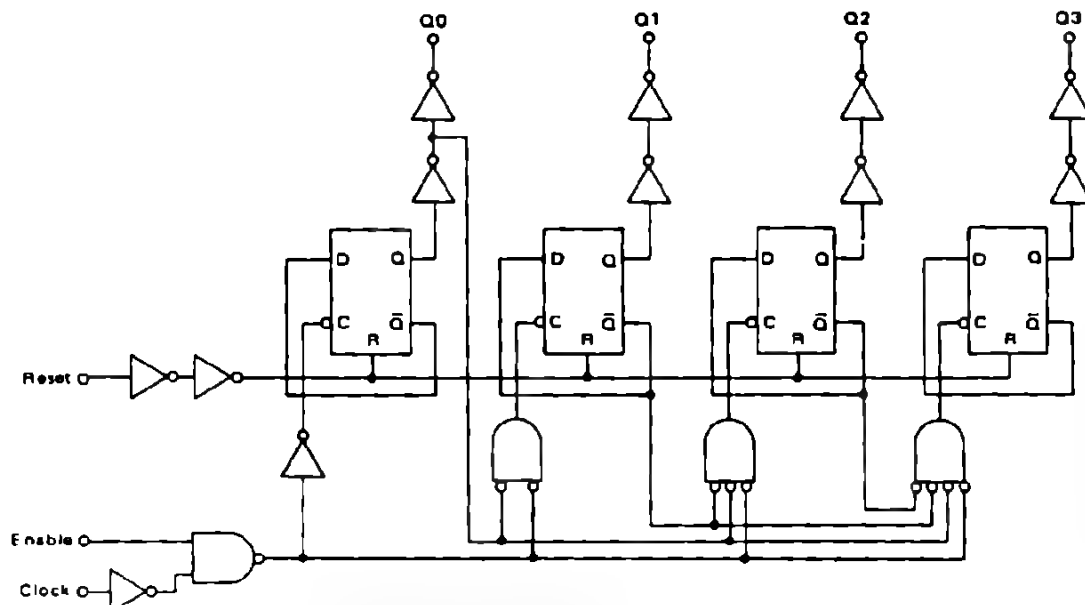


Fig. 4.49 LOGIC DIAGRAM OF THE DECADE COUNTER MC 14518
(1/2 OF DEVICE SHOWN)



**Fig. 4.50 LOGIC DIAGRAM OF THE BINARY COUNTER MC 14520
(1/2 OF DEVICE SHOWN)**

The truth table shown below applies for both types of counters.

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

It should be mentioned that the counters may be incremented on the Clock positive transition or on the Enable negative transition.

This feature is particularly useful when cascading the counters. Usually cascading is required to increase the total counter capacity. Several counters can be connected in cascade as indicated in Figure 4.51, their interconnexion diagram applies for both BCD and Binary counters.

The counting capacity X is equal to :

$X = 10^n$ for the decade counters

$X = 16^n$ for the Binary counters

n = number of counters

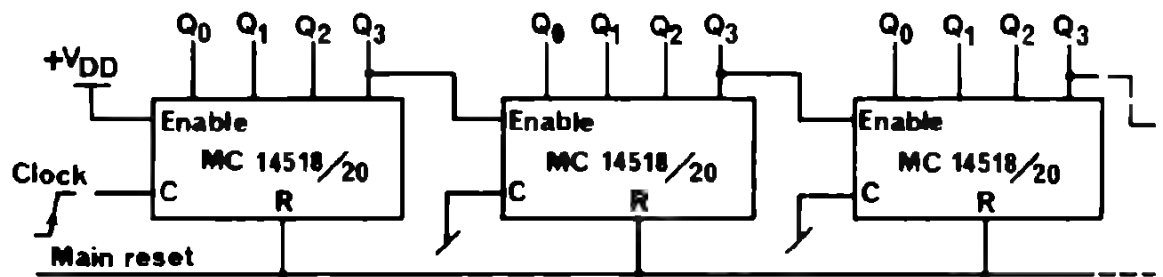
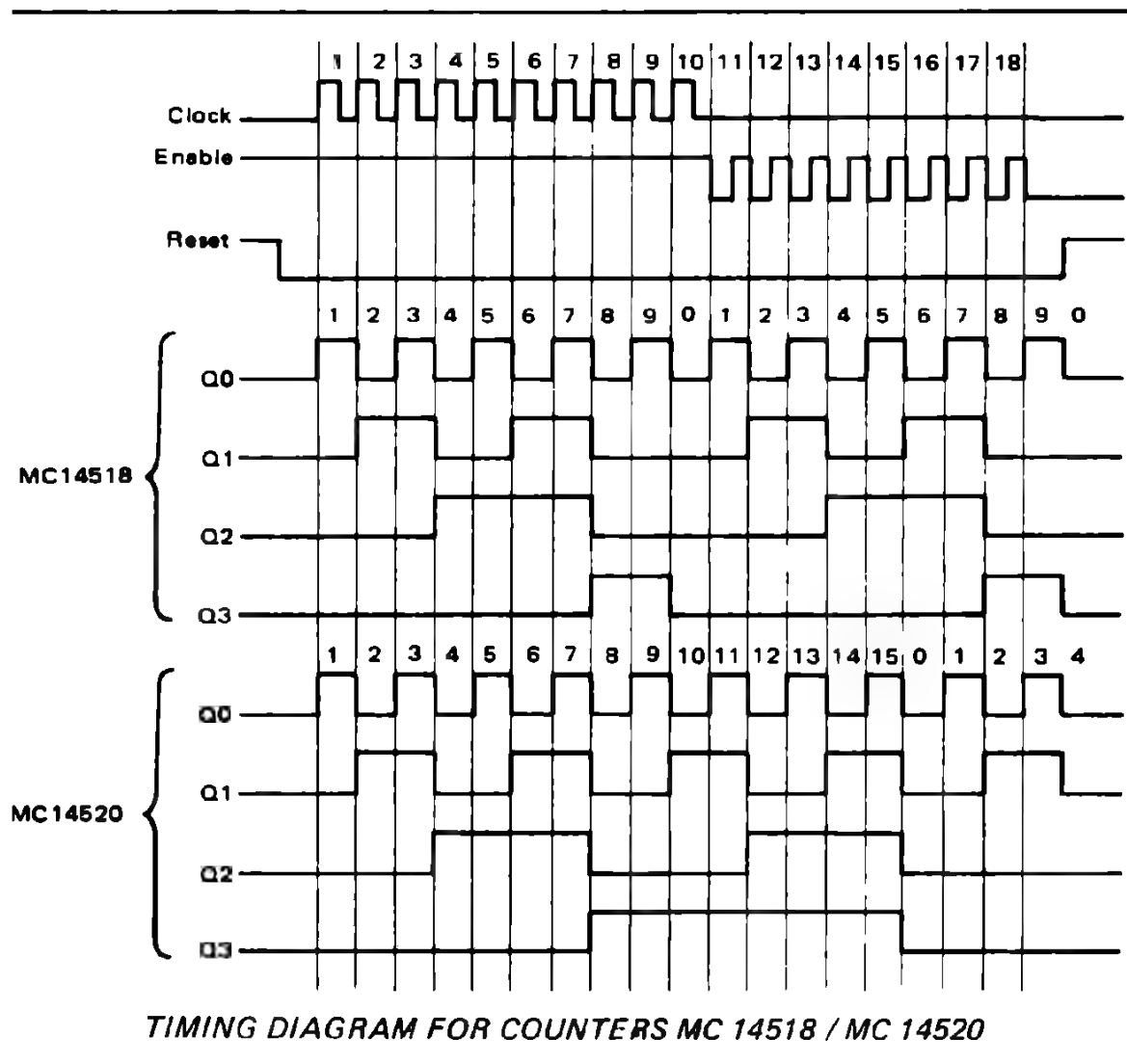


Fig. 4.51 INTERCONNECTION DIAGRAM FOR CASCADING COUNTERS MC 14518 or MC 14520

By considering the timing diagram, it can be seen that to increment the count, the enable input of the first counter has to be at "1".

The following counters are then incremented through the enable input by Q_3 outputs of the preceding counter, during its negative transition.

The main reset is provided by paralleling all the reset inputs of each counter.



TIMING DIAGRAM FOR COUNTERS MC 14518 / MC 14520

OCTAL AND DECADE JOHNSON COUNTERS MC 14022 & MC 14017

High speed operation and spike-free decoded outputs are the principal features of the Johnson counters. The octal counter (MC 14022) is composed of 4 D master-slave flip-flops, connected in cascade. The decade counter is composed of 5 stages.

The output decoding requires only two input gates, due to the nature of the Johnson Code. Normally, the outputs are low, with the exception of the one decoded state, which is high.

Both Clock and Clock enable inputs are provided. This feature allows the counters to be incremented either by the Clock positive transition or by the Clock enable negative transition.

For cascading purposes, a carry out is provided :

Figure 4.52 and 4.53 illustrate the logic diagram of the octal counter MC 14022 and the decade counter MC 14017 respectively.

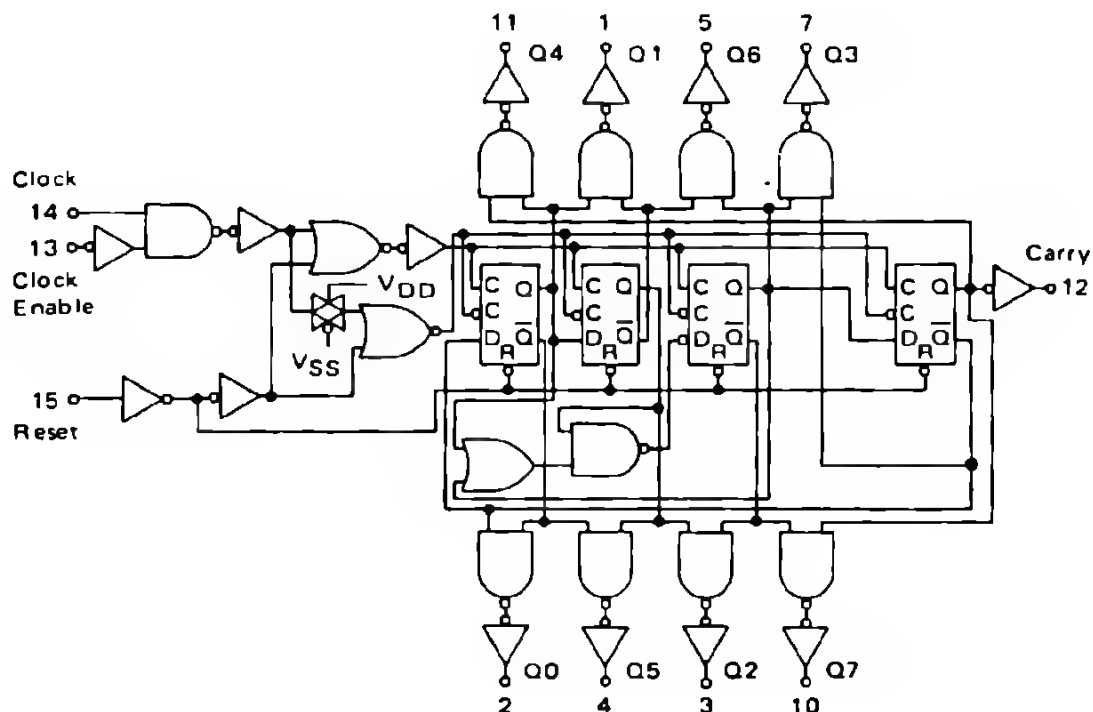


Fig. 4.52 LOGIC DIAGRAM OF THE OCTAL COUNTER MC 14022

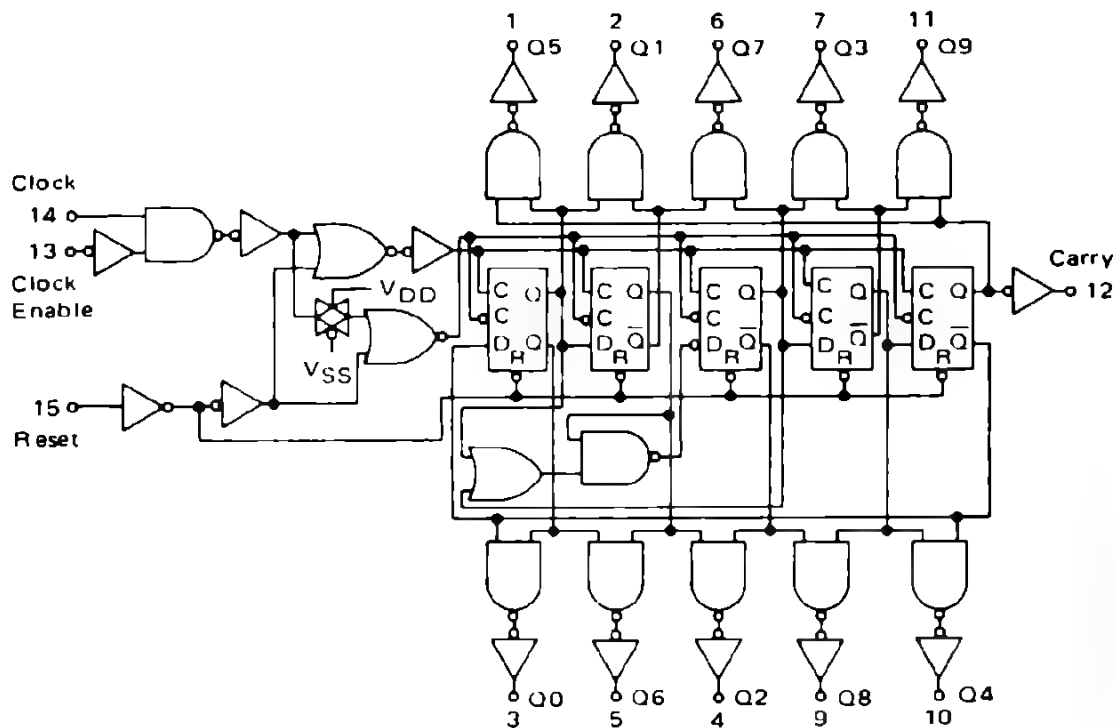


Fig. 4.53 LOGIC DIAGRAM OF THE DECADE COUNTER MC 14017

e functional truth table valid for both counters is :

FUNCTIONAL TRUTH TABLE
(Positive Logic)

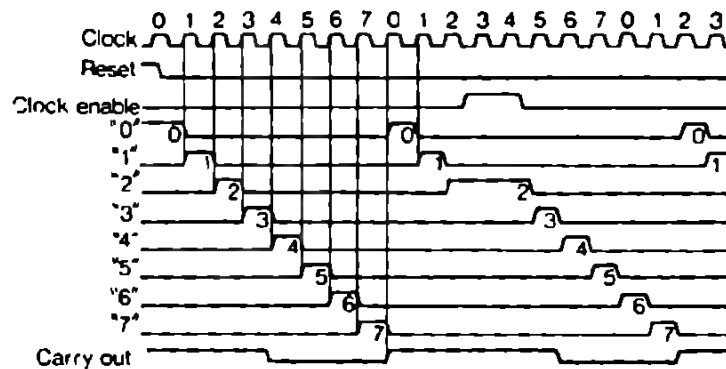
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
1	1	0	n
1	0	0	n+1
1	1	0	n
1	1	0	n+1
1	1	0	n
X	X	1	Q0

X = Don't Care

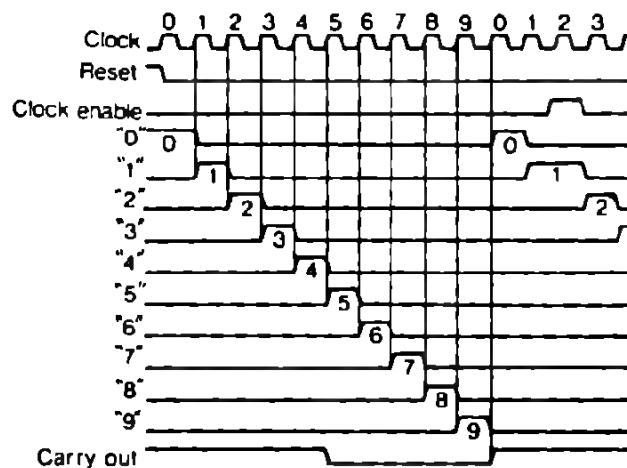
Carry = 1 if n < 4 for MC 14022

Carry = 1 if n < 5 for MC 14017

the timing diagrams for both counters are represented below :



Timing diagram of the octal counter MC 14022



Timing diagram of the decadecounter MC 14017

Figure 4.54 indicates the interconnexion diagram of Johnson counters when cascading is required.

When cascading, the total counter capacity X is given by :

$= 8^n$ when using Octal counter

$= 10^n$ when using decade counter.

$=$ number of counters connected in cascade.

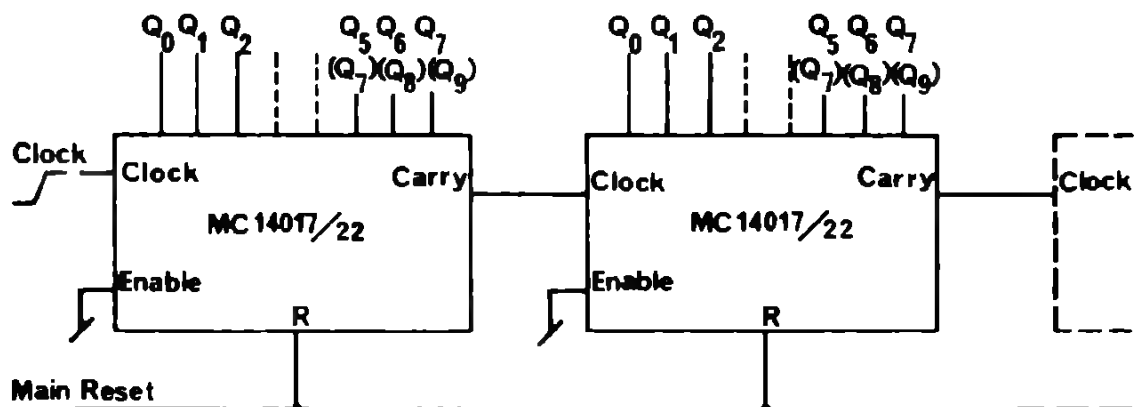


Fig. 4.54 INTERCONNECTION DIAGRAM OR CASCADING JOHNSON COUNTERS MC 14017 OR MC 14022

C D AND BINARY UP/DOWN COUNTER MC 14510 & MC 14516

The presettable B C D and binary up/down counters are, in principle, composed of 4 basic counter cells, with additional gating providing the required up/down and cascading functions.

The B C D up/down counter uses 4 "D" master slave flip-flops.

The binary up/down counter uses 4 toggle enable flip-flops.

The preset variable, applied to the preset inputs is transferred to the counter cells by means of the preset enable input. Selection of up or down counting mode is controlled by the up/down input.

For cascading purposes, a carry "input" and a carry "output" are also provided.

The control action of the carry input is:

$\text{Carry in} = 0 \longrightarrow$ counter enable

$\text{Carry in} = 1 \longrightarrow$ counter disable

The carry output depends on the counter content and is given by:

in up counting state:

$$\text{Carry out} = \overline{Q_1} \cdot Q_2 \cdot Q_3 \cdot Q_4.$$

in down counting state:

$$\text{Carry out} = \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{Q_4}.$$

Figure 4.55 and 4.56 show the logic diagram of the up/down counter MC 14510 and MC 14516 respectively.

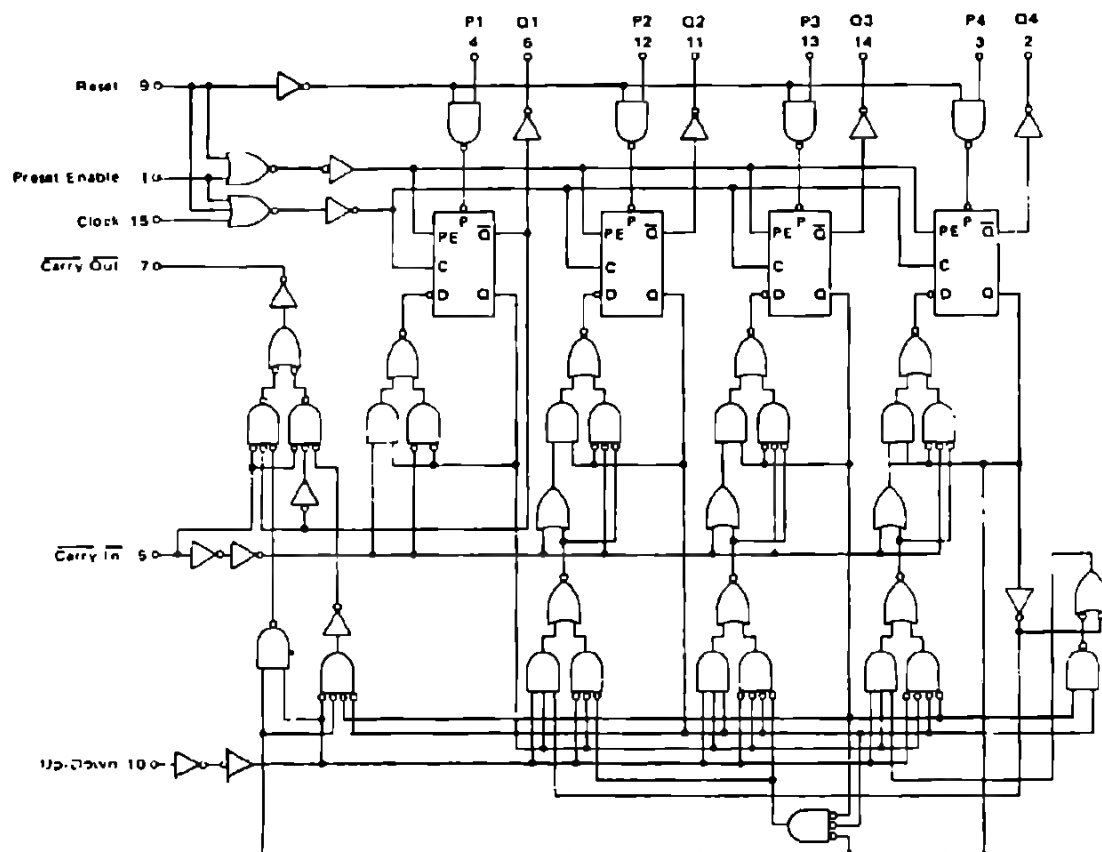


Fig. 4.55 LOGIC DIAGRAM OF THE BCD PRESETTABLE UP/DOWN COUNTER MC 14510

The following asynchronous truth table defines the operation mode for both counters.

TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

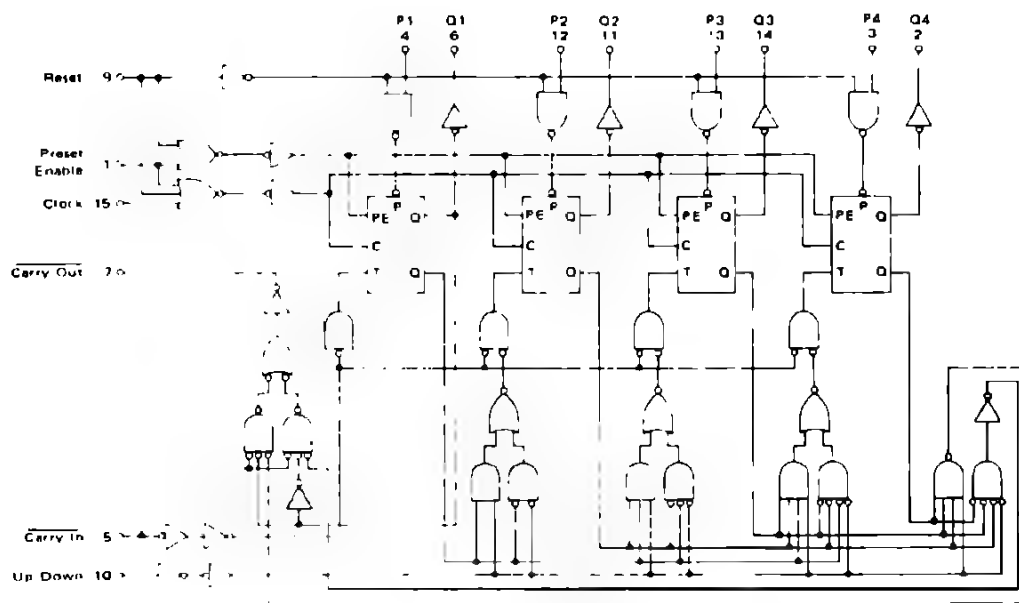
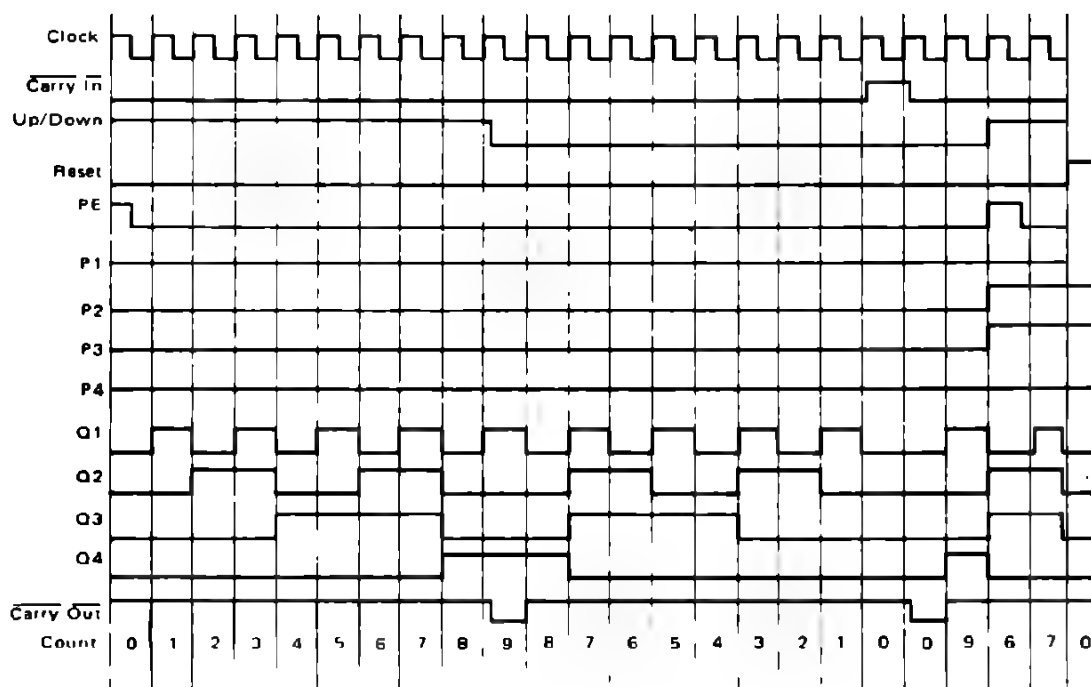
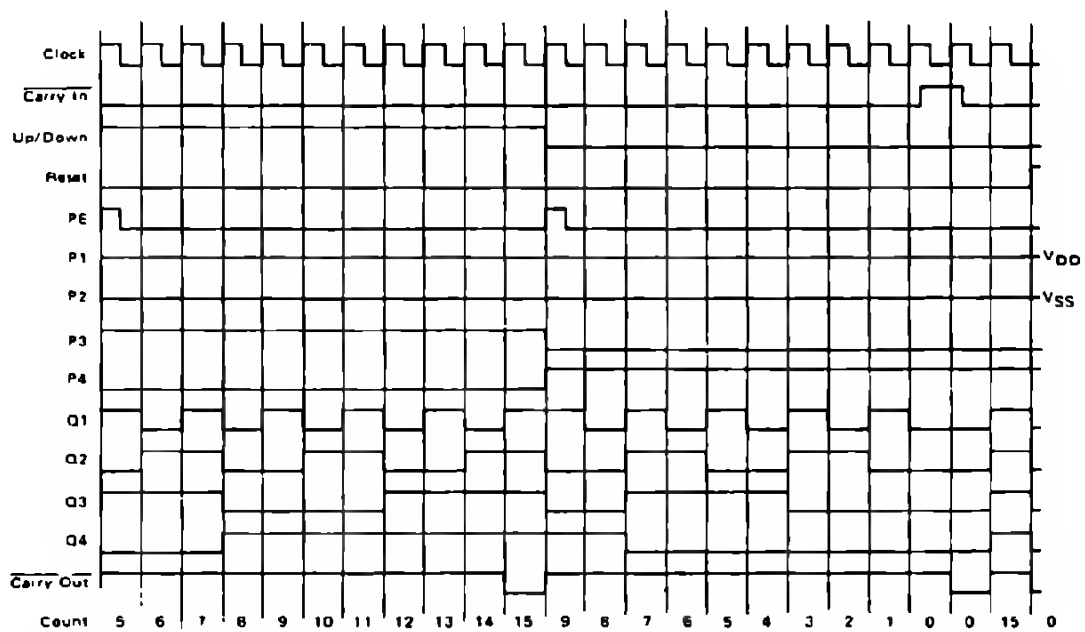


Fig. 4.56 LOGIC DIAGRAM OF THE BINARY PRESETTABLE UP/DOWN COUNTER MC 14516



TIMING DIAGRAM FOR COUNTER MC 14510



TIMING DIAGRAM FOR COUNTER MC 14516

The above illustrated timing diagrams shows the counter states in the different operation sequences.

Cascading the counters requires the interconnexions of the carry output from one counter to the following counter's carry input. The Clock is applied synchronously to all counters in the counting chain.

The following Figures 4.57: 4.58: 4.59: illustrate the interconnexions required to realize a presettable cascaded up/down counter, a presettable cascaded one cycle down counter to "0" and a programmable frequency divider.

Count

Fig. 4.57

PRESETTABLE CASCADED UP/DOWN COUNTER USING MC 14510 OR MC

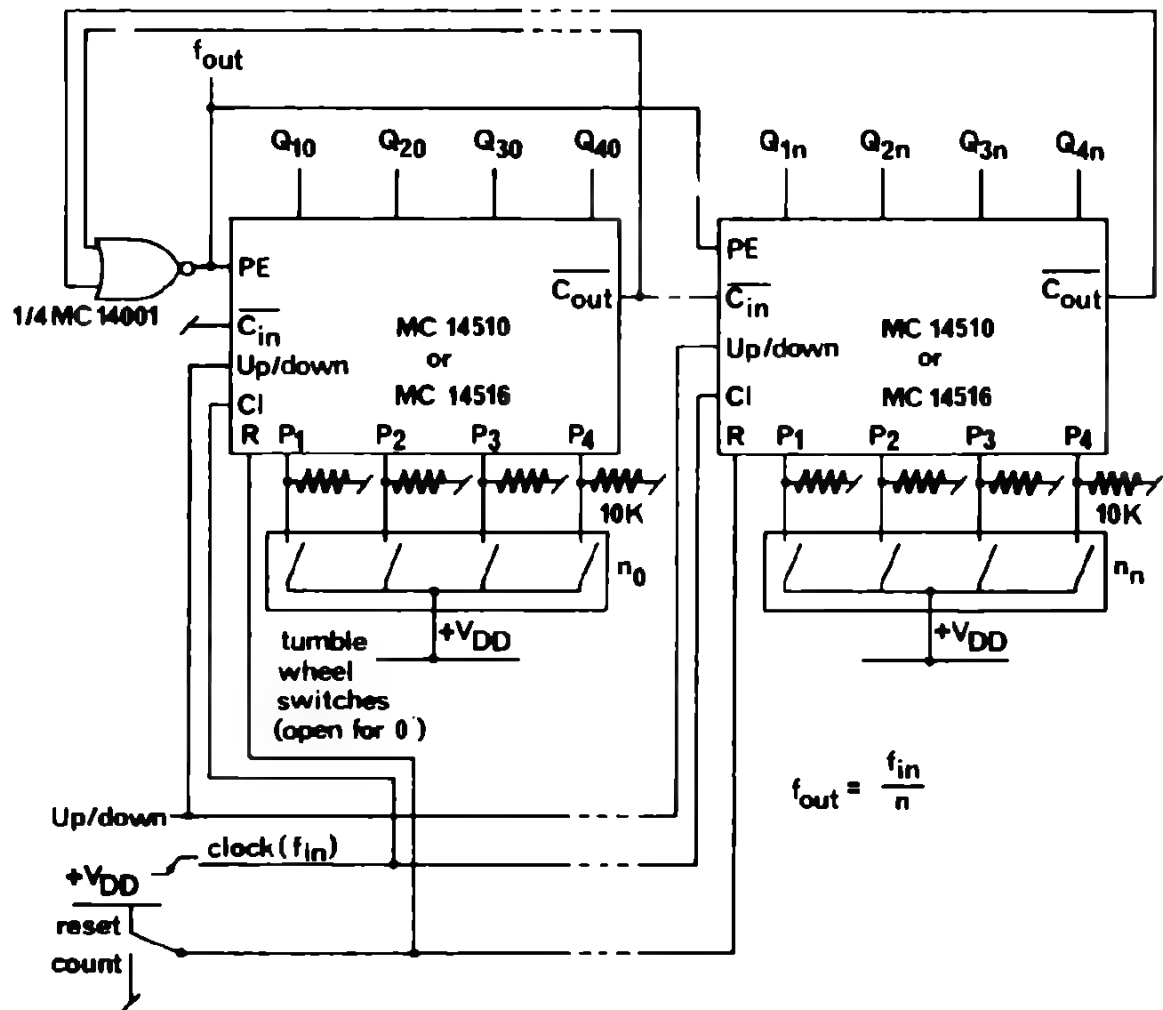


Fig. 4.59 PROGRAMMABLE CASCADED FREQUENCY DIVIDER USING MC 14510 OR MC 14516

PROGRAMMABLE DIVIDE BY N – 4-BIT COUNTERS MC 14522 & MC 14526

The programmable divide – by – N counters are, in principle, down counters and are composed of 4 toggle enable flip-flops with associated additional gating to provide the down counting mode and the possibility of cascading several counters without external gates.

Two types of counters are available:

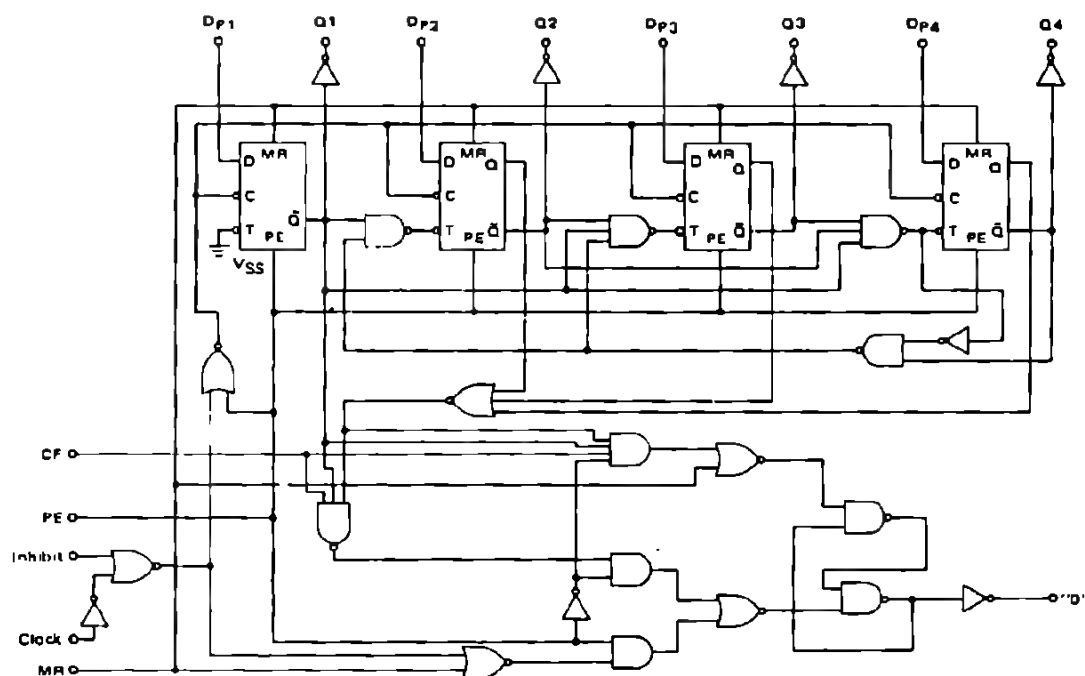
- A BCD programmable counter MC 14522
- A Binary programmable counter MC 14526

The programming is achieved by applying the preset variable to the Dp inputs; this is transferred to the counter cells by the presettable (PE) input control.

The clock inhibit allows the counters function to be disabled, the Master reset (MR) provide synchronous initiation of the divide – by – N cycle.

Cascade feedback (CF) input and "0" output are provided for cascading purposes.

figure 4.60 and 4.61 illustrate the logic diagram of the counter MC 14522 and C 14526 respectively.



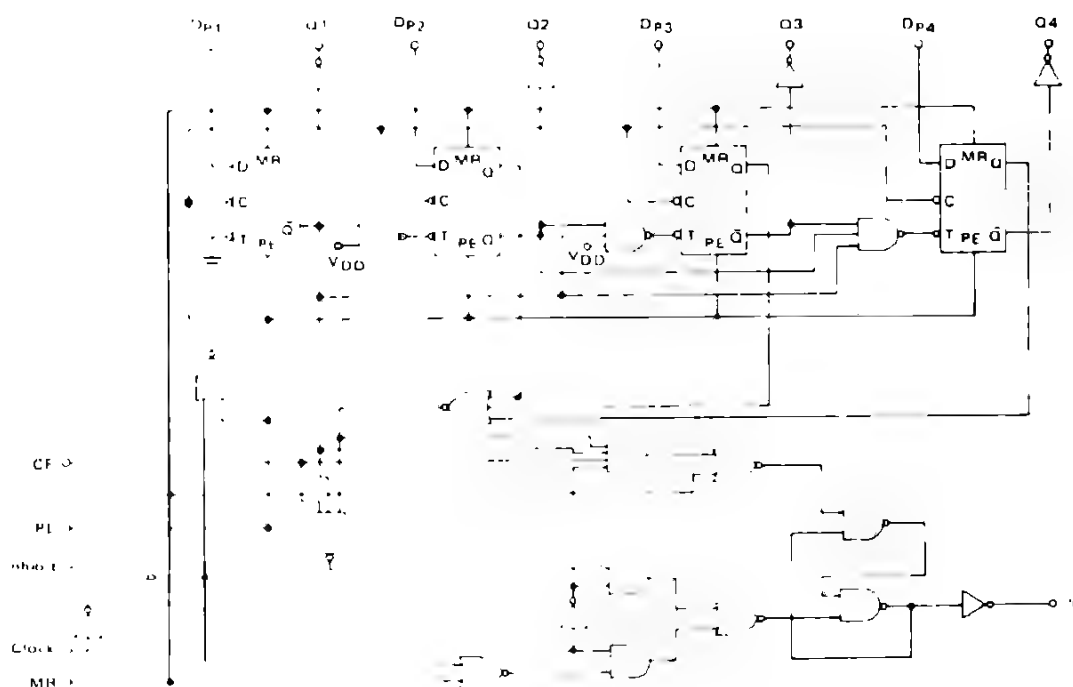


Fig. 4.61 LOGIC DIAGRAM (BINARY DIVIDE-BY-N COUNTER) MC 14526

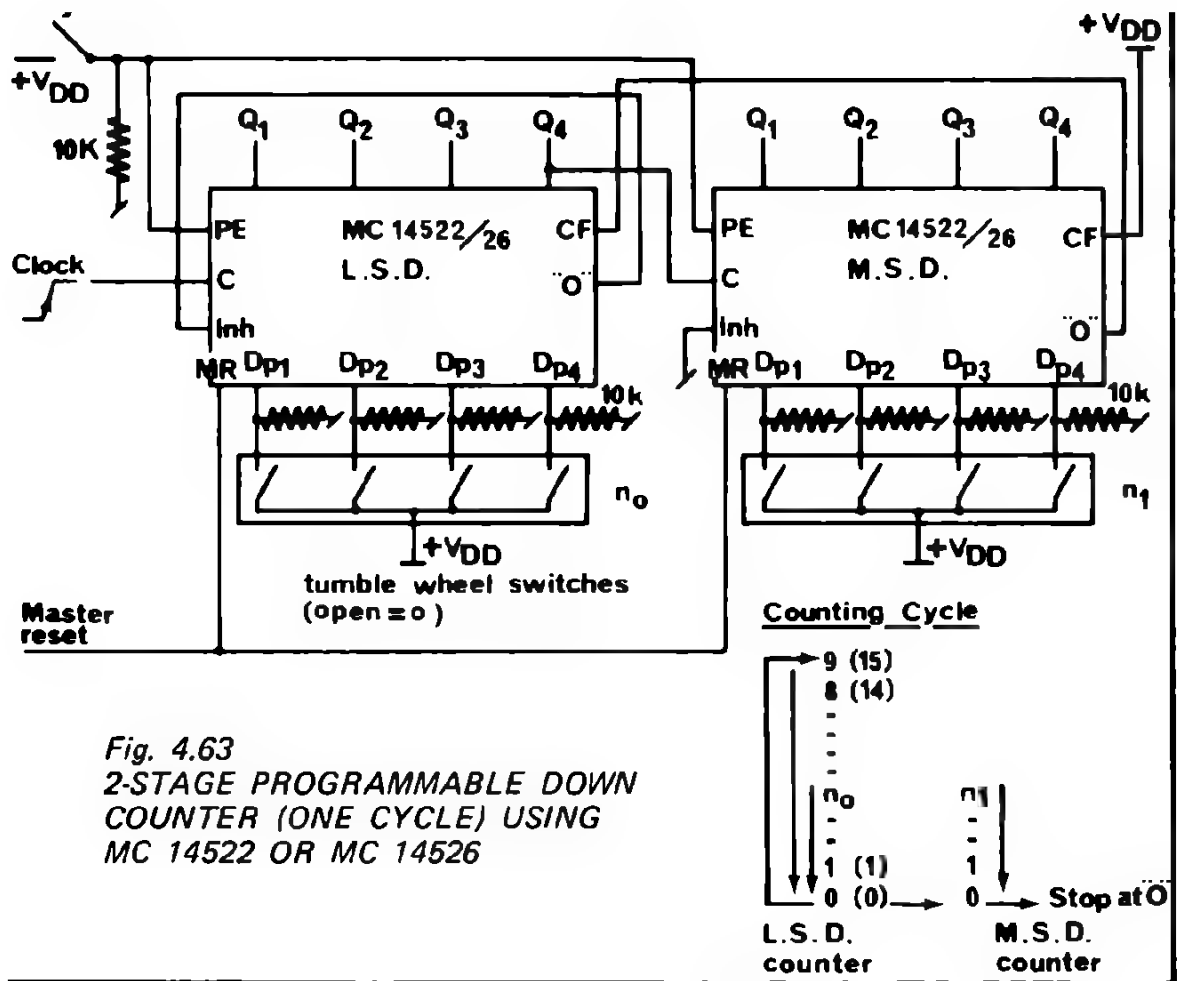
The functional truth table is:

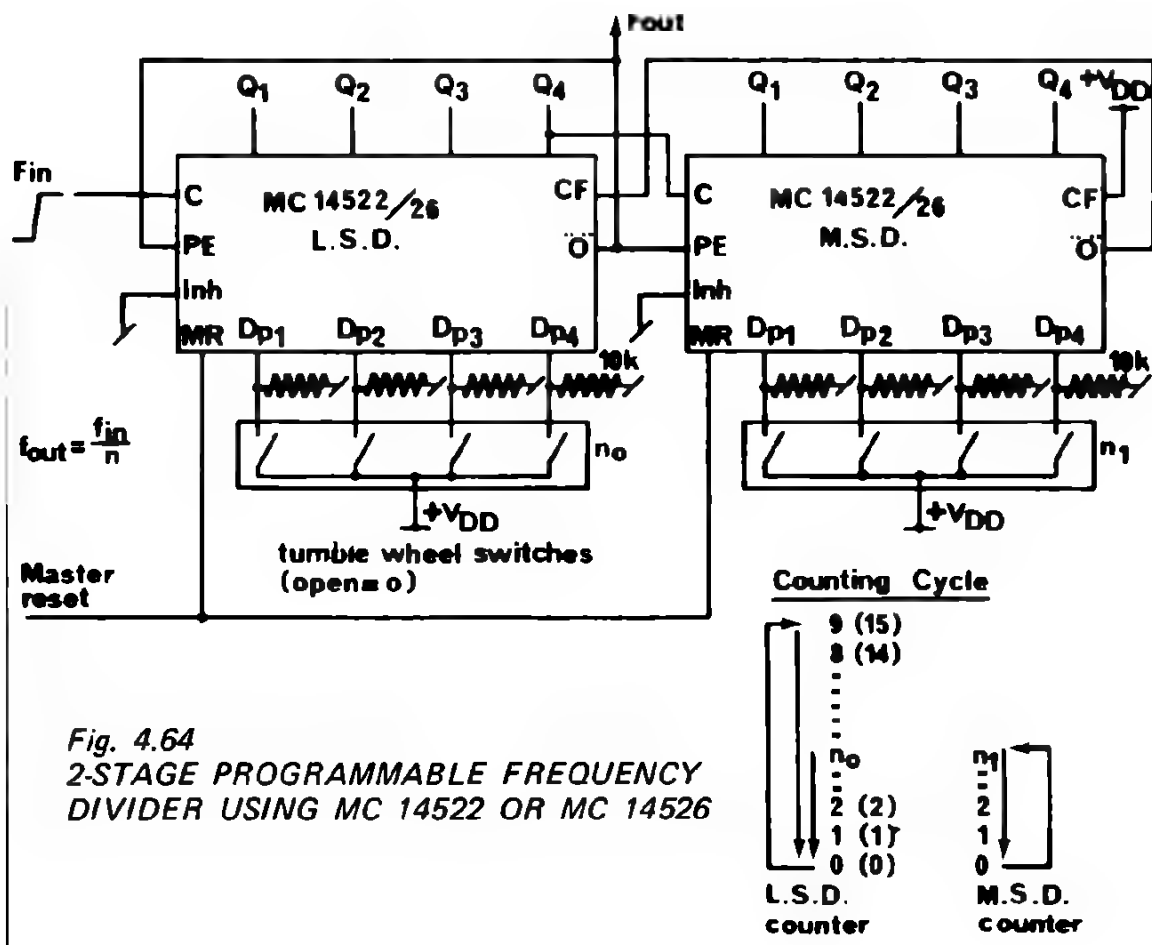
Clock	Inhibit I	Preset enable PE	Master enable Reset	action
0	0	0	0	No Count
	0	0	0	Count-1
X	1	0	0	No Count
X	X	1	0	Preset
X	X	X	1	reset

The counting capacity can easily be increased by using the cascading features provided internally in the counters.

In the cascade connected configuration (Figure 4.63), the operation mode is the following:

- the number preset at the input is introduced into the counter chain, when all counters are "zero",
- then the L.S.D. counter is decremented at each positive clock transition
- when the zero state of L.S.D. counter is reached, and the next cycle length of this counter will be 10 for the BCD count or 16 for the Binary.
- At each transition from 0 to 9 (or 0 to 15) of the L.S.D. counter will decrement one counting unit of next counter.
- When the "0" output of all counters connected in the chain are "0" which is also controlled by the cascade feedback input, the "0" output of the L.S.D. counter will detect this last state and preset the predetermined number again into the counter chain, (the "0" output of the L.S.D. counter is connected to all preset enable inputs).





2. 4. 4. Asynchronous counters

Ripple counters are very often used in frequency divider applications and are in principle asynchronous counters.

The basic structure of ripple counters is a chain of interconnected toggle flip-flops, which require no additional gating functions, and are usually up counters.

The clock and its complement are always generated by each flip-flop and these control the transmission gates of the next flip-flop stage. Each counter stage takes a divide-by-2, with a duty cycle of 50%.

EVEN STAGE RIPPLE COUNTER – MC 14024

Composed of seven toggle flip-flops, connected as a binary ripple carry counter with an input pulse shaping circuit, the MC 14024 is mainly intended for frequency division applications.

A main reset is also provided. All inputs and outputs are buffered to obtain maximum noise immunity.

Figure 4.65 represents the logic diagram of the MC 14024.

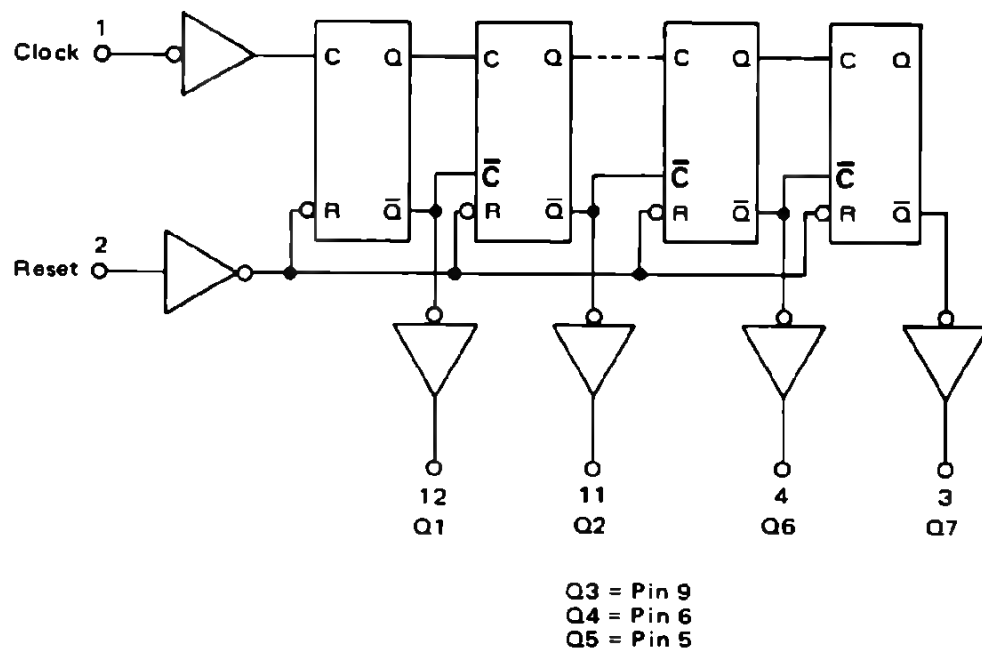




Fig. 4.65

LOGIC DIAGRAM OF THE SEVEN STAGE RIPPLE COUNTER MC 14024

The truth table is:

Clock	Reset	State
0	0	no change
	0	no change
1	0	no change
	0	count +1
X	1	All outputs low

X = don't care

The counter is incremented by the negative clock transition. The timing diagram is shown in Figure 4.66. It should be noted that when used in cascaded configuration, the Q_7 output can be used directly as the clock for the next counter stage (the 128th falling edge).

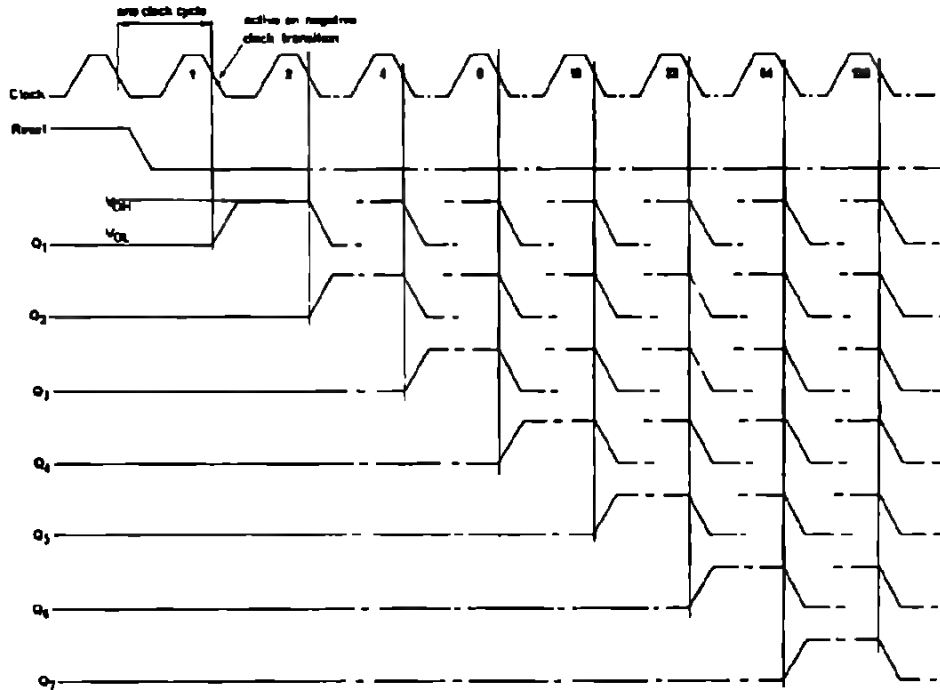


Fig. 4.66 TIMING DIAGRAM OF THE MC 14024

Figure 4.67 represents an example of cascading counters to give a division capacity of 2^{21} (2,097,152).

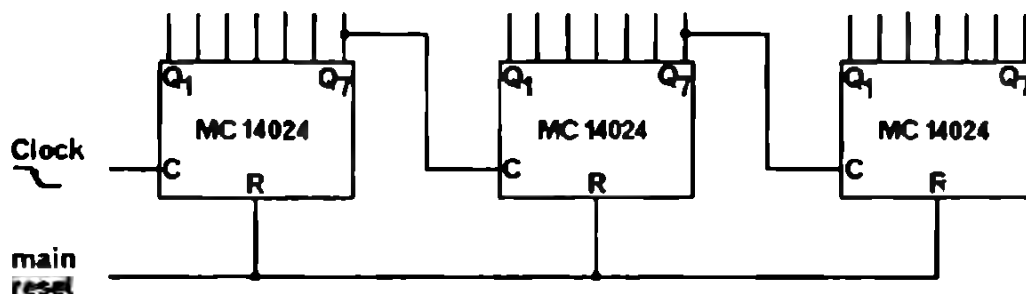


Fig. 4.67 CASCADED RIPPLE COUNTERS WITH COUNTING CAPACITY OF 2^{21} USING 3 x MC 14024

12 AND 14-BIT BINARY RIPPLE COUNTERS MC 14020 & MC 14040

Composed of toggle flip-flops connected as a binary ripple carry counter, fully static, and also including a pulse shaping circuit, these circuits are intended for frequency division applications. All inputs and outputs are buffered to obtain maximum noise immunity. A main reset input is also provided.

The device MC 14020 is a 14 stage ripple carry counter with maximum division capacity of 2^{14} (16,384).

The device MC 14040 is a 12 stage ripple carry counter with maximum division capacity of 2^{12} (4,096).

For the device MC 14020 connections to outputs Q_1 , Q_4 to Q_{14} are provided and for the device MC 14040 all outputs Q_1 to Q_{12} are available.

Figure 4.68 illustrates the logic diagram of the counters MC 14020 and MC 14040.

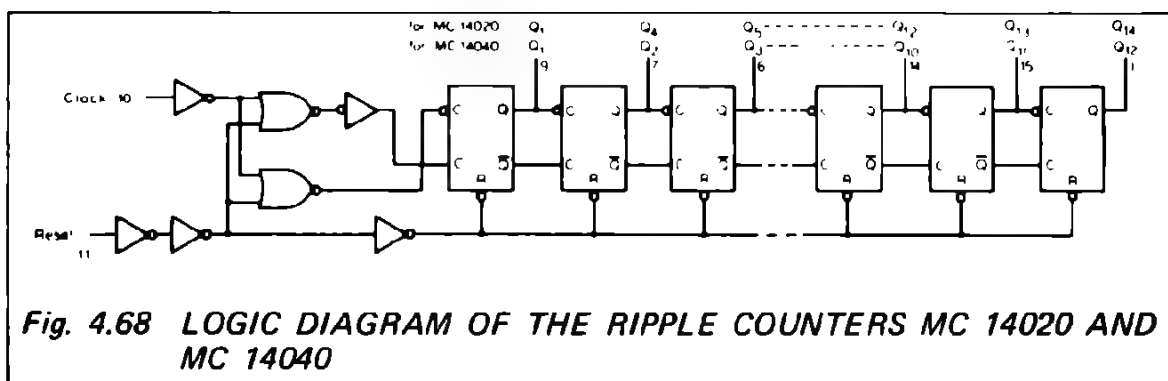


Fig. 4.68 LOGIC DIAGRAM OF THE RIPPLE COUNTERS MC 14020 AND MC 14040

The truth table is:

TRUTH TABLE		
CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

It should be mentioned that the counter is incremented by negative transitions of the clock, which allows easy interconnexion of counters when cascading is required (as shown in Fig. 4.67).

24 BIT COUNTER / TIMER MC 14521 – (preliminary information)

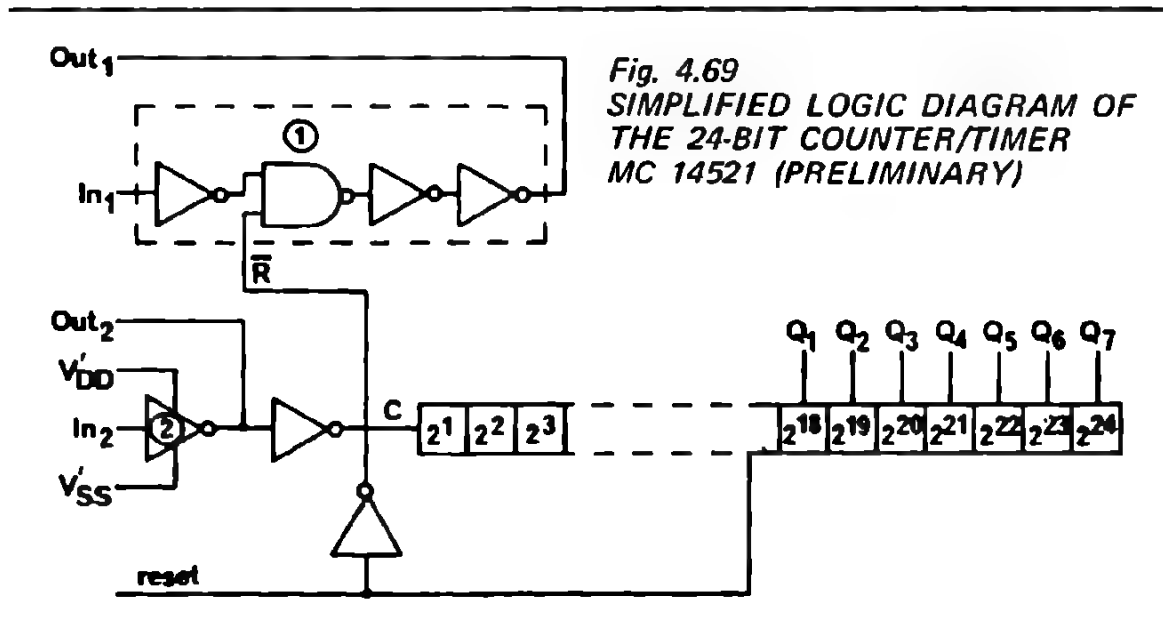
Composed of 24 flip-flop stages and an internal oscillator, this counter will divide by 2^{24} (16,777,216). Two accessible amplifiers are provided in the module so that by adding external RC elements or crystal, the time base for the counters section may be generated.

The outputs of the last 7 stages of this counter are available, providing the following division factors:

Outputs	$Q_1 = 2^{18} = 262.144$
	$Q_2 = 2^{19} = 524.288$
	$Q_3 = 2^{20} = 1.048.576$
	$Q_4 = 2^{21} = 2.097.152$
	$Q_5 = 2^{22} = 4.194.304$
	$Q_6 = 2^{23} = 8.388.608$
	$Q_7 = 2^{24} = 16.777.216$

A main reset which resets all counter stages to "0" is also provided.

Figure 4.69 illustrates the logic diagram of the 24 stage counter MC 14521.



An oscillator is realized by interconnecting the amplifier ① and ② as shown in Figure 4.70a and b with external RC elements or a crystal. For the operation of the oscillator reference to chapter 8 should be made. It should be mentioned that the amplifier ② has separate power supply inputs V'_{DD} V'_{SS} . The resistors R_s in series with V_{DD} and V_{SS} gives the possibility of reducing the power consumption of the crystal oscillator configuration.

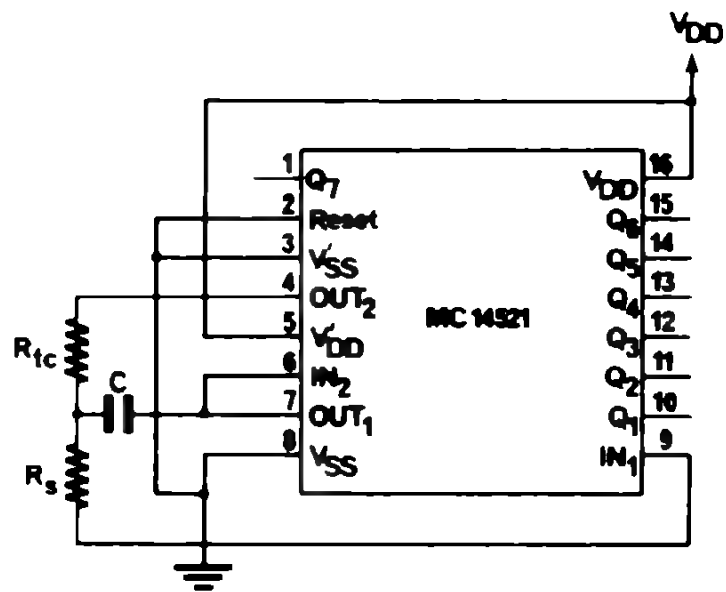
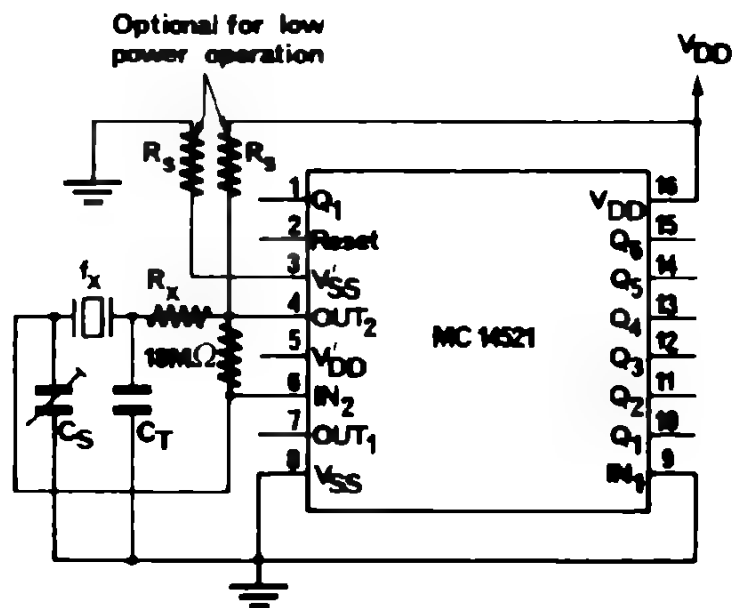


Fig. 4.70a RC OSCILLATOR CONFIGURATION



f_x	R_x	C_T	C_S	Xtal cut
50 KHz	6.3 KΩ			M
500 KHz	1 KΩ	100 pf	42 pf	AT
10 MHz	5 Ω			S

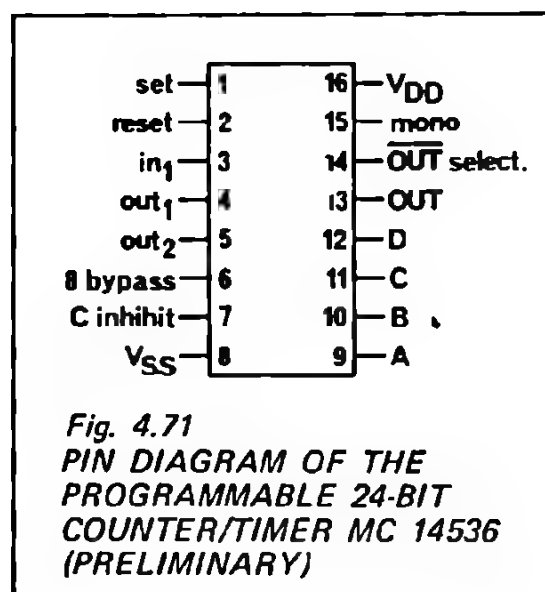
Fig. 4.70b CRYSTAL OSCILLATOR CONFIGURATION

D	C	B	A	Stage selected	Division factor
0	0	0	0	9	512
0	0	0	1	10	1.024
0	0	1	0	11	2.048
0	0	1	1	12	4.096
0	1	0	0	13	8.192
0	1	0	1	14	16.384
0	1	1	0	15	32.769
0	1	1	1	16	65.536
1	0	0	0	17	131.072
1	0	0	1	18	262.144
1	0	1	0	19	524.288
1	0	1	1	20	1.048.576
1	1	0	0	21	2.097.152
1	1	0	1	22	4.194.304
1	1	1	0	23	8.388.608
1	1	1	1	24	16.777.216

PROGRAMMABLE 24-BIT COUNTER/TIMER MC 14536 (preliminary information)

Composed of 24 flip-flop stages connected in cascade with a maximum counting capacity of 2^{24} (16.777.216) an internal oscillator and an output selection logic, this counter can be used where the division factor has to be programmed. A 4-bit binary word, applied to the control inputs A, B, C, D, selects 1 of the last 16 counter stages, thereby allowing the division factor to be programmed.

The table indicates the relation between the program word and the division factor obtained.



By using the "8 bypass" input, the first 8 flip-flops can be eliminated (in a logic sense), which then gives a 16 stage counter fully programmable from 2^0 to 2^{16} .

Access to two amplifiers is also provided, so by adding external components (RC or crystal) the internal time base may be generated. Clock inhibit, direct set, and "true"/"complement" control of the output is also provided. Figure 4.71 illustrates the pin diagram of the programmable 24-bit counter/timer MC 14536.

CHAPTER 5

Complex functions

- 5.1.1. SIMPLE ADDERS
- 5.1.2. COMPARATORS
- 5.1.3. ARITHMETIC LOGIC UNIT
AND LOOK-AHEAD BLOCK
- 5.2.1. READ-WRITE MEMORY
- 5.2.2. READ-ONLY MEMORY
- 5.3.1. THE MAJORITY-LOGIC
FUNCTION
- 5.3.2. INVERTING OUTPUT
- 5.3.3. APPLYING THE DUAL
M₅ GATE
- 5.3.4. MORE CORRELATION
- 5.3.5. THE FUTURE OF MAJORITY
LOGIC

ARITHMETIC FUNCTIONS

5.1.1. SIMPLE ADDERS

Binary or decimal arithmetic can be performed in two ways: serial or parallel.

For low speeds serial arithmetic is generally considered more economical. There the addition or subtraction is carried out bit by bit starting with the least significant bit. In the case of addition, the carry input must initially be held at zero. The carries which eventually result from the addition, must be stored and added to the next higher bits. The adders are referred to as full adders when they can handle two data bits and a carry bit from the previous position generating a sum output and a carry bit to be forced into the next higher position.

The truth table of a full adder is shown below:

A	B	Carry in	Sum	Carry out
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

The CMOS circuits MC 14032 and MC 14038 are triple full adders which have built-in flip-flops to save carry bits resulting from addition.

The logic equations are:

$$S = (A \oplus B) \oplus C_{in}$$

$$C_{out} = A \cdot B + A \cdot C_{in} + B \cdot C_{in}$$

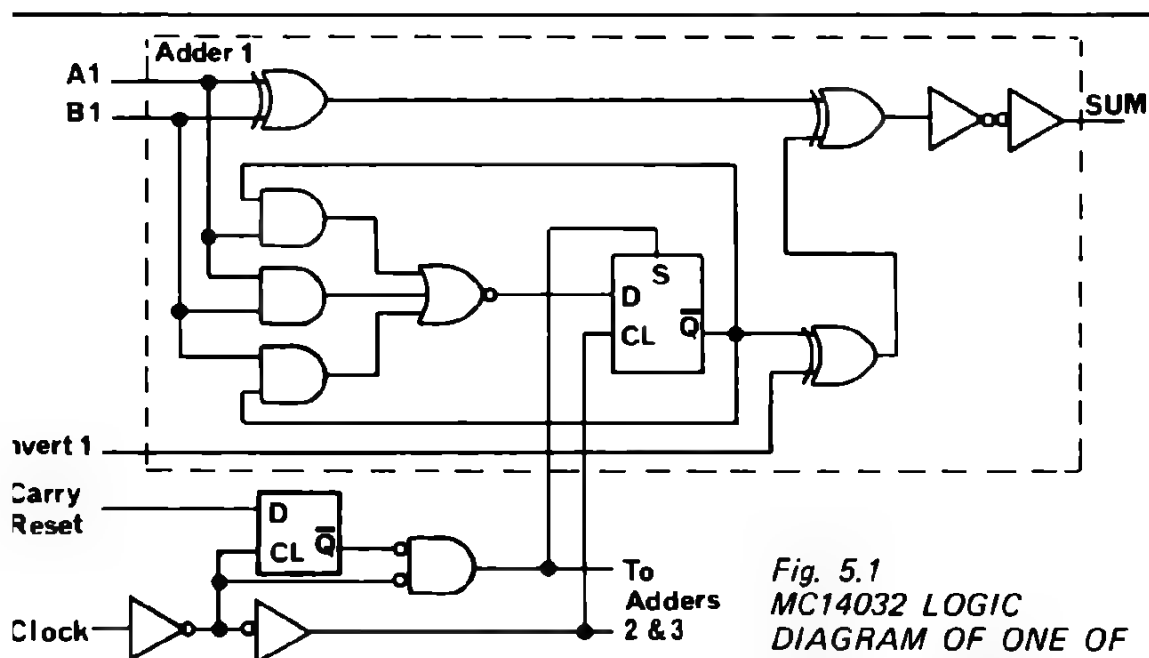


Fig. 5.1
MC14032 LOGIC
DIAGRAM OF ONE OF
THREE ADDERS

There is also a facility for resetting the carry bit at the beginning. This part of the circuit is common to all three adders (Fig. 5.1).

It can be seen from the logic diagram that an additional input has been provided. With the "INVERT" high the sum output can be complemented. This is useful when using the circuit for subtraction.

The usual way of performing a binary subtraction is by inverting the subtrahend and forcing a carry bit into the least significant position. Then, an addition is made and the resulting carry ignored.

Example:

		force carry →	1
12	1100		1100
– 7	0111	invert →	<u>1000</u>
5		result	0101

Note that the same result can be achieved when the subtrahend is inverted instead of the subtrahend. Then, a normal addition is made without forcing the carry bit into the first position. Finally the result is inverted.

Example:

12	1100	invert →	0011
– 7	0111		<u>0111</u>
			1010
		invert	↓
5		result	0101

The serial adders MC 14032 and MC 14038 operate in a clocked mode. The carry is clocked into the flip-flop at the positive-going edge of the clock for the MC 14032 and at the negative-going edge for the MC 14038. It is convenient to use the same clock edge to shift new data to inputs A and B and to take the result from the SUM output. The internal delay is sufficient to allow safe operation.

The carry flip-flop is reset to a logical "0" when a high level is applied to the CARRY RESET input at the clock transition.

Whenever high speed is important parallel addition should be considered.

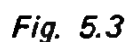
The MC 14008 is a four bit full adder with a fast parallel-carry-out stage. This permits high speed operation in arithmetic sections using several adders. The sum is calculated in less than 150 ns typical with $V_{DD} = 15V$. The carry output is even faster.

Besides the typical and well known applications in arithmetic units, there is an interesting possibility to use this circuit for counting.

The schematics is given in Figure 5.2.



he stages may be cascaded but propagation time for the addition must be considered. The minimum counting period is given by the sum of the propagation times from the clock inputs to the Q outputs, from the input of the adders to their outputs and the set-up time of the flip-flops. Instead of discrete flip-flops, a memory array can be used. A single adder can serve many memory locations.



The described configuration is useful whenever great flexibility is needed. For simple up/down counting the MC 14516 circuits would be more economical to use.

5.1.2. COMPARATORS

The adders can also be used to compare numbers. Two numbers are subtracted from each other and the result will be zero if both numbers were equal. If the numbers were not equal then, the state of the carry bit shows which one is greater.

When only the comparison of two numbers is needed, the comparator circuits MC 14585 should be used. The circuits can compare two 4-bit numbers, each of them giving the outputs $A < B$, $A = B$ or $A > B$. They can be cascaded to compare numbers which are longer than 4 bits.

The schematic of the cascade is given in the data sheet. Note that the numbers to be compared need not necessarily be true binary numbers. BCD-numbers may be compared as well.

5.1.3. ARITHMETIC LOGIC UNIT AND CARRY LOOK-AHEAD BLOCK

The arithmetic logic unit MC 14581 is one of the most complex and powerful circuits in the CMOS logic family. This large scale integrated circuit has the following features:

- capability of providing 16 binary arithmetic functions and 16 functions of two Boolean variables of 4 bits each
- on-chip decoding of function
- fully static operation
- low input capacitance-5 pf typical.

Typical applications include:

- Parallel Arithmetic Units
- Process Controllers
- Remote Datalink Processing
- Graphic Display Terminals
- Flight Control Computers
- Digital Servo Control Systems.

Besides the inputs for two 4-bit words and the 4-bit function outputs, there are ripple carry input and output, a comparison output and two carry look-ahead outputs.

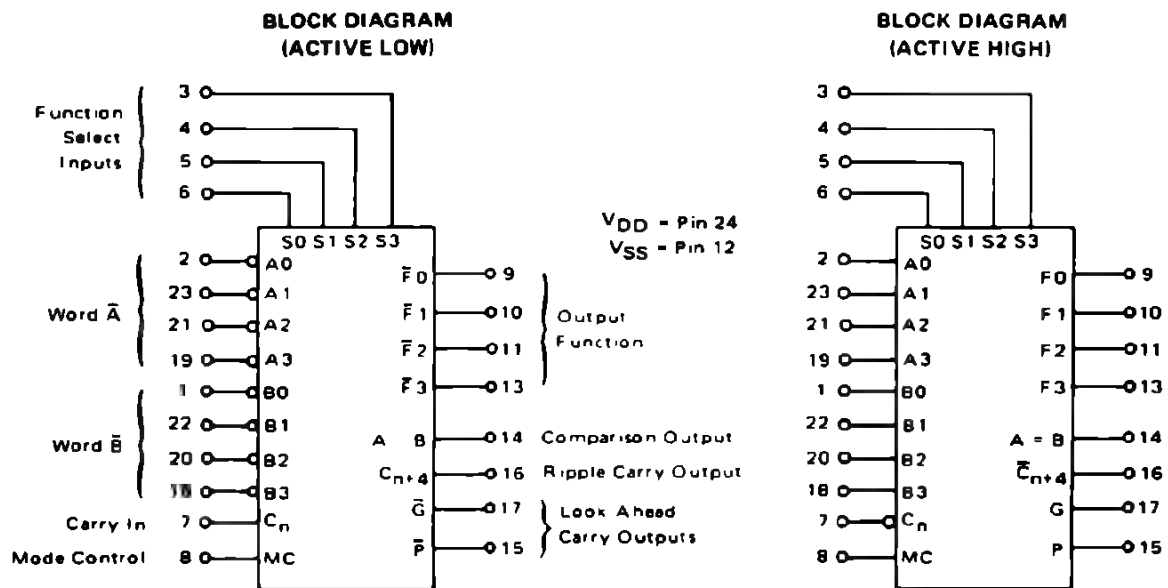
The code on the function select inputs and the level of mode control input determine the function to be performed.

Arithmetic operations are selected by applying a low level to the mode control input. The desired function is chosen by applying the appropriate binary code to the select inputs (S_0 thru S_3).

When the device is in the subtract mode (LHHL and mode bit L), comparison of two words present at A and B inputs is provided, a high level on the comparison output indicating when the two words are equal. In case that there was no equality, the carry output can be used to indicate the relative magnitude.

The truth table is given for both negative and positive logic (Fig. 5.4).

Note that the arithmetic functions always handle the carry input bit, which is added in two's complement arithmetic to the function, if present. In the logic mode (MC=H), the state of the carry input is irrelevant, since the logic function is calculated for every single pair of bits A and B.



TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
				LOGIC FUNCTION (MC = H)	ARITHMETIC* FUNCTION (MC = L, C _n = L)	LOGIC FUNCTION (MC = H)	ARITHMETIC* FUNCTION (MC = L, C _n = H)
S3	S2	S1	S0				
L	L	L	L	\bar{A}	A minus 1	\bar{A}	A
L	L	L	H	$\bar{A}\bar{B}$	AB minus 1	$\bar{A+B}$	A+B
L	L	H	L	$\bar{A}+B$	$A\bar{B}$ minus 1	$\bar{A}B$	$A+\bar{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A+B)	\overline{AB}	A plus $A\bar{B}$
L	H	L	H	\bar{B}	AB plus (A+B)	\bar{B}	(A+B) plus $A\bar{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\bar{B}$	$A+\bar{B}$	$A\bar{B}$	$A\bar{B}$ minus 1
H	L	L	L	$\bar{A}B$	A plus (A+B)	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	$A\bar{B}$ plus (A+B)	B	(A+B) plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	AB	AB plus A	$A+\bar{B}$	(A+B) plus A
H	H	H	L	AB	$A\bar{B}$ plus A	A+B	(A+B) plus A
H	H	H	H	A	A	A	A minus 1

* Expressed as two's complement

Fig. 5.4 BLOCK DIAGRAMS AND TRUTH TABLE

Example:

MC	S ₀	S ₁	S ₂	S ₃	\bar{A}				\bar{B}				C _{in}	\bar{F}			
L	H	H	H	H	L	L	H	H	X	X	X	X	L	L	L	H	H
L	H	H	H	H	L	L	H	H	X	X	X	X	H	L	L	H	L
H	H	H	H	H	L	L	H	H	X	X	X	X	X	L	L	H	H

X = Don't care

The versatility of the Arithmetic Logic Unit allows the realisation of very complex operations with a small number of packages.

Figure 5.5 shows a four bit parallel multiplier circuit. Multiplication is performed on two 4-bit words, providing an 8-bit product.

The straight-forward method is used. Each package adds the content of the word Y₀ thru Y₃ to the previous sum if the corresponding X bit is true. Shifting to the more significant positions is performed by wiring the outputs \bar{F}_1 , \bar{F}_2 , \bar{F}_3 and C_{n+4} to the next higher significant unit.

As already stated, two additional outputs: carry propagate (P) and carry generate (G), are provided on the Arithmetic Logic Unit in order to allow a look-ahead carry scheme for simultaneous carry generation for the four bits in the package. These outputs can be used with the MC 14582 as a second order look-ahead block. One MC 14582 circuit allows fast carry calculations for up to 16 bits (4 MC 14581 packages). Further details are given in the MC 14582 data sheet.

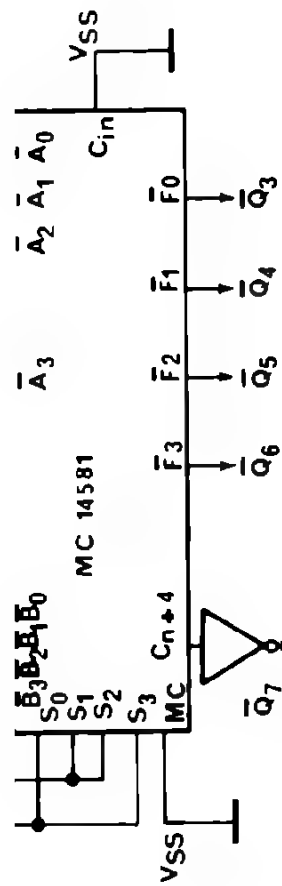


Fig. 5.5

2. MEMORIES

5.2.1. READ-WRITE MEMORY

The MCM 14505 64-bit Random access Read-Write Memory has extremely low power requirements. Unlike many other semiconductor memories the MCM 14505 is a static one. The information contained in the memory can be retained indefinitely without refreshing memory cells. This drastically reduces the amount of supporting circuitry and the quiescent power dissipation.

With a battery buffered power supply, the information may be held in the memory for very long periods of time without significant discharging. When the system is powered down the V_{DD} voltage may be less than 5V, since there is no speed requirement. At $V_{DD} = 4.5V$ supply the typical power dissipation is about $0.15 \mu W$ per device.

Figure 5.6 shows a typical power supply. The Ni-Cd battery is charged during normal operation. When the mains power fails, the battery will give current for the memory. In most of the cases the diodes may be omitted. The resistor R should limit the charging current to less than 0.03 times nominal battery capacity in Ah. Thus, a battery with 225 mAh is allowed to be charged with 6 mA continuously without being damaged.

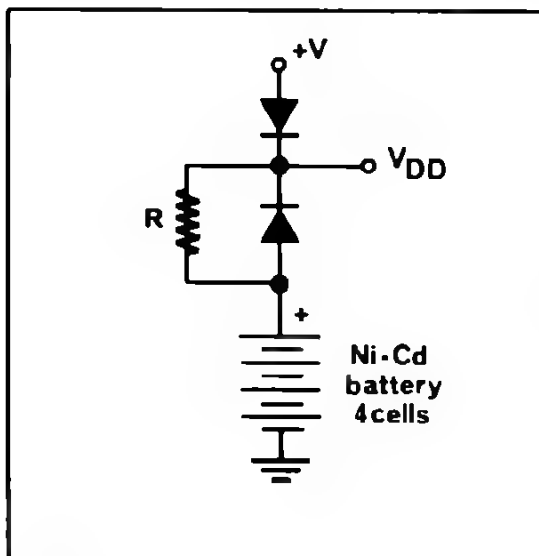


Fig. 5.6 STAND-BY BATTERY CIRCUIT

Besides the low power drain the memory has other advantages. Tri-state output and two chip enable inputs allow easy expansion.

Further application information such as timing diagrams and interfacing with other logic families can be found in the data sheet.

There are two other random access memories, the MC 14537 and the MC 14552. The organisation is 256×1 bit for MC 14537 and 64×4 bits for MC 14552.

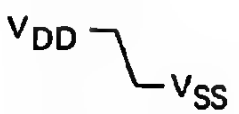
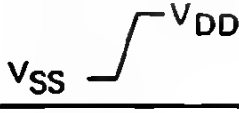
5.2.2. READ-ONLY MEMORY

The MCM 14524 is a 1024-bit Read-Only Memory organized in 256 words of 4 bits each. The device is a mask programmable part, which is programmed in the factory according to the user's specification.

The circuit must be clocked with a negative clock pulse in order to obtain the desired information from a specified address. The data will appear on the outputs following the negative going edge of the clock. When the clock goes high the data will be latched in the output latches. The address inputs must not change during the clock pulse. The addresses must be present for t_{setup} -time prior to the negative going clock-edge and must stay unchanged for t_{hold} -time after the positive going clock-edge.

There is another input which is called MEMORY ENABLE. This input may be taken low asynchronously, forcing all outputs low and resetting the output latches.

Truth table:

CLOCK	ENABLE	B ₀	B ₁	B ₂	B ₃
	1	<Address>	<Address>	<Address>	<Address>
	1	Output data latches			
X	0	0	0	0	0

There are many possible applications for this READ ONLY MEMORY, the most typical being code conversion, microprogramming in computers, and for storing "look up" tables.

3. MAJORITY LOGIC GATE MC 14530

The class of logic functions called "majority logic" which has long been dormant, is now being used as basic logic building blocks alongside conventional AND, NAND, OR, and NOR functions. Broadening the logic and system designer's list of useful tools, majority logic is defined simply as a function whose output depends on the state of the majority of its inputs. Devices having this capability often significantly reduce the total number of logic gates required to implement a function.

Already a new majority-logic chip built with complementary-MOS technology is available for functions that are otherwise difficult to realize, for example, in correlation techniques dealing with weighted variable values and in communications systems where information must be retrieved from noisy backgrounds.

5.3.1. THE MAJORITY-LOGIC FUNCTION

Figure 4.1 relates the majority logic to the other basic gating functions. Taking n as the number of inputs to a gate, the standard gate functions sense n unique combinations out of 2^n total combinations. Out of a possible 2^n combinations, the last grouping of gates senses 2^{n-1} combinations, and these are the majority and parity functions. It should be noted that if all inputs are random in nature, the output of these functions can be expected to be true half of the time.

The majority-logic function is most useful because inputs may be used for both logic and control.

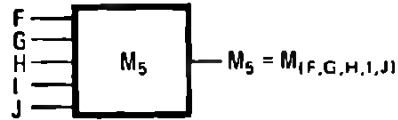
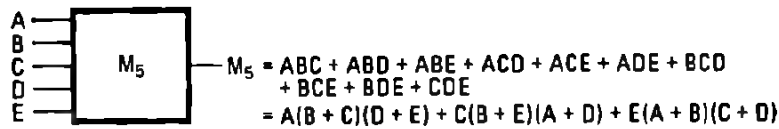
This new member of the CMOS family is a dual five-input majority-logic gate (M_5). Because of the tradeoffs of production cost and logic flexibility, a five-input device was chosen, since five inputs are sufficient to demonstrate the flexibility of majority logic but are not too many to unduly complicate fabrication. The function shown in Figure 5.7a was packaged in a 16-pin DIP instead of the conventional 14-pin DIP.

5.3.2. INVERTING OUTPUT

The two additional pins allow an exclusive-NOR gate to be added to each M_5 gate, providing two significant advantages as shown in Figure 5.7b. The output may be logically inverted by applying a logic 0 to the W input. Also, the W input may be used as a variable that is logically compared to the majority of the other inputs, a function that cannot be easily implemented with conventional gates. The resulting logic component lends itself to numerous applications that were not heretofore economically practical.

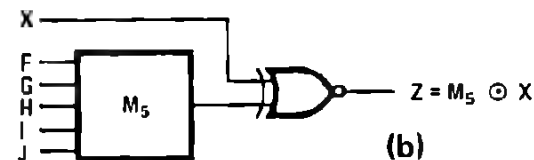
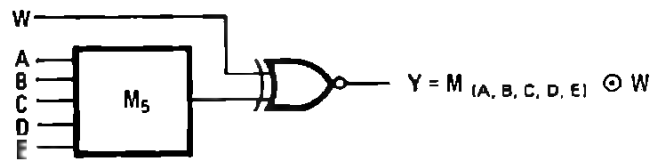
5.3.3. APPLYING THE DUAL M_5 GATE

The basic M_5 gate with exclusive-NOR is a powerful combinatorial logic function. In Figure 5.8 which shows the basic M_5 configurations, the functions in 5.8a through 5.8d represent the majority of five inputs and three inputs, and the OR of three inputs, and the AND of three inputs, respectively. By changing the W input of the exclusive-NOR from a 1 to a 0, the complements of the previous four functions are obtained (functions 5.8e through 5.8h).



(a)

Fig. 5. 7
BLOC DIAGRAM OF
THE MAJORITY
LOGIC GATE M_5
MC 14530.



(b)

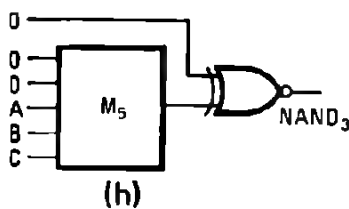
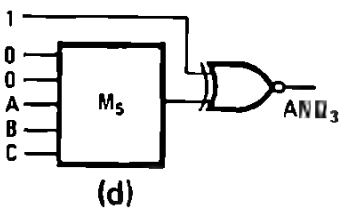
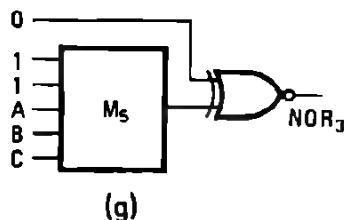
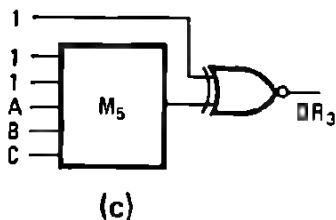
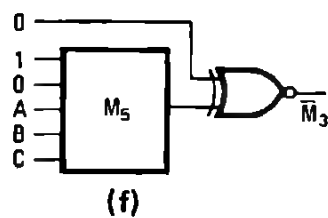
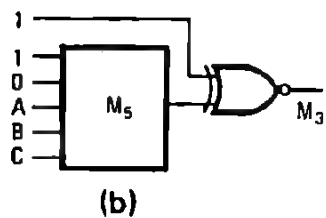
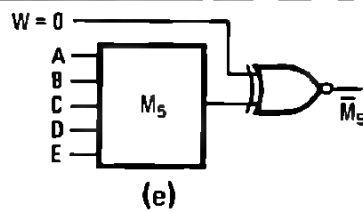
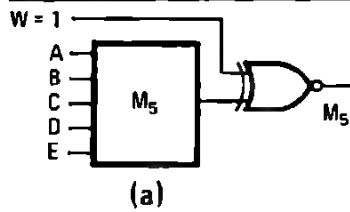
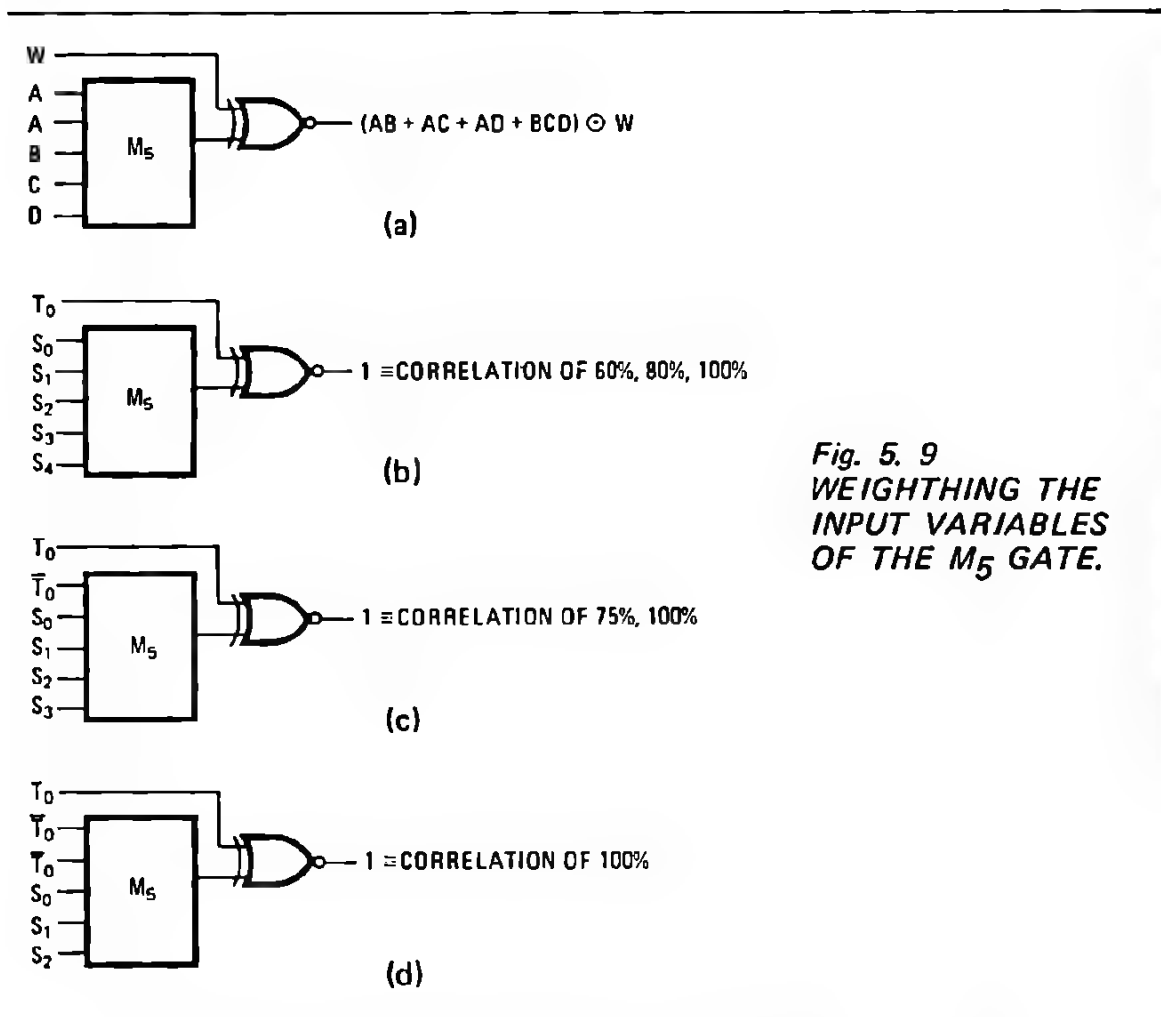


Fig. 5. 8
USING THE M_5 GATE
TO GENERATE
COMBINATORIAL
FUNCTIONS

Figure 5.9a illustrates a method used for increasing the "weight" of a variable. Here the A input is given a weight of two by repeating it once, with the resultant Boolean output expression shown. The majority gate may also be used to indicate if the correlation between a test bit (T_0) and various input variables is greater than or equal to a predetermined value.

For example, Figure 5.9b illustrates correlation greater than or equal to 60%, in Figure 5.9c, it is 75%, and in Figure 5.9d, correlation of 100% is required for a true or logical 1 output. By using arrays of these gates, it is possible to check the correlation factor between words stored in a memory and multiple samples of word data that have a large noise content. Thus, this correlation technique can be used for enhancing radar signatures and improving the performance of recognition equipment.



The versatility of majority logic can be appreciated from Figure 5.10, which shows two combinational uses of M_5 gates. Figure 5.10a provides the NAND of three variables ANDed with two more variables, impossible with a single package in other logic families. By using only two packages in the configuration of Figure 5.10b, many combinatorial functions of a large number of variables can be obtained with a significant saving in package count over other approaches. For the example shown, TTL requires twice as many packages.

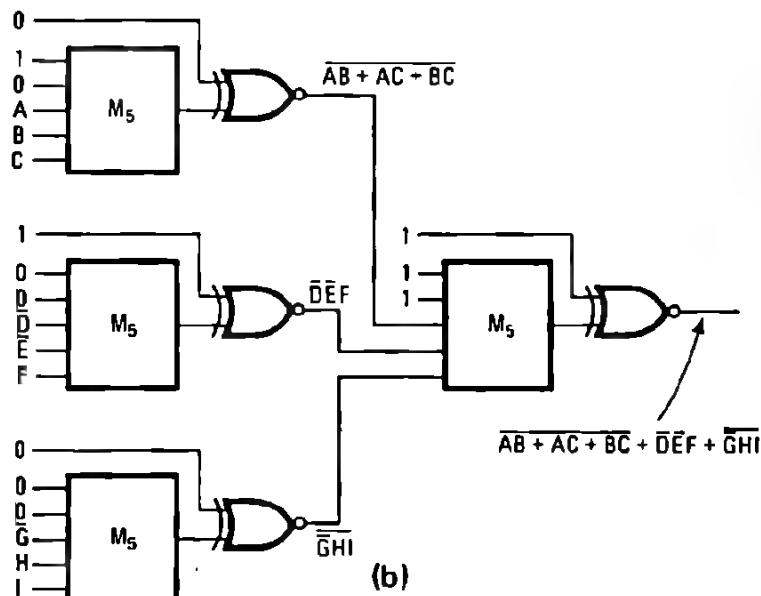
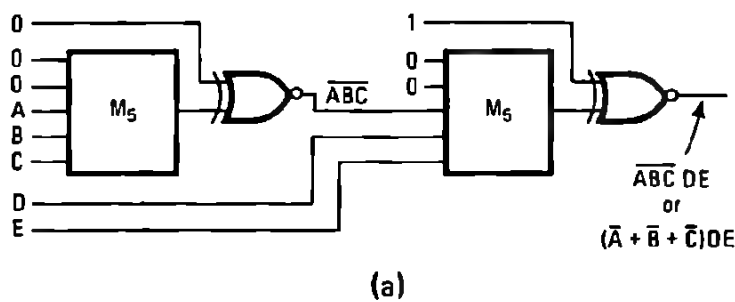


Fig. 5. 10
TYPICAL APPLICA-
TIONS OF THE M_5
GATE SHOWING THE
COMBINATORIAL
FLEXIBILITY.

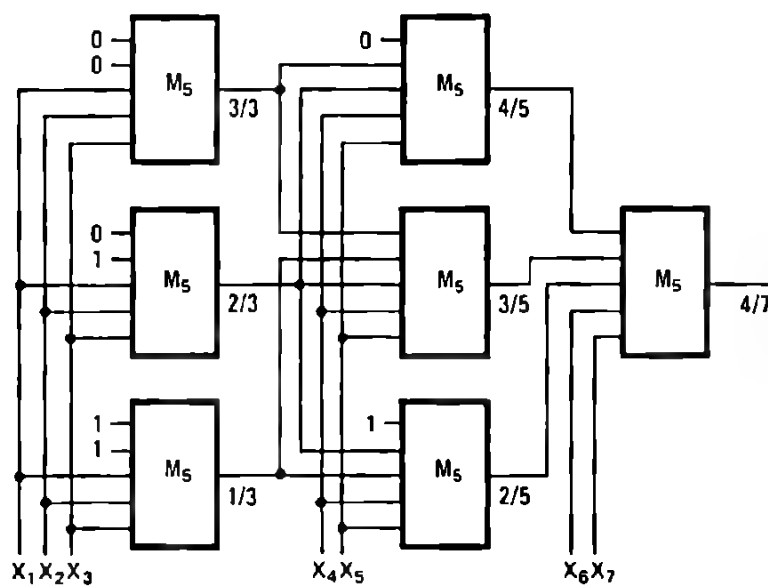


Fig. 5. 11
N-BIT DETECTION IN
A M-BIT WORD USING
USING CASCADED
 M_5 GATES

The majority-logic gates may also be formed into arrays that are useful for detecting whether or not n bits out of m bits of a given word are true. This is useful in conjunction with certain types of coding schemes involving a fixed number of 1s. Majority gates with more than five inputs can also be built with arrays, as illustrated in Figure 5.11a. The general symbology n/m is used to illustrate that the majority gate is wired to detect whether n or more inputs are true out of a possible m input bits. For example, $2/3$ -states that the output is true if two or more of three inputs are true, i.e. M_3 . The array in Figure 5.11 is best understood by following through the array from left to right for the seven input bits, X_1 through X_7 . It will be noted that the output $4/7$ is true only when four or more inputs are true, i.e. M_7 .

A general-purpose array is easily formed so that all possible cases of n/m can be detected. This is illustrated in Figure 5.12a, where 15 M_5 gates ($7 \times 1/2$ packages) are required. If the exact number of true bits in the input word is required, the output of the array may be encoded into a 3-bit binary word through the use of a priority encoder (Fig. 5.12b). A priority encoder is an MSI function in which each input is assigned a fixed priority (0 through 7 in the example shown) and the output is the encoded binary equivalent of the highest-priority input that is true. This array is useful for checking the correctness of n/m codes and determining the number of bits in a word that correlates with a test word.

5.3.4. MORE CORRELATION

Because of the ability to weight inputs in majority-logic sequencing, M_5 chips are ideal for applications where sensed data is to be compared to standards or various test words, and the degree of comparison or correlation is desired. Examples are in character-recognition equipment, speech recognition, radar-return analysis, recognition of various codes, and the recovery of information from noisy data samples.

The array shown in Figure 5.13, generic in nature, has been generalized for use in many correlation applications. Although this array may not be optimized for some applications, it presents a typical method of solution for many correlation problems.

In operation, the portion to the left of the figure consists of seven shift-register segments. Five flip-flops from each shift-register are shown containing five time-sequential samples (S_1 through S_5) of one bit of a 7-bit data word.

The first seven M_5 gates vote on the five data-word samples. The majority of the five samples of each bit are then compared bit by bit with a test word (test bits 1 to 7). The result of each comparison is then available at the bit-correlation outputs.

Moreover, it is possible, by the method shown in Figure 5.9, based upon the bit-correlation outputs, to deliberately feed back complements of the test bits to check for a higher correlation factor. These complements may be fed back in a serial manner and mixed with the data word in a predetermined manner.

The over-all correlation factor (on a word basis) is sensed by the 11 M_5 gates shown to the right. This configuration senses from 4 out of 7 up to 7 out of 7 bits in agreement with the test word. If none of the four outputs is true, the anticorrelation factor may be obtained by inverting all 7 test bits; e.g., the $7/7$ output would then be true if no original bits were in agreement.

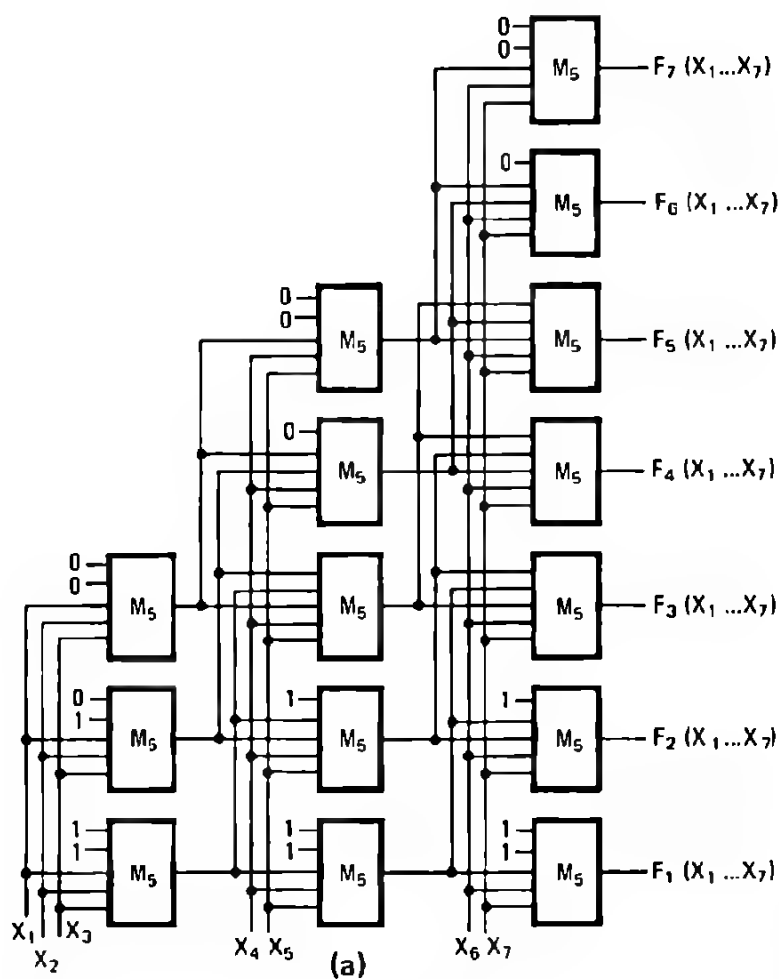
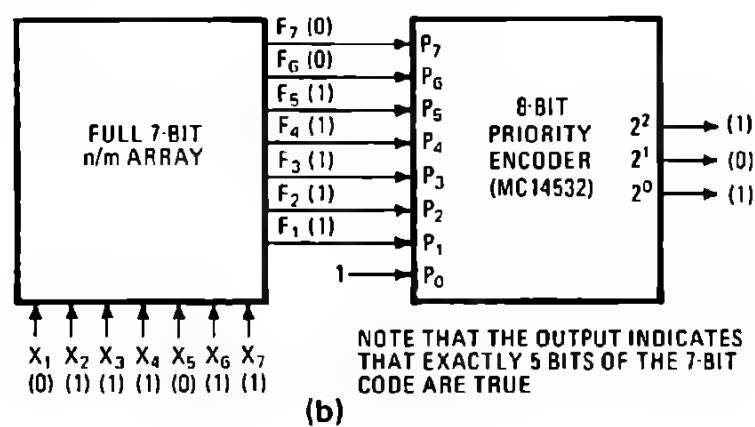


Fig. 5. 12
GENERAL DIAGRAM
FOR N-BIT DETECTION
IN A M-BIT WORD.



in addition to performing combinational logic with M_5 gates, sequential logic can also be implemented by feeding the output of a majority gate back to one or more inputs. Figure 5.14a illustrates this application for both three-input and five-input configurations. As the truth tables show, this type of flip-flop will change states only when there is coincidence of all inputs. For changing inputs, the device will hold the state of last coincidence until the opposite coincidence

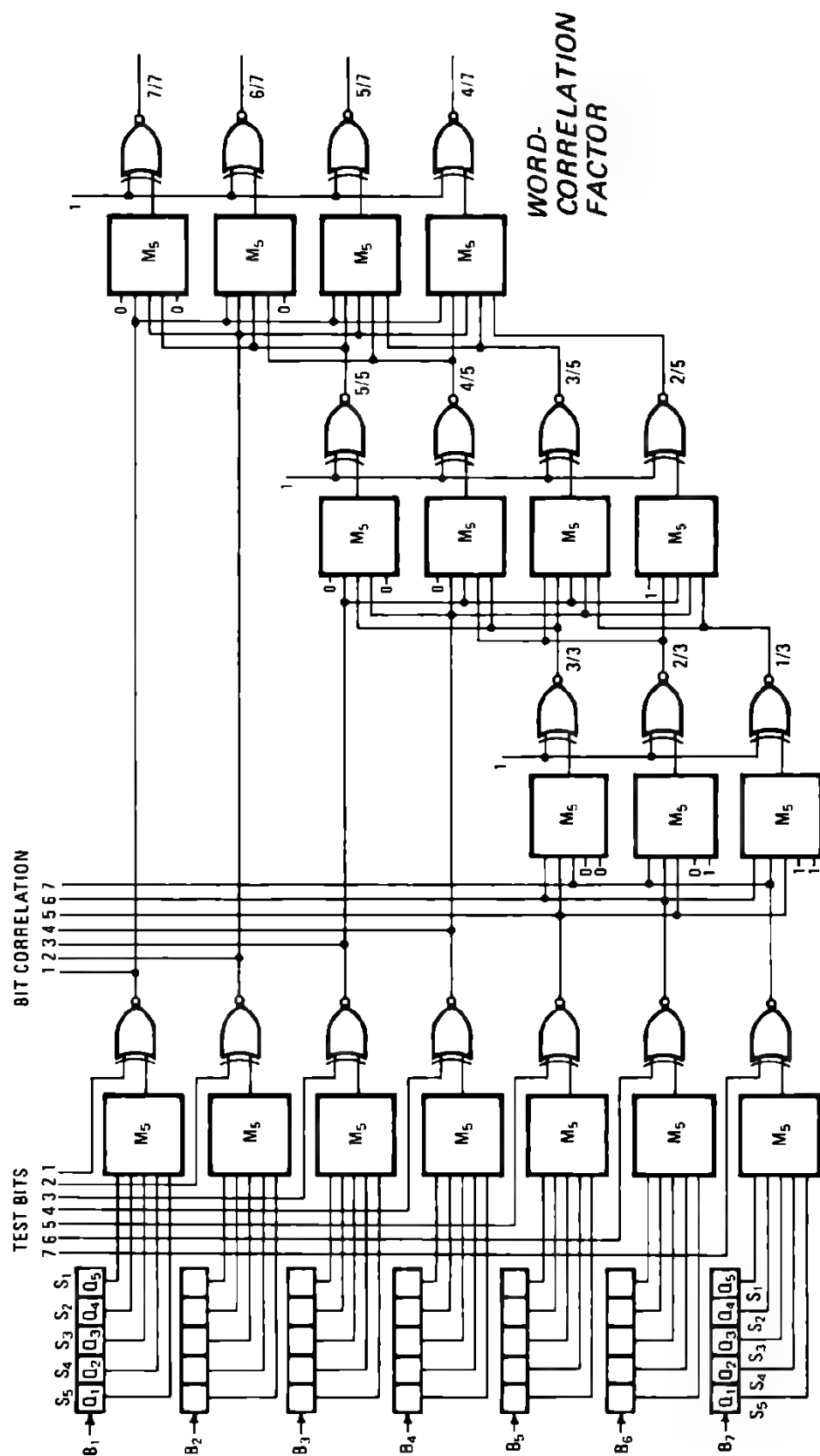


Fig. 5. 13. CORRELATION EXAMPLE OF TWO WORDS OF 7 BITS USING M_5 GATE

One area where this scheme is useful is in the control of UP/DOWN counters. Frequently, when a maximum or minimum count is reached, further counting must be inhibited to prevent spillover — the counter will change all states (all 1s to all 0s, or vice versa). An example is shown in Figure 5.14b, where the dual M_5 gate detects all 0s or all 1s, for a 32-state UP/DOWN counter.

The first gate, A, senses whether all 1s or 0s are present from the first 3 bits of the counter. The output of gate A feeds back to two of its inputs and one of the inputs of gate B. Only when the remaining two stages of the UP/DOWN counter agree with the output of A can the output of B change.

If the counter is in the UP mode (1 on the control line), and a maximum count is obtained (all 1s), the output of gate B will be a 1, inhibiting the clock and thus preventing further counting. On the other hand, if the mode control goes low while the clock is still high, counting will occur downward on the next clock edge, until all 0s result. The counter will then be inhibited again, thus preventing roll-over.

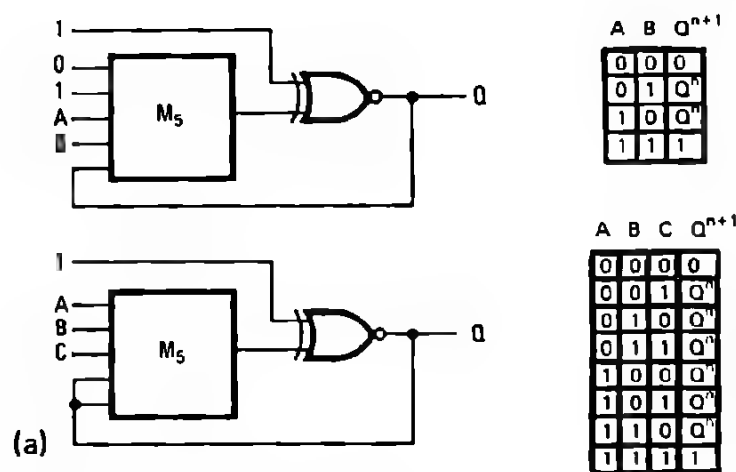
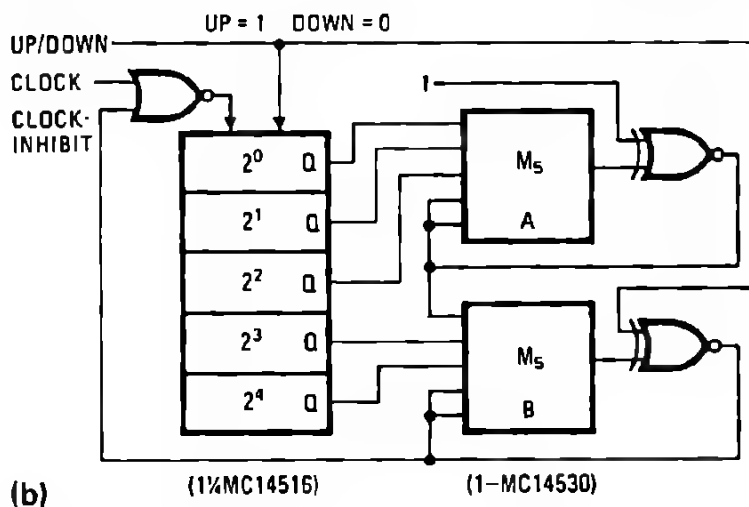


Fig. 5. 14
SEQUENTIAL FUNCTIONS
GENERATION BY
USING M_5 GATES



5.3.5. THE FUTURE OF MAJORITY LOGIC

Now that majority logic has become economically practical through MSI, the function may become an industry standard. As familiarity grows, the M_5 gate will be used in applications to reduce package count and provide logic that is programmable as a result of its own decisions or external computer control. Correlation arrays that are useful for character and speech recognition are natural applications. The symmetry of the majority-logic layout, using CMOS devices, lends itself to high-density packing. By using minimum-geometry devices, large majority-logic-gate arrays of more than 200 gates can be fabricated by means of present production technology. Arrays of this size could easily usher in whole new philosophies in system architecture that would lend themselves to what is sometimes referred to as probabilistic processing, where many variables are not necessarily 100% true but instead may be mixed with noise or have assigned weights or degrees of confidence.

CHAPTER 6



System Design

SYSTEM DESIGN

A CMOS SYSTEM DESIGN CONSIDERATIONS

B ELECTRICAL CONSIDERATIONS FOR CMOS GATES

1. TRANSFER REGION VARIATION
FOR GATES
2. OUTPUT IMPEDANCE
3. OUTPUT SHORT-CIRCUIT
LIMITATION
4. UNUSED INPUTS
5. INPUT CHARACTERISTICS
6. PARALLELING GATES
7. WIRED "OR" CONNEXION
8. CAPACITIVE LOAD
9. TRISTATE FEATURES

C POWER SUPPLY CONSIDERATIONS

1. VOLTAGE REGULATION
2. POWER AND CURRENT
REQUIREMENTS
3. RIPPLE AND FILTERING

D INTERFACING CMOS WITH OTHER LOGIC FAMILIES AND DISCRETE DEVICES

1. CMOS TO TTL
2. CMOS TO HTL
3. CMOS TO ECL
4. CMOS TO PMOS DEVICES
5. CMOS TO DISCRETE
TRANSISTOR INTERFACE

E FANOUT CONSIDERATIONS FOR CMOS

F INTERCONNECTING CMOS CIRCUITS

A CMOS SYSTEM DESIGN CONSIDERATIONS

This section is intended to give guidelines for achieving a correct system design with CMOS devices. All considerations that have to be made for an implementation will be mentioned successively.

The main items will concern the dc and ac operating conditions, the interface problems with other families and the interconnections between devices of the CMOS family.

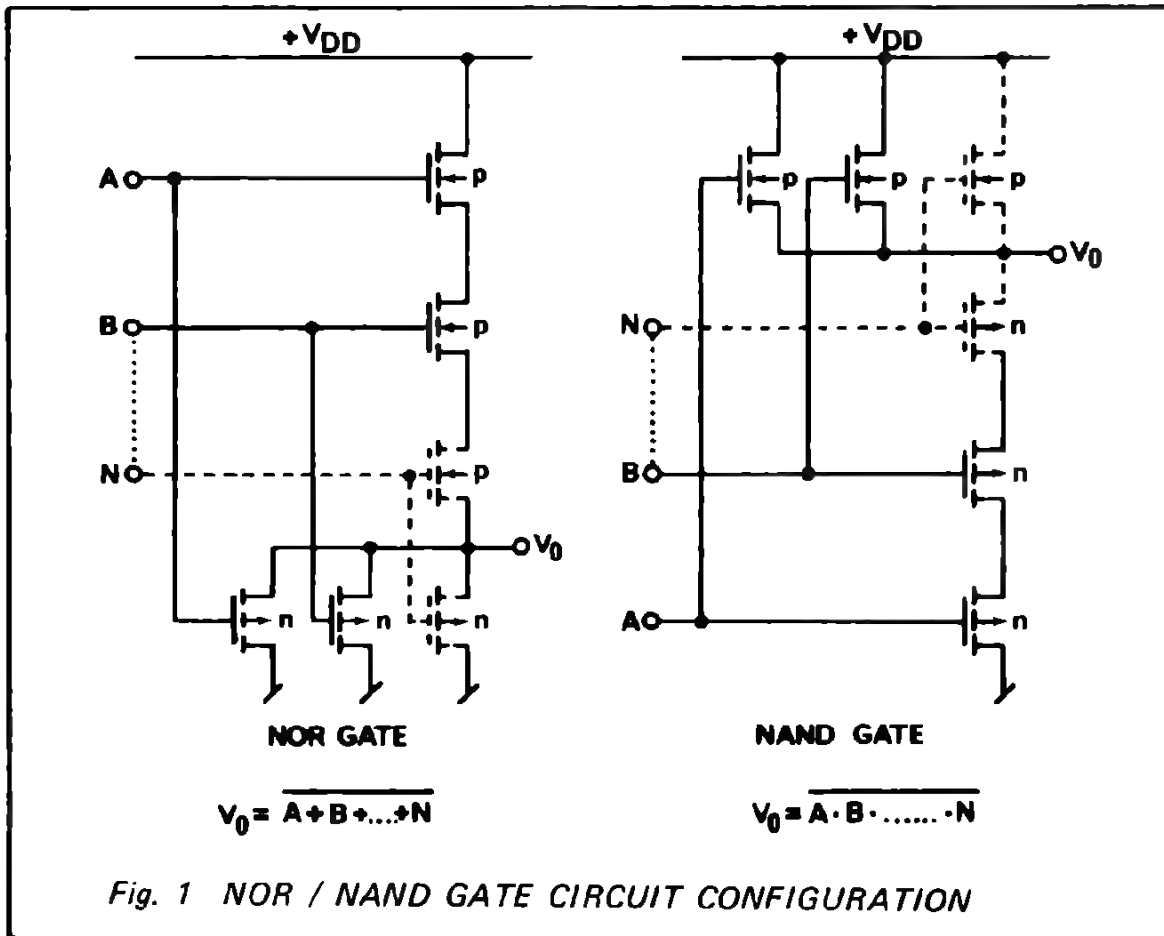
B ELECTRICAL CONSIDERATIONS FOR CMOS GATES

Besides the main features of the CMOS family such as low power dissipation and supply voltage flexibility, several other parameters should be considered when using CMOS devices

- variation of the transfer region (or dc noise immunity) of the gate in conjunction with the gate configuration
- variation of the output impedance in conjunction with the number of used inputs per gate
- output short circuit limitation
- unused inputs
- paralleling gates
- wired "or" connections
- capacitive load
- input characteristics and
- tristate features.

1. TRANSFER REGION VARIATION FOR GATES

In the CMOS circuits, the fundamental gate structure is directly related to the required logic function. Therefore, for NOR gates, the n-channel transistors are connected in parallel and referred to V_{SS} , the p-channel transistors are connected in series and referred to $+V_{DD}$. For the NAND gate, the circuit configuration is the mirror image of the NOR gate (see Fig. 1).



Since the MOS transistors are mainly voltage controlled resistors, the transfer region and consequently also the dc noise immunity, is determined by the parallel/series combination of the transistor impedances in conjunction with the input voltages, the number of inputs and the gate circuit configuration. The transfer region of a gate is defined as:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \text{maximum.}$$

As can be seen in Figure 2, the values of the standard transistor on-resistance may vary from 10 mohm down to 30 ohms (depending on the physical dimensions of the MOS transistor and on the value of the applied voltages).

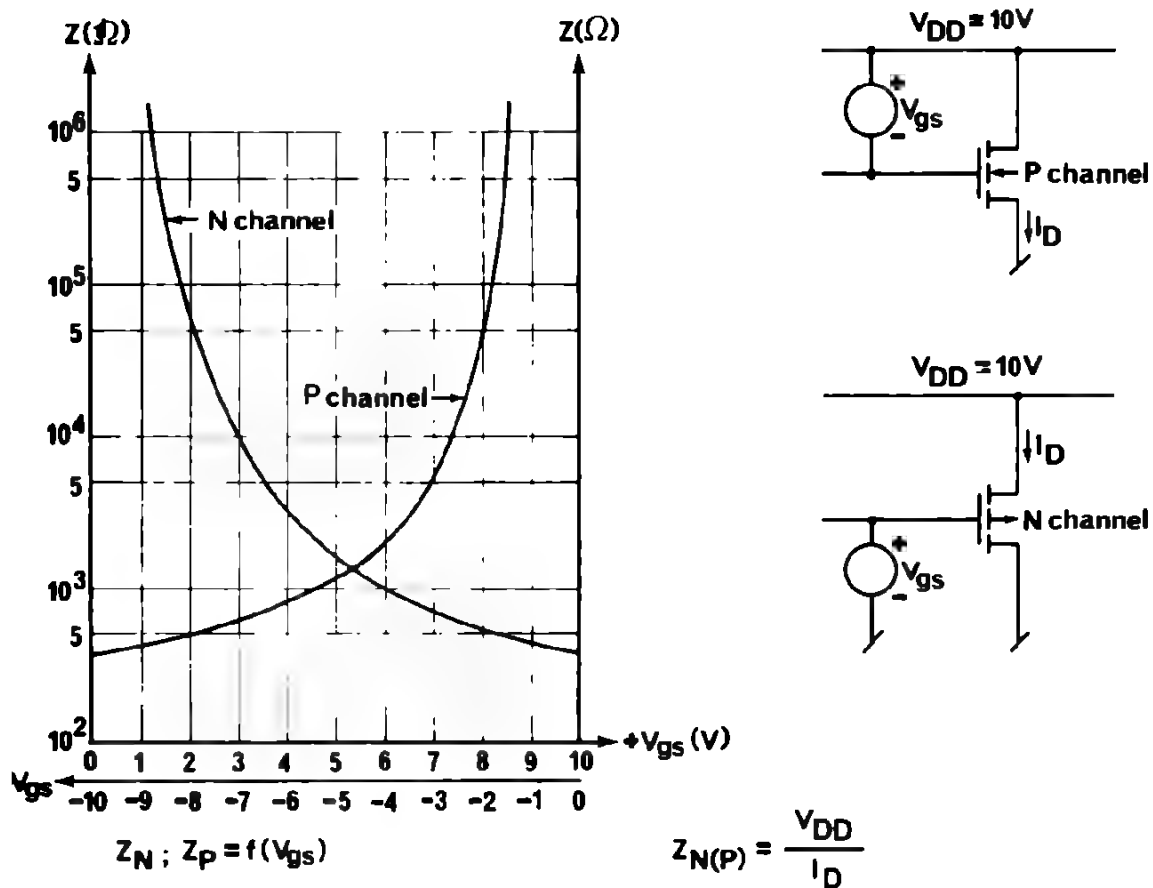


Fig. 2 TYPICAL N- AND P-CHANNEL IMPEDANCE

as illustrated in Figure 3, the transfer region in NOR gates will result from the combination of the impedances of the n-channel transistors connected in parallel and the p-channel transistors connected in series.

For the NAND gate, the transfer region is given by the ratio of the impedance of the n-channel transistors connected in series and the p-channel transistors connected in parallel. (See also chapter 3).

Using these considerations for the NOR gate, the resulting dc noise margin, which is directly related to the transfer region centre, is defined approximately by the empirical relation (1) and (2).

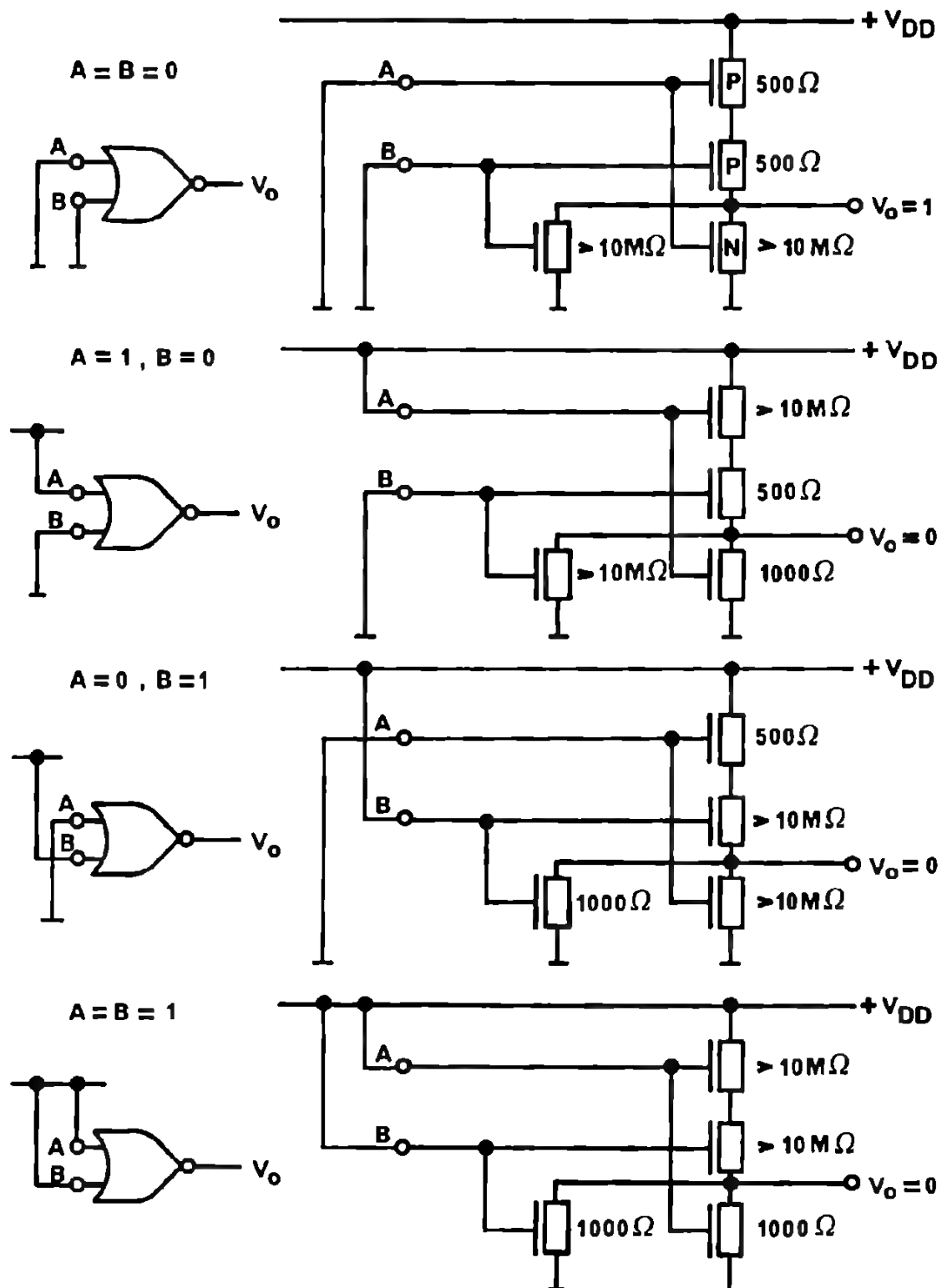


Fig. 3 TYPICAL TRANSISTOR "ON/OFF" RESISTANCE FOR THE INPUT CONFIGURATION OF A 2-INPUT NOR GATE.

- the input voltage low noise margin (V_{NIL}) can be calculated as follows:

$$V_{NIL} \approx V_{DD} \left[\frac{1}{1,5 + \frac{n_i}{n_m}} - 0,1 \right] \quad 1$$

where: - n_i = number of used inputs/gate
 - n_m = total number of inputs/gate.

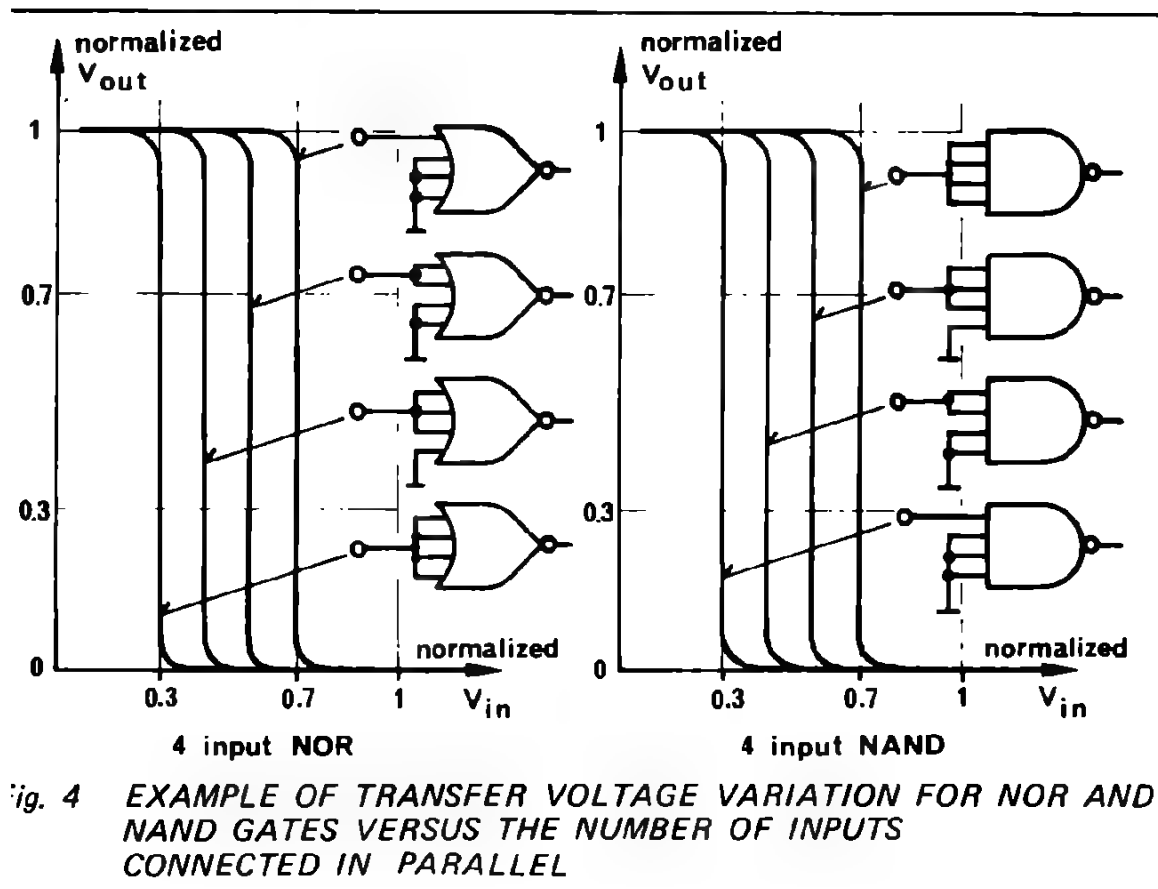
- the input voltage high noise margin (V_{NIH})

$$V_{NIH} \approx V_{DD} \left[0,9 - \frac{1}{1,5 + \frac{n_i}{n_m}} \right] \quad 2$$

For the NAND gates similar equations can be derived.

It should be noted that the input "low" noise margin will decrease as a function of the number of controlled inputs in a NOR gate; for a NAND gate, it will increase. The input "high" noise margin will increase in function of the number of controlled inputs for the NOR gate, for the NAND gate it will decrease.

In Figure 4 the transfer regions $V_{out} = f(V_{in})$ are shown as a function of the number of parallel connected inputs, for NOR and NAND gates.



OUTPUT IMPEDANCE

The output impedance of a CMOS gate is related to the circuit configuration, OR or NAND, to the number of inputs used, to the logic state "1" or "0" and to the value of the applied voltages. Again the parallel/series combination of the transistors has to be considered.

The following curves (Fig. 5, 6, 7, 8) indicate the output impedances for two-input NOR and NAND gates, in both high and low output states.

Two operation regions should be distinguished:

- constant "Z" region where the transistors operate in saturation,
- constant current region where the transistors operate in the pinch-off condition.

These curves should be considered particularly when designing interface circuits for other logic families or to discrete devices.

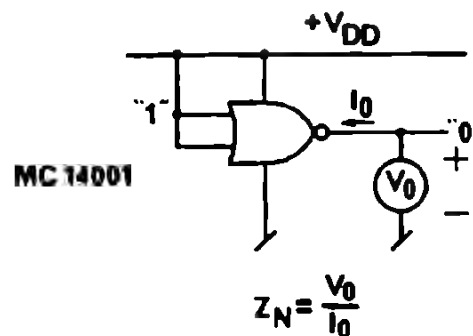
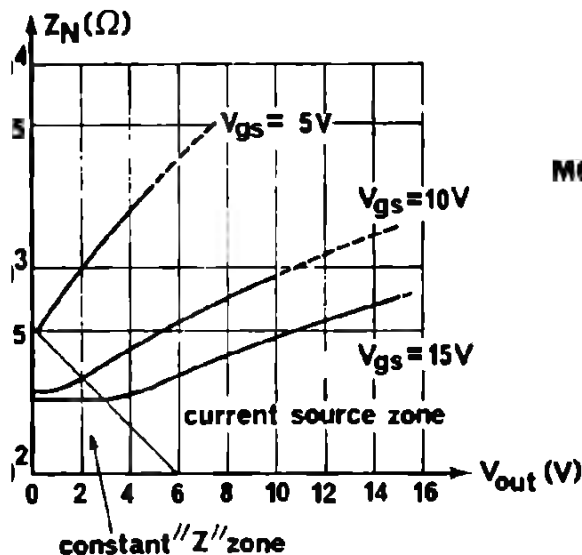


Fig. 5
OUTPUT IMPEDANCE Z_N
VERSUS OUTPUT
VOLTAGE V_0 (LOW STATE)
MC 14001

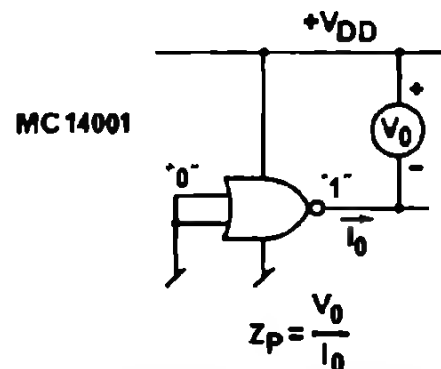
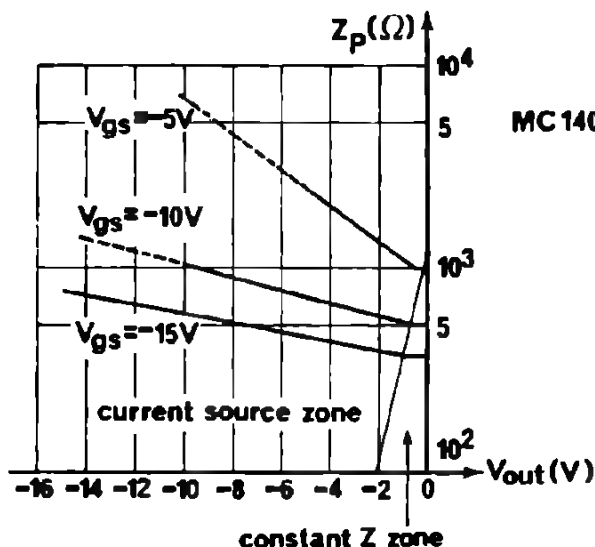


Fig. 6
OUTPUT IMPEDANCE Z_P
VERSUS OUTPUT
VOLTAGE V_0 (HIGH STATE)
MC 14001

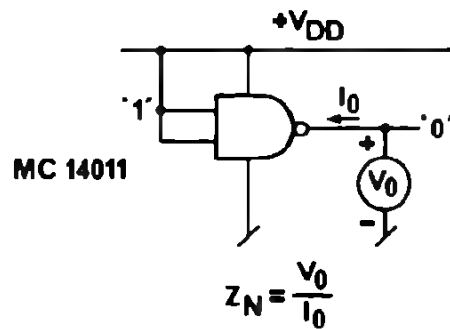
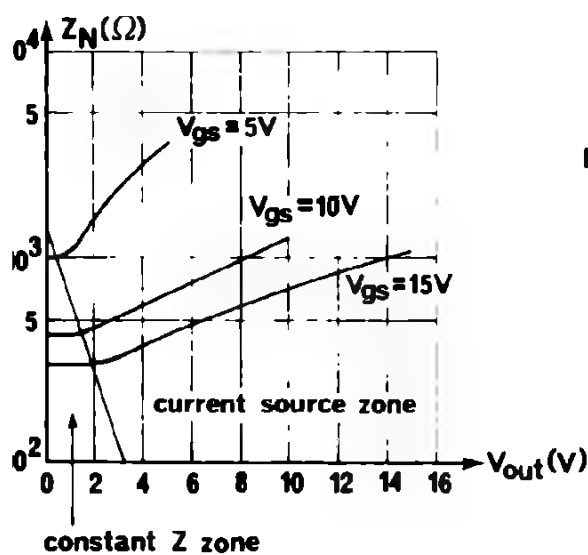


Fig. 7
OUTPUT IMPEDANCE Z_N
VERSUS OUTPUT
VOLTAGE V_0 (LOW STATE)
MC 14011

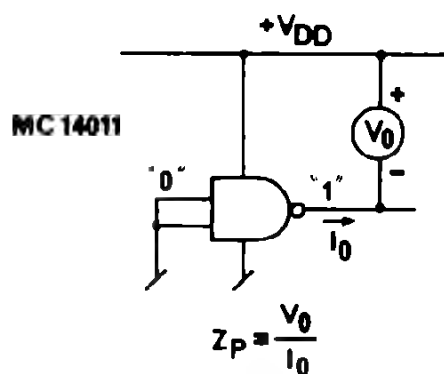
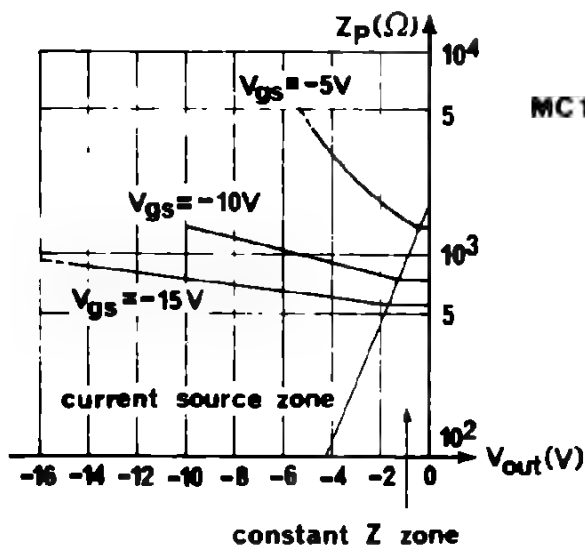


Fig. 8
OUTPUT IMPEDANCE Z_P
VERSUS OUTPUT
VOLTAGE V_0 (HIGH STATE)
MC 14011

or practical design purposes, the table of Figure 9 summarizes the output impedance in the logic "low" and "high" state for a NOR gate, NAND gate and buffer with $V_{DD} = 15V$, in relation to the number of used inputs. In some applications, it is required to achieve the lowest possible impedance for the output low or high state. In such a case, besides using buffers, it is recommended that the designer uses 4-input NOR or NAND gates with all inputs connected in parallel.

Output logic state	NOR		NAND		BUFFER	
	2 inputs*	4 inputs*	2 inputs*	4 inputs*	one input inverting	one input non-inverting
	MC 14001	MC 14002	MC 14011	MC 14012	MC 14009	MC 14010
High	380 Ω	400 Ω	550 Ω	85 Ω	330 Ω	250 Ω
Low	220 Ω	60 Ω	300 Ω	200 Ω	40 Ω	30 Ω

*All inputs are connected in parallel.

$V_{DD}=15V$ — Saturation voltage of n- and p-channels = 1V.

Fig. 9 COMPARATIVE TABLE OF TYPICAL OUTPUT IMPEDANCES FOR DIFFERENT GATE CONFIGURATIONS

Therefore, a 4-input NOR gate should be considered when it is required to sink current. In opposition a 4-input NAND gate should be used when it is required to source current. It should be noted that the output impedance in the low or high state is directly related to the number of controlled inputs.

In Figure 10 and 11 the output impedance is indicated for a 4-input NOR respectively NAND gates in conjunction with the number of used inputs. It should be noted that the output impedance is inversely proportional to the number of connected inputs.

$Z_0(\Omega)$

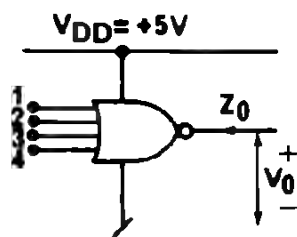
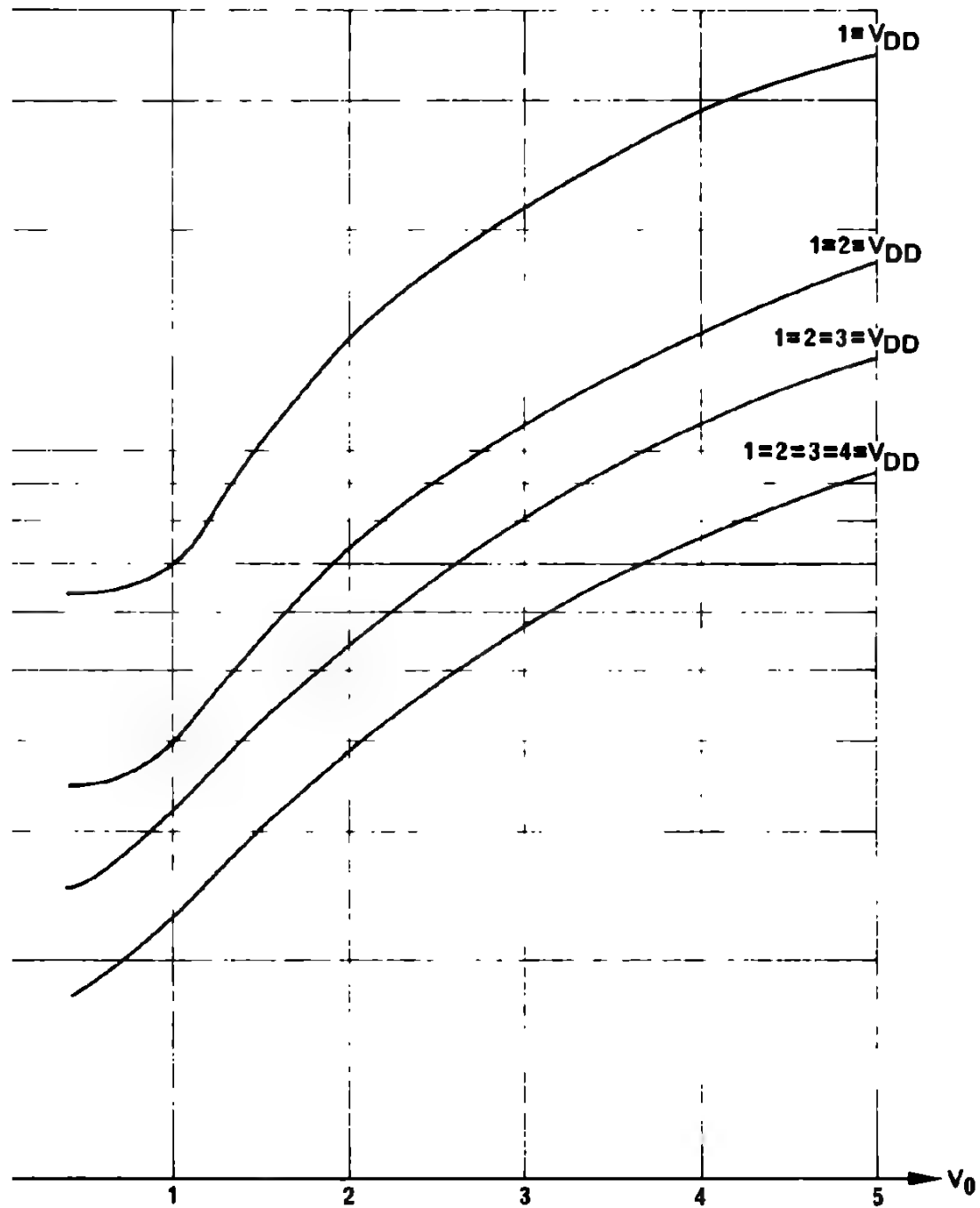


Fig. 10
TYPICAL OUTPUT IMPEDANCE Z_0 VERSUS
OUTPUT VOLTAGE V_0 FOR INPUT
(1, 1 2, 1 2 3, 1 2 3 4) CONNECTED IN
PARALLEL TO V_{DD} , NOR GATE MC 14002

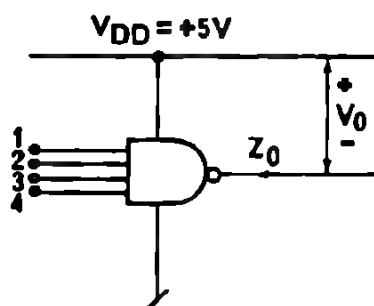
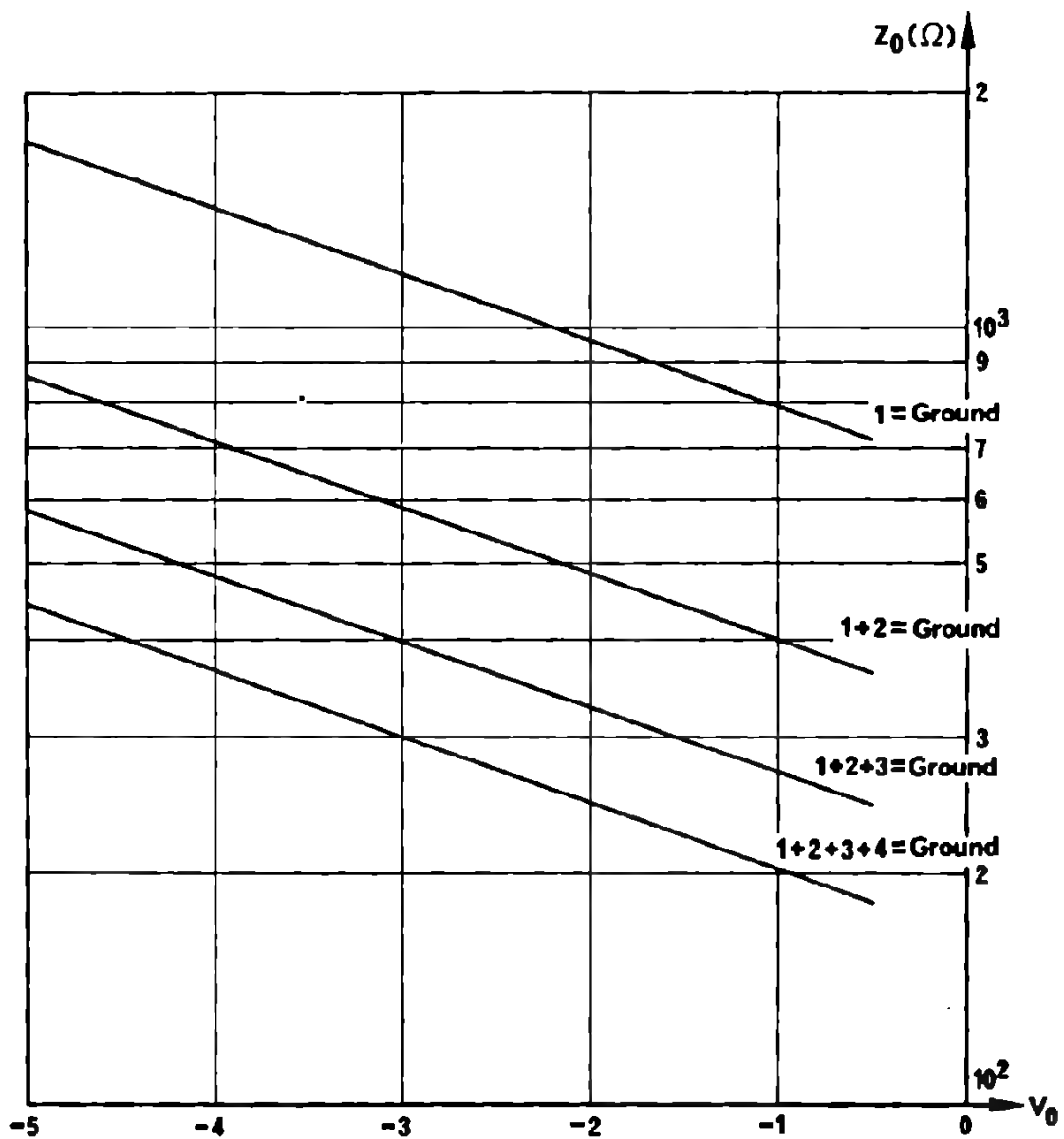


Fig. 11
TYPICAL OUTPUT IMPEDANCE Z_0 VERSUS
OUTPUT VOLTAGE V_0 FOR INPUT
(1, 1 2, 1 2 3, 1 2 3 4) CONNECTED TO
GROUND, NAND GATE MC 14012

3. OUTPUT SHORT-CIRCUIT LIMITATION

Usually standard bipolar logic is not short-circuit proof, which means that the output current is not limited to an acceptable value, so the device can be accidentally destroyed. In the case of the CMOS family, due to the nature of the MOS transistor, the maximum output current is limited to a relatively well

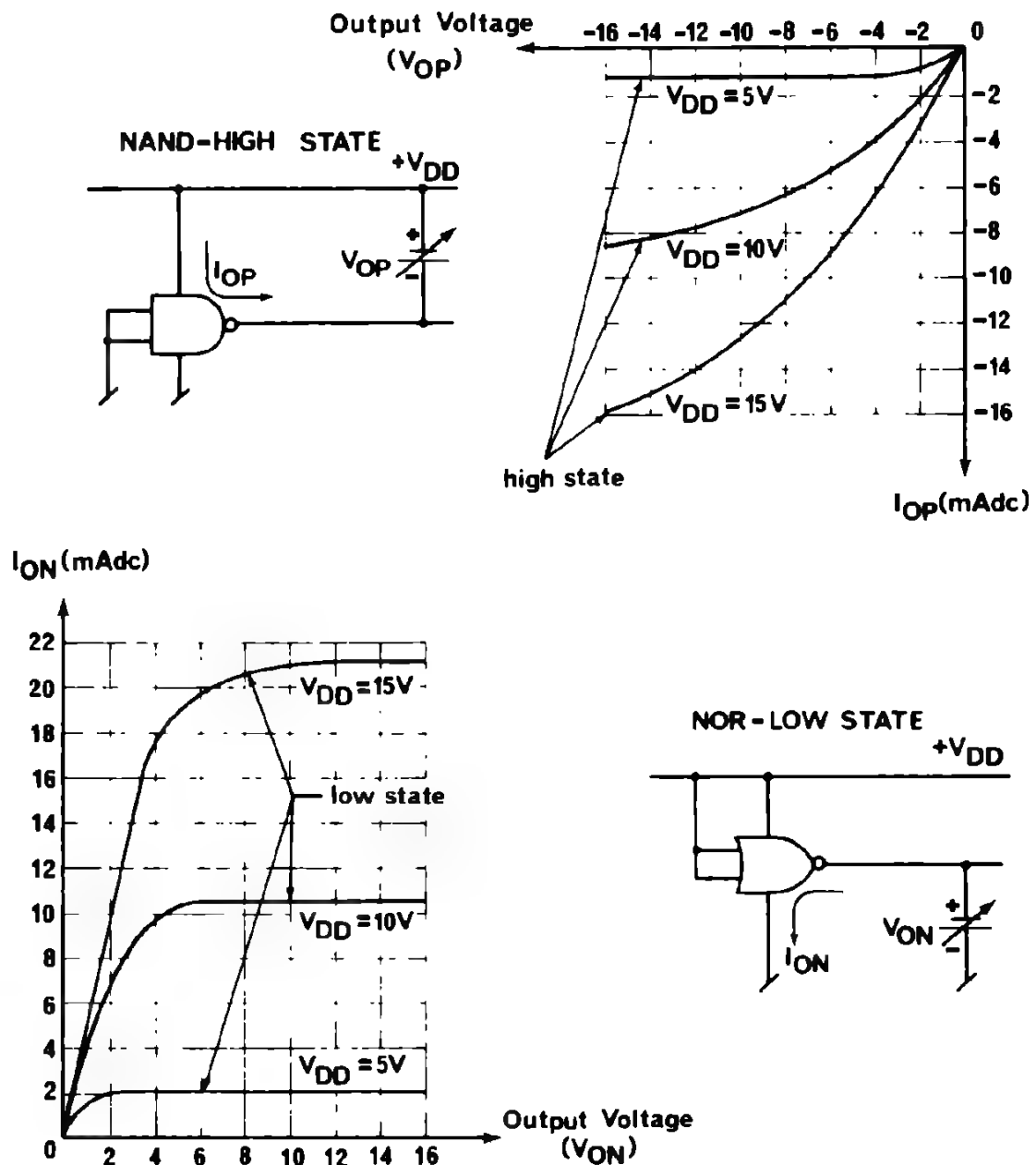


Fig. 12 TYPICAL LOW AND HIGH STATE GATES OUTPUT CHARACTERISTIC (MC 14001 & MC 14011) WHICH INDICATES THE CURRENT LIMITING EFFECT.

defined value, determined by the pinch-off effect of the output transistors. This limitation gives an inherent short time short-circuit protection of the CMOS circuit, particularly at low supply voltages.

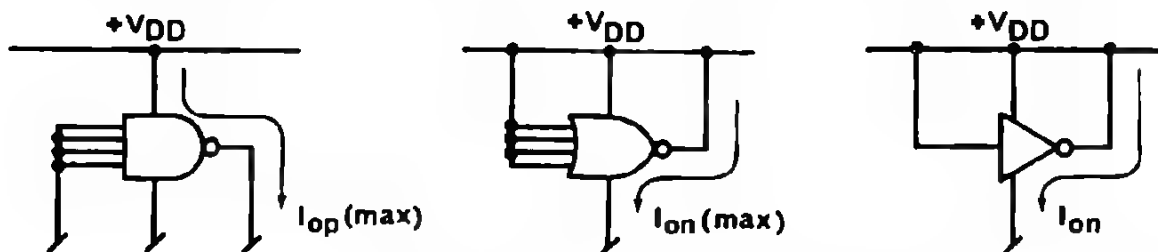
Figure 12 indicates a typical output characteristic for the output "low" or "high" state for NAND and NOR gates. As can be seen, the output current is always limited when the output is shorted to ground or to V_{DD} . However, the problem which will be faced when an output is shorted for a long time, is that the rated power dissipation or the current density in the metallization may be exceeded. This may degrade the output devices (see also paragraph 8).

The table in Figure 13 indicates for NOR, NAND gates and buffers the maximum output current which can be expected to flow "out of" or "in to" the circuit, in case of short-circuit.

$V_{DD} = +5V$	Output shorted to:		NOR		NAND		BUFFER
			2 input	4 input	2 input	4 input	
	+ V_{DD}	I_{ON}	4 mA	8 mA	2 mA	2 mA	25 mA
	Ground	I_{OP}	3 mA	2 mA	2 mA	13 mA	7 mA
$V_{DD} = +10V$	Output shorted to:		NOR		NAND		BUFFER
			2 input	4 input	2 input	4 input	
	+ V_{DD}	I_{ON}	16 mA	45 mA	12 mA	10 mA	100 mA
	Ground	I_{OP}	14 mA	9 mA	10 mA	50 mA	20 mA
$V_{DD} = +15V$	Output shorted to:		NOR		NAND		BUFFER
			2 input	4 input	2 input	4 input	
	+ V_{DD}	I_{ON}	30 mA	90 mA	20 mA	25 mA	170 mA
	Ground	I_{OP}	25 mA	20 mA	15 mA	90 mA	60 mA

Remark:

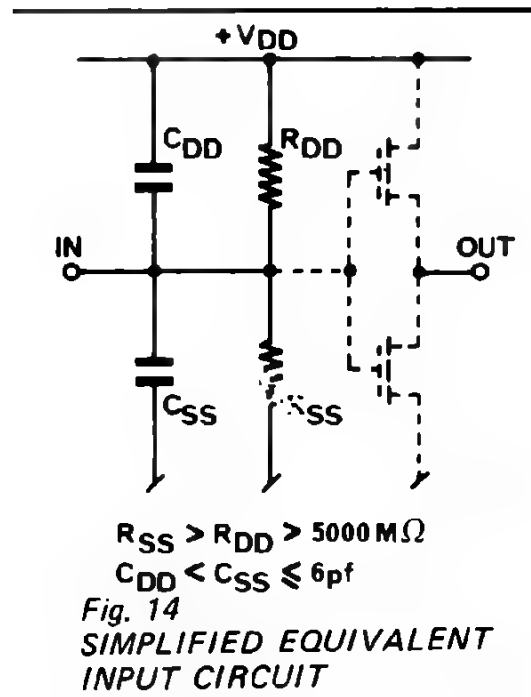
The DC operation of the CMOS circuit under these conditions is not guaranteed.



$I_{ON} \text{ (max)}$ – max short-circuit sink current (n-channel)
 $I_{OP} \text{ (max)}$ – max short-circuit source current (p-channel).

Fig. 13 EXPECTED MAX OUTPUT SHORT-CIRCUIT CURRENT FOR NOR, NAND GATES AND BUFFERS AS A FUNCTION OF ($V_{DD}=5, 10, 15V$)

period a DC current of 10 mA per
d gates. For the buffers, a maximum



equivalent capacitors and equivalent
can be seen that the input poten-
well defined. This fact can bring the
output information. Consequently,
round or to V_{DD} depending on the

ed to V_{DD} .
to V_{SS} .

gates in a package which can gene-
power supply line.
onnecting printed cards), a resistor
n the momentarily unused inputs
the gates in the correct logic state
stem.

important to use the high impe-
ample in RC delay circuits, it is
cs.

e input characteristics for a CMOS
the double diode protection system.

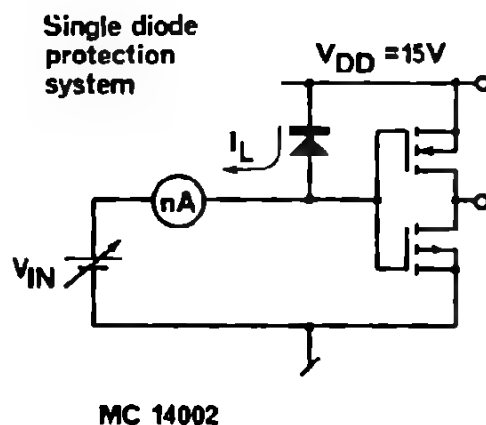
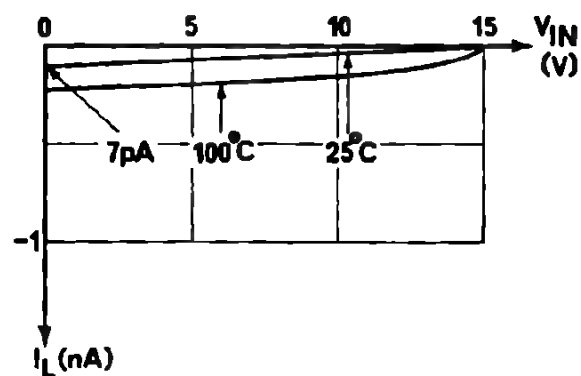
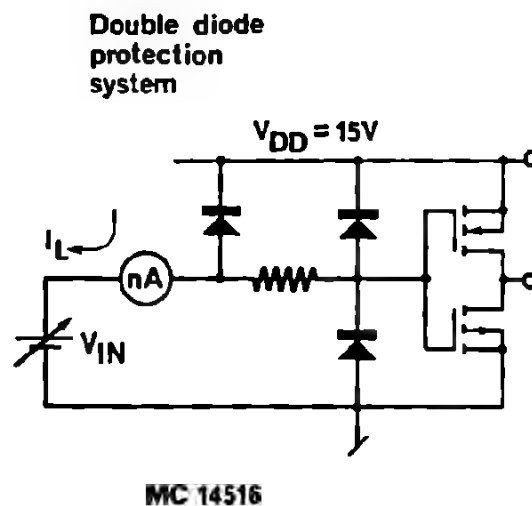
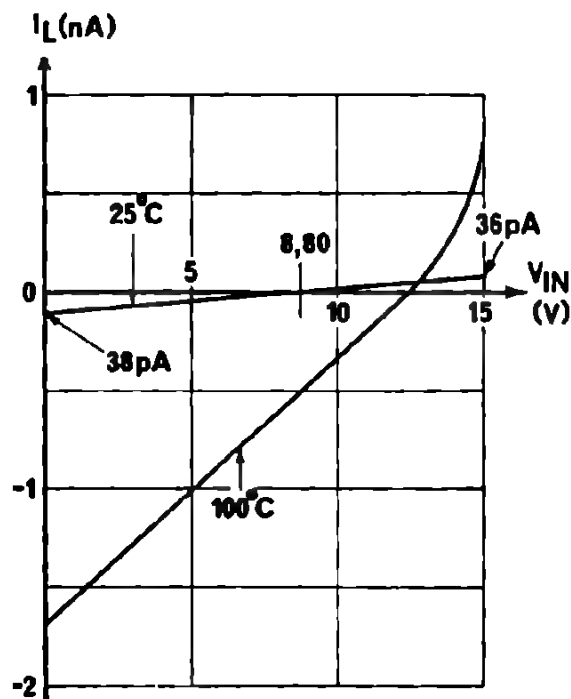
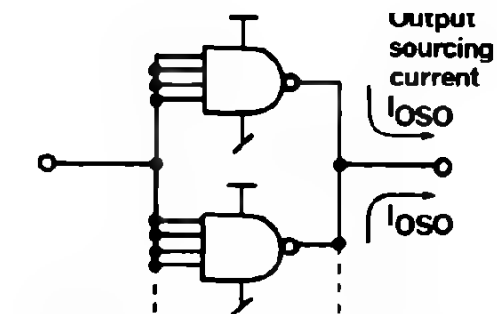
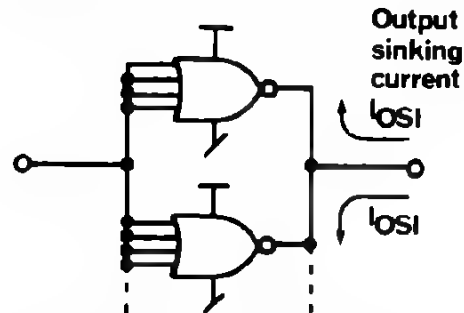


Fig. 14a TYPICAL INPUT LEAKAGE CURRENT OF A CMOS CIRCUIT FOR BOTH INPUT PROTECTION SYSTEMS

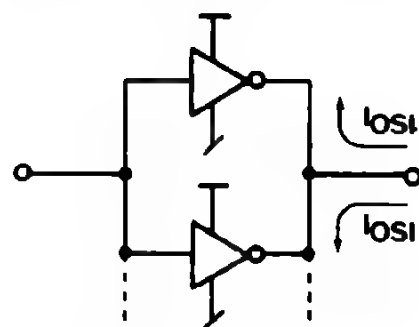
It should be remarked that the maximum input current changes in a proportion of 1 to 30 when the temperature varies from 20°C to 100°C. The input impedance which should be considered for practical purposes, is in the order of 10 MΩ at 100°C.



NAND GATE paralleling increases the current sourcing capacity.



NOR GATE paralleling increases the current sinking capacity.



INVERTER paralleling increases the current sinking capacity.

Fig. 15
CURRENT SOURCING/SINKING
INCREASES BY PARALLELING
GATES

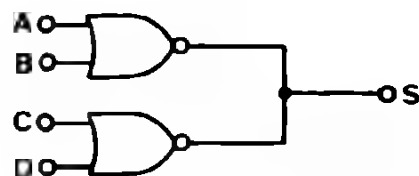


Fig. 16
WIRED "OR" CONNECTION
(should be avoided)

8. CAPACITIVE LOAD

8. 1. INPUT CAPACITIVE LOAD

The total input capacitance is determined by the capacitance of the case leads, the capacitance of the input protection system and the gate to substrate capacitance of the transistors.

As indicated in Fig. 6, ch. 3 the total input capacitance varies in conjunction with the applied input voltage and is mainly due to the variation of the gate to substrate capacitance of the transistor. Interconnecting gates automatically increase the total input capacitance which has, as first effect, to increase the switching times (refer to chapter 3).

The second effect is an increase of the power dissipation. One particular case of increased power dissipation is when an external capacitor is connected to the input for long delays, as shown in Figure 17.

If this delay is equal or larger than the thermal time constant of the IC chip, then the instantaneous power dissipation should be considered because the temperature of the chip will follow the instantaneous power rate. The instantaneous power dissipated in the CMOS circuit is determined by the V_{DD} voltage and the DC current circulating from the power supply line (refer to chapter 3).

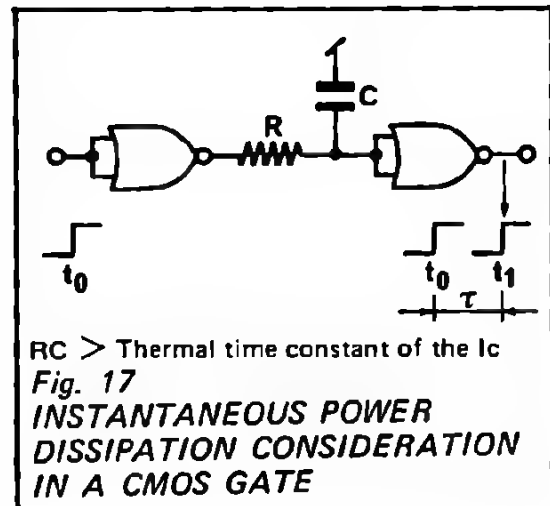


Figure 18 illustrates the expected power dissipation in function of the input voltage for $V_{DD} = 5, 10, 15V$ and for a 2-input NOR gate when the inputs change slowly.

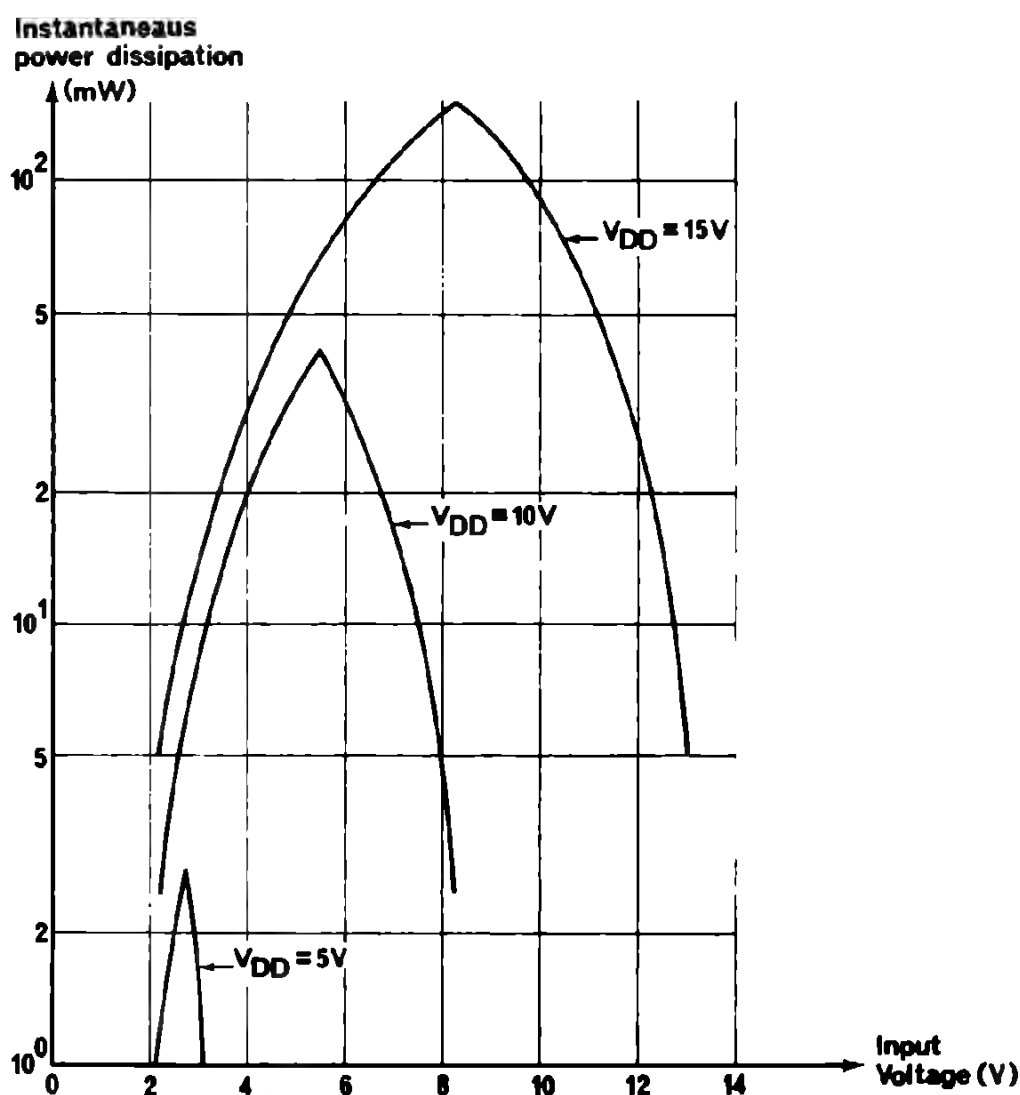


Fig. 18 EXPECTED INSTANTANEOUS POWER DISSIPATION OF A CMOS GATE WHEN THE INPUT VOLTAGE CHANGES SLOWLY (MC 14001)

These curves should be considered when the input voltage changes from 0 to V_{DD} in more than 200 ms. A thermal time constant of the IC chip of 50 ms can be used.

Considering a thermal resistance junction-to-air of $0,2^{\circ}\text{C}/\text{mW}$ (plastic package), it can be seen that the temperature rise of the junction is approximately:

$$\Delta t = 8^{\circ}\text{C} \text{ at } V_{DD} = 10V$$

$$\Delta t = 30^{\circ}\text{C} \text{ at } V_{DD} = 15V.$$

These values have to be taken into consideration particularly for operation at high ambient temperatures. The thermal resistance junction-to-air of the ceramic package is approximately $0,15^{\circ}\text{C}/\text{mW}$. The power ratings of the packages are:

D.I.L. plastic : 625mW at 25°C

D.I.L. ceramic : 825mW at 25°C .

nined by the load capacitance and
 lue of 8 pf per output can be
 ncrease the switching time propor-
 lissipation (see previous example).
 onnecting large capacitors
 uits.
 ally limited by the n- or p-channel
 elatively high peak current values
 n a 4-input NOR/NAND gate or a
 or the standard gates and 100 mA
 ical value. It should be mentioned
 ot only the chip temperature
 it may be reduced due to metal

nput" allows the output of a CMOS
 either with the output in a "low"
 erconnection on a single bus system
 vely activated.

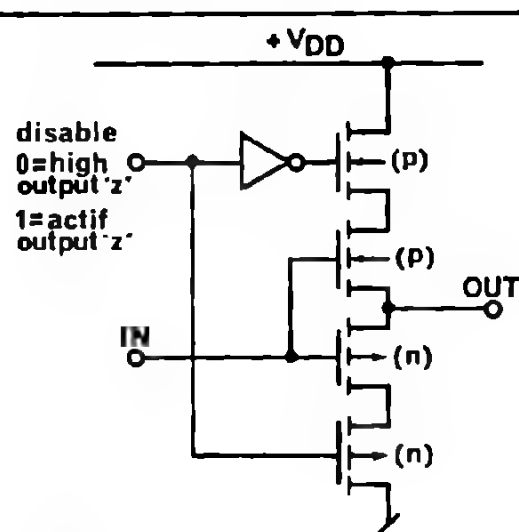


Fig. 19
**TYPICAL CMOS TRISTATE
 OUTPUT STAGE CIRCUIT
 CONFIGURATION**

be used to realize the tristate

haracteristics when the disable input

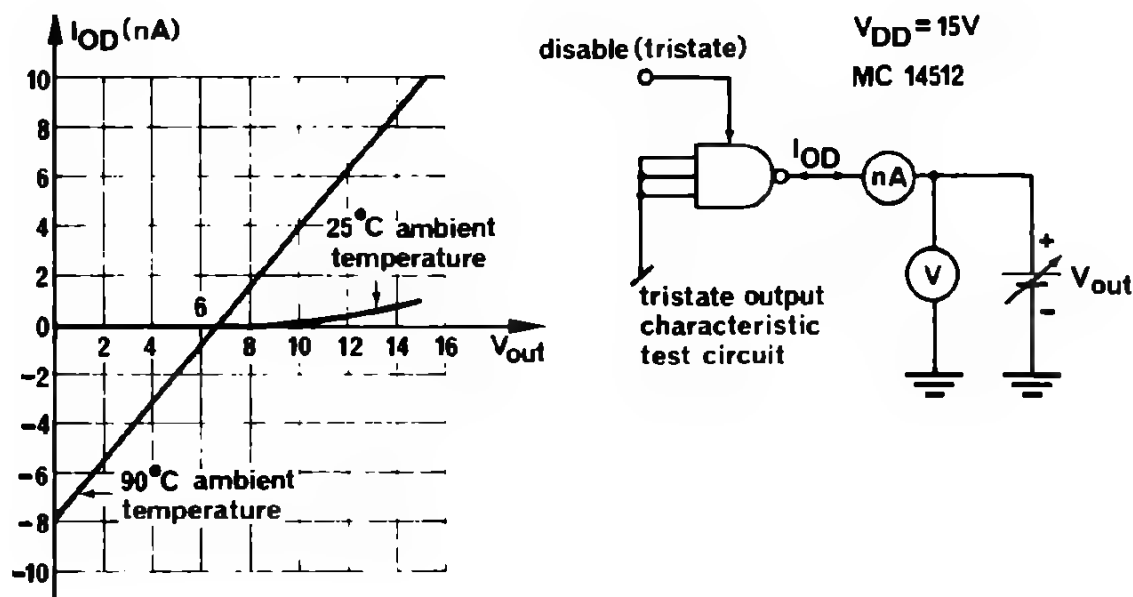


Fig. 20 TYPICAL DC OUTPUT CHARACTERISTIC OF A CMOS OUTPUT BUFFER WHEN THE DISABLE INPUT IS ACTIVE
 $Z_{out} = HIGH$ (MC 14512)

The number of "tristate" devices which can be connected in parallel on one single bus system are practically unlimited, if high speed is not required. As practical design rule, it can be assumed that each tristate connection represents a current load of about 100 nA.

For example:

100 tristate connexions connected on one bus system represent an additional current load on the active output of only 10 μA . This, of course, does not affect the DC noise immunity significantly. The number of devices which can be interconnected is limited only by switching time and supply voltage considerations. In the table given in Figure 20a, the resulting propagation delay obtained on the bus, as a function of the number of interconnected outputs and for $V_{DD} = 5, 10$ and 15V, is shown.

V_{DD} (V)	10	20	50	100
5	360 ns	520 ns	1 μs	1,8 μs
10	140 ns	220 ns	460 ns	860 ns
15	80 ns	110 ns	210 ns	370 ns

Fig. 20a RESULTING PROPAGATION DELAY ON BUS SYSTEM (TRISTATE) WHEN SEVERAL CMOS CIRCUITS ARE INTERCONNECTED

C POWER SUPPLY CONSIDERATIONS

1. VOLTAGE REGULATION

Due to the nature of CMOS circuit operation, an unregulated power supply can be used for CMOS systems. One application example can be seen in chapter 10 A. However, some considerations have to be given to the supply voltage in accordance with certain specific requirements. The choice of the lowest operating voltage will be governed by the minimum required speed and/or the minimum desired noise immunity.

The maximum supply voltage V_{DD} is limited at 18V as breakdown can occur above that value. If devices are operated close to their speed limit, regulation may become necessary in order to keep the lowest voltage above the value where the speed can be guaranteed. Standard zener stabilisation circuit or low cost series voltage regulators can be used.

2. POWER AND CURRENT REQUIREMENTS

In order to calculate the current requirement of a CMOS system, it is necessary to calculate the power dissipation considered under the worst operating conditions. As has been shown in chapter 3, the power dissipation in a CMOS package is determined by:

- the quiescent power dissipation
- the dynamic power dissipation.

2. 1. QUIESCENT POWER DISSIPATION

The quiescent power dissipation is generated by the leakage current of all parasitic PN-junctions in the CMOS circuit. This leakage current usually flows from the supply line V_{DD} to ground. For practical purposes this current can be considered as proportional to the supply voltage and every 10°C it increases by a factor of 2. This means that the quiescent power dissipation changes in the same proportions.

2. 2. DYNAMIC POWER DISSIPATION

The power dissipation increases with frequency according to the law:

$$P_D = f \cdot V^2 \cdot C$$

where f is the frequency, V the supply voltage and C the load capacitance. This law only refers to the power dissipated during switching with a capacitive load or other CMOS circuits. In addition, some power is dissipated through the channels n and p , since they are momentarily both conducting. For a step input, this power is negligible, but it may be necessary to take it into account for very slow switching speeds (see paragraph B8).

The necessary information for the calculation of the system power can be found on all data sheets. The calculation is made by summing all the maximum quiescent and dynamic powers dissipated, device by device, considering the operating frequency of each one. The table in Figure 21 gives examples of dc and ac power consumptions for different CMOS circuits.

V_{DD}	5V		10V		15V		C_L
	dc nW	ac $\mu W/kHz$	dc nW	ac $\mu W/kHz$	dc nW	ac $\mu W/kHz$	
Gates (MC 14001)	25	0,8	50	2,8	100	7	25 pF
Dual FF (MC 14027)	50	1	200	5	400	12	15 pF
Counters (MC 14522)	500	6	1000	20	2000	40	15 pF
Complex functions (MC 14532) (parity encoder)	25	4,3	50	19	350	46	15 pF

Fig. 21 SUMMARY OF TYPICAL POWER DISSIPATION FOR THE MAIN CMOS CIRCUITS

Practical example:

Let us consider a CMOS system with 50 packages comprising:

- 5 counters
- 10 flip-flops
- 15 complex functions
- 20 gates.

In order to simplify the calculation of the power requirements, a table, as indicated in Figure 22, should be used.

ing frequency of the 4 main functions
dissipation per function

power dissipation at 25°C

rection factor $K = 2 \left(\frac{t_{\max} - 25}{10} \right)$

power dissipation at the maximum operating temper
oltage, taking the maximum required frequency into

tion with numerical values, it is seen that a total p
quired. It should be mentioned that most of the pow
ie dynamic operation (99%). The required supply c
only 5 mA!

Average operating frequency kHz	Total power rate μW/kHz	Dynamic power dissipation μW	Total quiescent power dissipation at 25°C μW	Temperature correction factor K	Total quiescent power dissipation at maximum temperature = 80°C μW	Total μW
100	56	5.600	1	50	50	5.650
100	50	5.000	2	50	100	5.100
100	100	10.000	5	50	250	10.250
100	285	28.500	0,75	50	37.50	28.537
/DD = 10V. Grand total						<u>49.537 ≈</u>

**F CALCULATION OF THE POWER REQUIREMEN
TEM**

FILTERING

ed on the dc voltage must be such as:

total supply voltage below the minimum required f
nunity;

total voltage above breakdown.

etermined accordingly. Normally, a ripple of 10 to 20
performance very much with CMOS logic, and filter
sized.

oupling purposes, it is recommended that a capacit
to be used on each CMOS circuitboard.

D INTERFACING CMOS WITH OTHER LOGIC FAMILIES AND DISCRETE DEVICES

In system design, the interface problem between logic families of different nature is always present.

In this section we will consider several situations which show how to interconnect CMOS circuits with the most popular logic families such as TTL, DTL and ECL.

An interface example of CMOS to PMOS as well as to discrete devices will also be shown.

The examples show the interface circuit from CMOS to the different logics and back to CMOS. It should be mentioned that the noise voltage margins are indicated by considering only the guaranteed limits. In practice, the voltage margin is higher because usually only one CMOS gate controls one gate of the other family.

1. CMOS TO TTL INTERFACE

Due to the higher positive logic levels, the noise margin at CMOS-bipolar interface can prove to be higher than that of the bipolar system standing alone.

Here, a 2 k ohm to a 3 k ohm pull-up resistor is recommended to assure adequate positive driving levels to the CMOS device. Notice that a CMOS gate is typically capable of driving a low-power TTL load (LTTL). To increase the output current sinking capability of the CMOS device a 2 or 4 input CMOS NOR gate could be used with all of its gate inputs tied together in parallel. For even higher fan-outs the MC 14049/14050 Hex Buffer is available. This buffer is capable of driving two medium power TTL or two DTL loads with an I_{OL} of 3.2 mA at 0.4 volts.

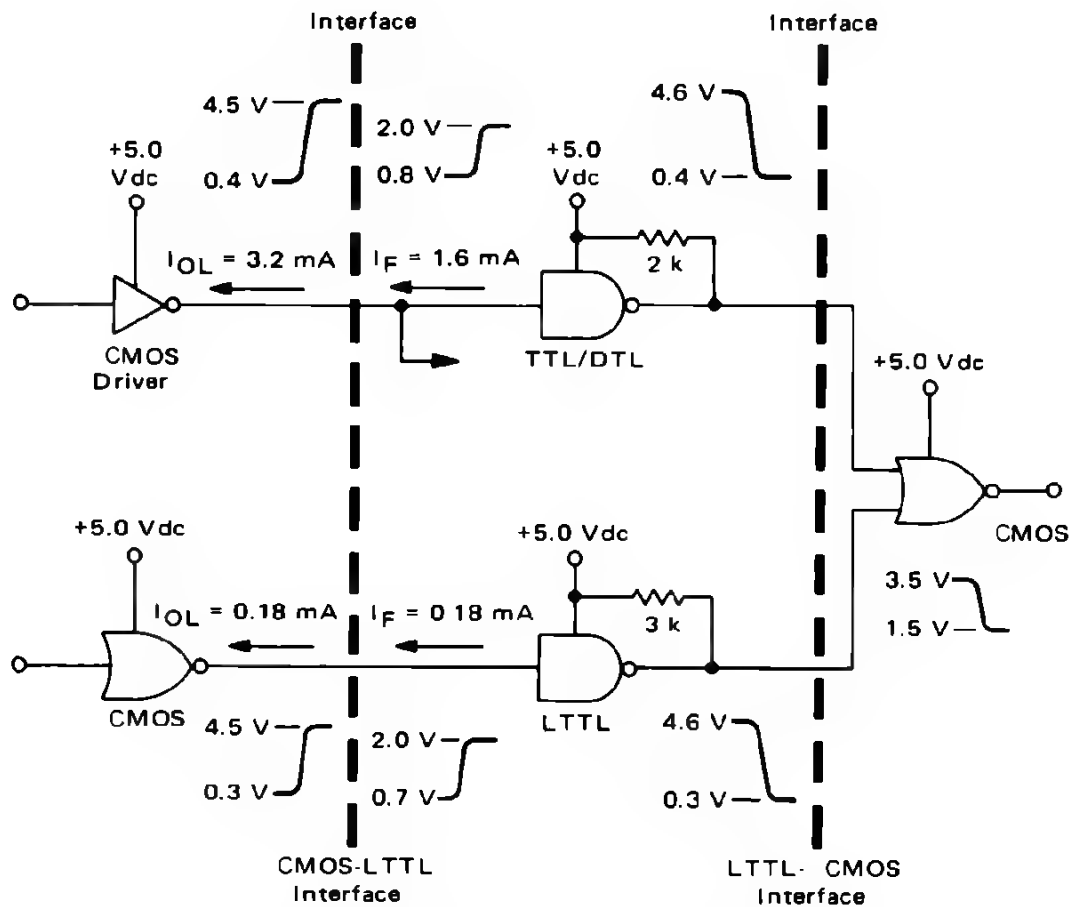


Fig. 23 CMOS TO TTL / DTL INTERFACE

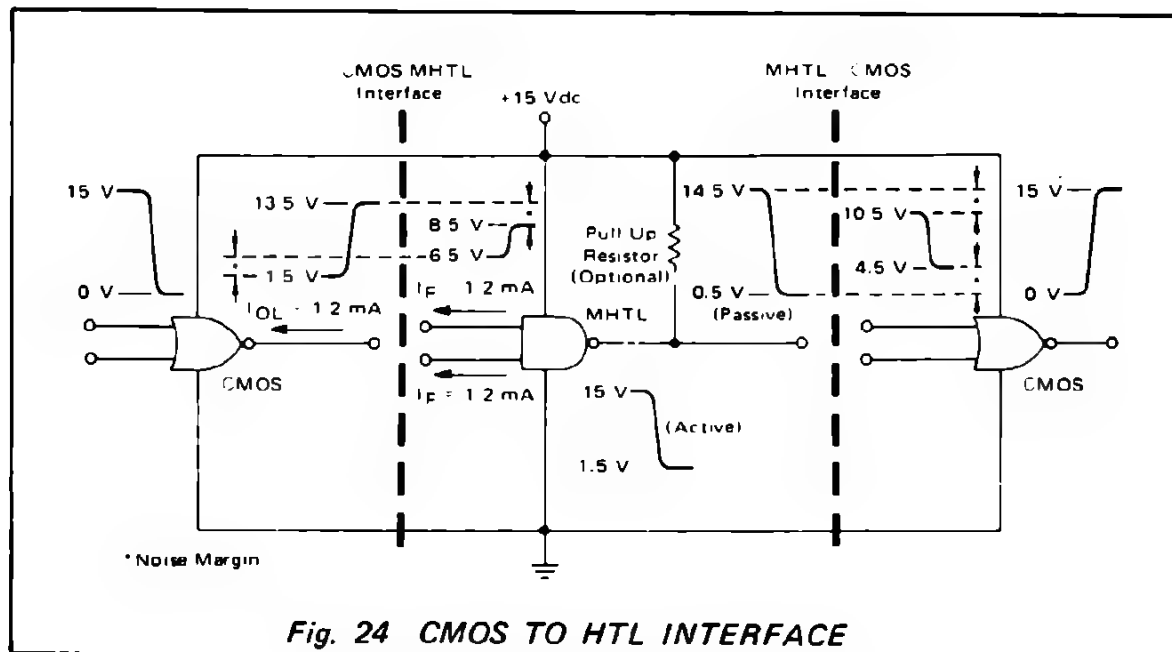
2. CMOS TO HTL INTERFACE

CMOS functions can be used to expand the complexity of standard industrial high threshold logic systems where a large signal swing and high noise immunity are important. HTL is limited in its per device complexity by an inherently high power dissipation, typically 60 mW/logic gate . Not so for CMOS, with a rating of less than $2\text{ }\mu\text{W/gate}$.

So CMOS can be used to provide the complex functions for HTL. In doing so, proper interface of the two types of logic must be implemented as shown below. Here again, both logic types operate from a single supply, $+15\text{ Vdc}$. The CMOS devices here supply output logic level at $V_{OH} = 13.5\text{ V}$ and $V_{OL} = 1.5\text{ V}$. Since HTL responds to signals that exceed V_{IH} of 8.5 V and V_{IL} of 6.5 V , a full 5 V noise margin of HTL exists at the interface of the two logic device types.

HTL can directly drive CMOS with the same slow rise and fall times desired in most HTL systems. A faster output rise time is easily obtained by paralleling an external resistor with the internal HTL "pull-up" resistor.

A passive output HTL circuit with a $2.5\text{ k}\Omega$ pull-up resistor provides a good working circuit with an inherently low saturation voltage. To drive a large number of CMOS gates, an active pull-up HTL circuit can be used, but noise margins will be considerably reduced.



3. CMOS TO ECL INTERFACE

To interface CMOS to ECL (emitter coupled logic) only a single power supply is needed, see Figure 25a. The speed of the overall circuit is limited, however. CMOS cannot operate at its fastest speeds at 5.2V (an ECL requirement) as it can at higher voltages. Note in the schematic that the CMOS gate operates between ground and $-V_{SS}$. This V_{SS} can be any negative voltage within the range of the CMOS device, to a $-18V$, maximum. A clamp diode is used to prevent the ECL input from falling more than a diode drop below $-5.2V$. Level translation is required in order to drive CMOS devices with ECL. (See Figure 25b.) This is due to the fact that the ECL output swing is specified at a minimum 0.7V. This is not enough to drive a silicon bipolar transistor, let alone a CMOS device. By using a 2-input expandable ECL gate, a differential output voltage can be obtained large enough to drive a transistor which in turn drives a CMOS device. When the input to the ECL dual gate is $-0.8V$, both ECL outputs (pins 4 and 6) are also at $-0.8V$. When the input goes to $-1.6V$ on pin 3, then a differential output of 0V on pin 4 and $-1.6V$ on pin 6 results. This is sufficient to drive the translating transistor which switches the CMOS gate. The CMOS gate operates between 0V and $-V_{SS}$ where $-V_{SS}$ can again be as large as $-18V$, maximum. The larger negative values of V_{SS} would allow the CMOS devices to operate at higher speeds.

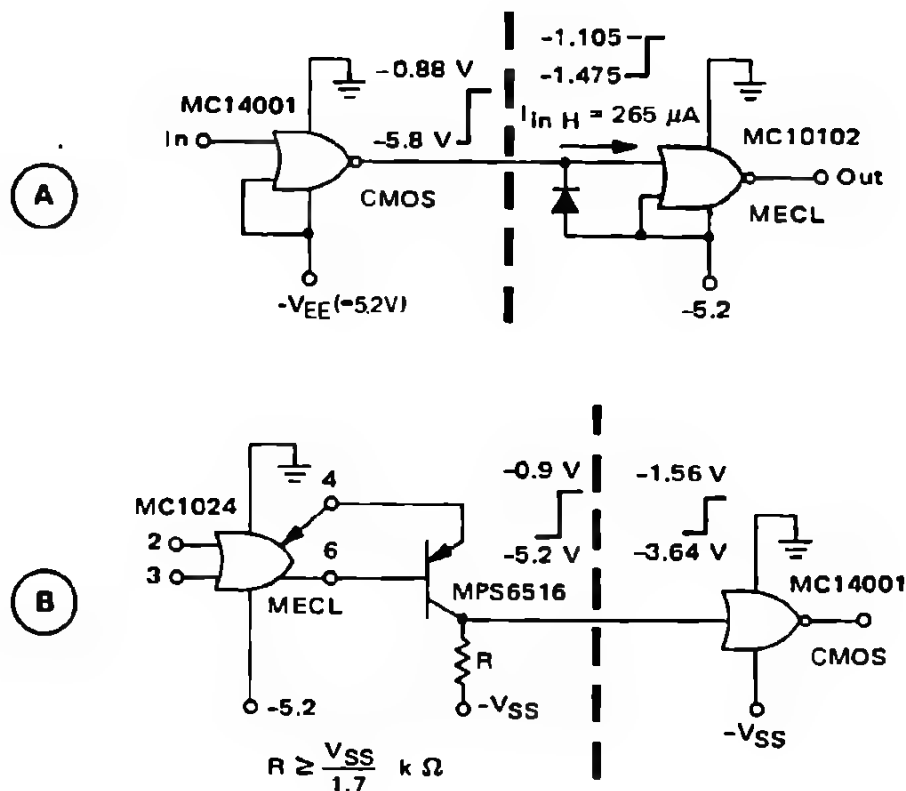


Fig. 25 CMOS TO ECL INTERFACE

The most common MOS devices available today are p-channel high threshold. Becoming more common are low threshold units (silicon gate and $<100>$ devices) capable of direct interface with TTL/DTL bipolar logic. The main difference between the two types is the supply voltage necessary for operation. Typical high threshold supplies are $V_{SS} = 0V$, $V_{DD} = -13V$ and $V_{GG} = -27V$. Corresponding low threshold supplies are $V_{SS} = +5V$, $V_{DD} = -5V$ and $V_{GG} = -12V$. Another important difference to note is that high threshold devices generally use negative logic convention ("0" is the most positive level and "1" the most negative level) while low threshold use positive logic convention. The typical output swing for both high and low threshold devices goes from V_{SS} to V_{DD} when driving the high input impedance of a CMOS logic function. The wide supply range of CMOS and the high input impedance of MOS and CMOS devices make interfacing between them a simple matter. Figure 26a shows CMOS/High Threshold PMOS interface while Figure 26b shows CMOS/Low Threshold PMOS interface.

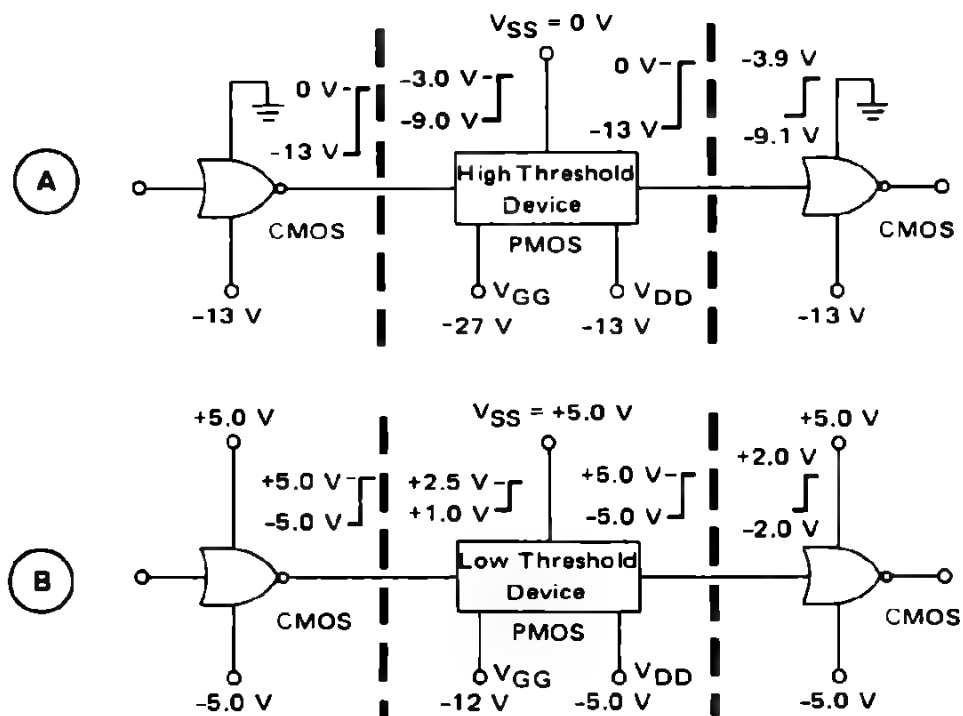


Fig. 26 CMOS TO PMOS DEVICES INTERFACE

CMOS TO DISCRETE TRANSISTOR INTERFACE

is problem is raised when it is required to control heavy loads with CMOS suits.

no basic interface circuits should be considered:

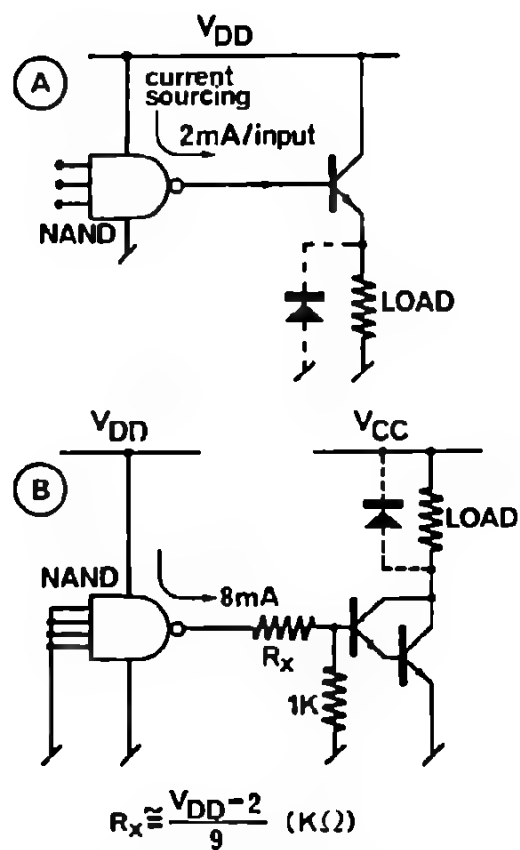


Fig. 27
**CMOS TO DISCRETE
 TRANSISTOR INTERFACE**

E FANOUT CONSIDERATIONS FOR CMOS

In contrast to bipolar logic where the fanout factor is an important limitation, particularly when DC noise margin is considered, the standard fanout factor has a different meaning for CMOS circuits.

One could say that there is practically no DC fanout factor limitation, because there is in principle no voltage noise immunity loss due to the absence of input current (with the exception of the input leakage current generated by the input protection system).

For practical design purposes a DC fanout factor of more than 100 can be applied. However, if speed or fast switching times are required, the dynamic fanout factor becomes an important consideration.

Each additional CMOS input connected to one CMOS output represents an additional load of 5 pF which means that the output time constant is increased accordingly. Figure 28 illustrates the switching times (on/off) of a CMOS gate as a function of the output capacitance and the supply voltage V_{DD} .

Since each CMOS input represents a load of 5 pF, the total capacitance C_L is equal to:

$$C_L = (X \cdot 5) + C_o \text{ (pF)}$$

$$\begin{array}{ll} \text{For } V_{DD} = 5V & C_o = 40 \text{ pF} \\ & = 10V \quad C_o = 20 \text{ pF} \\ & = 15V \quad C_o = 10 \text{ pF} \end{array}$$

where X = number of interconnected inputs.

Therefore, the horizontal axis of the Figure 28 can be directly related to the dynamic fanout factor. As an example, if the maximum required switching speed is 40 ns at $V_{DD} = 10V$, then a maximum fanout factor of 10 should not be exceeded.

In general, the switching time curves are indicated on the data sheet for each product.

Switching
time

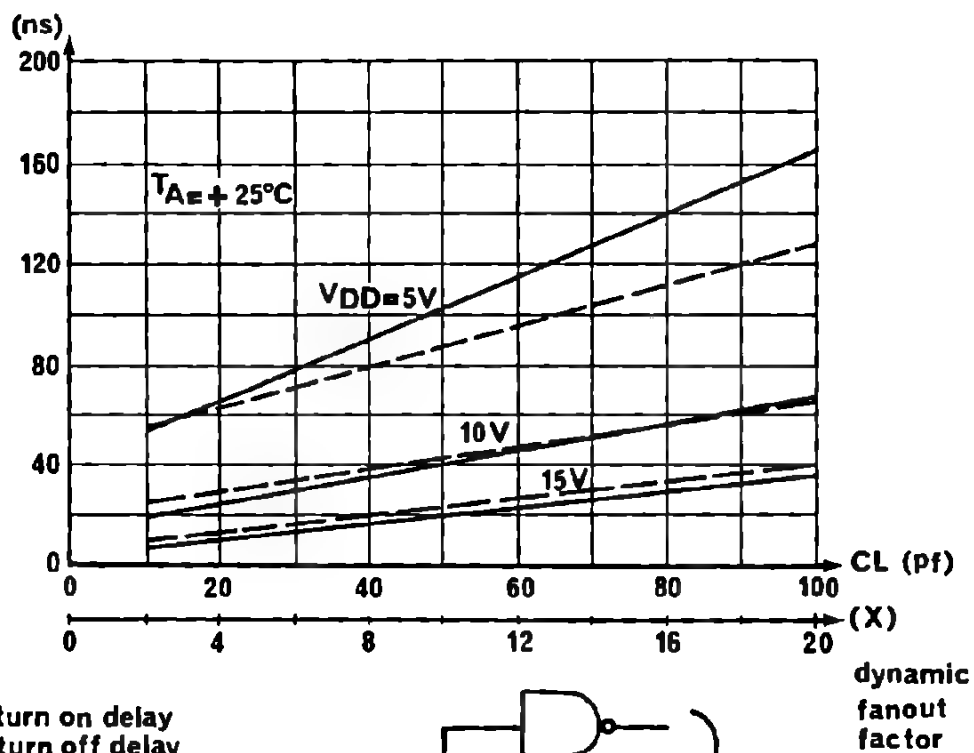


Fig. 28 SWITCHING TIMES AS A FUNCTION OF DYNAMIC FANOUT FACTOR AND SUPPLY VOLTAGE V_{DD}

F INTERCONNECTING CMOS CIRCUITS

Interconnection problems in logic families are usually related to the switching times in conjunction with the length and the nature of the signal transmission lines in a system.

Some typical signal propagation delays for different line systems normally used are given in the following table:

Line specifications	Propagation delays (ns)	Line length
CO-AXIAL with an air-gap 50 Ω	3,9	1 m
CO-AXIAL with polyethylene 50 Ω	5,	1 m
Feeder, TV-75 Ω	5	1 m
Twisted pair (110 Ω)	4,8	1 m
Microstrip line on glass epoxy mod. GR10FR4	5,6	1 m

As can be seen, the signal propagation delay rarely exceeds 5 ns for a distance of one meter between two gates, which, compared to the CMOS switching times, is particularly fast. Therefore, reflections, if they occur, are absorbed during the signal transitions.

When CMOS is driving lines, the waveform is mainly determined by the output characteristics of the circuit, the line in this case only represents an additional capacitive load.

When using NOR or NAND gates as line drivers, the resulting waveforms are asymmetric which is due to the lack of symmetry of the high and low state impedances. When using inverters, the symmetry is improved.

For practical purposes, Figure 29 illustrates an example of the interconnection of two CMOS gates. It shows the maximum frequency that can be transmitted with full noise immunity as a function of the length of the transmission line (twisted pair), with V_{DD} as a parameter. It should be noted that the maximum frequency is defined at the point where raising and falling edges of the signal join together.

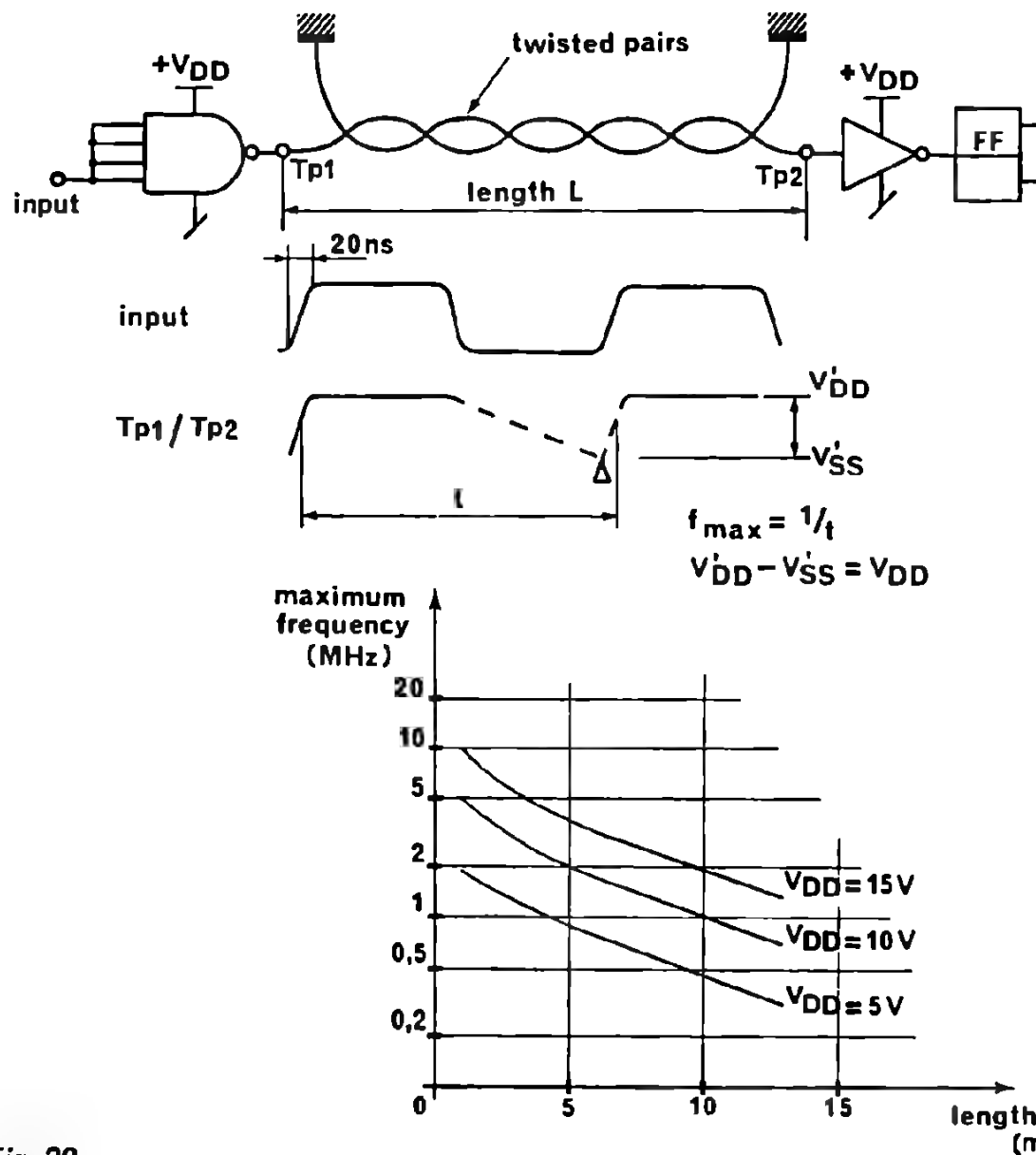


Fig. 29
MAXIMUM TRANSMISSION FREQUENCY OF TWO INTERCONNECTED CMOS GATES AS A FUNCTION OF THE LINE LENGTH FOR $V_{DD}=5, 10, 15V$

CHAPTER 7



Reliability

RELIABILITY



- A INTRODUCTION**
- B HANDLING PRECAUTIONS**
- C RELIABILITY SCREENING**
- D LIFE TEST RESULTS**
- E DERATING OF
RELIABILITY DATA
WITH TEMPERATURE**
- F SOME STATISTICAL
TOOLS FOR THE DESIGN
ENGINEER**

A INTRODUCTION

Quality is referred to as being the degree to which a product meets the requirements of the customer; reliability, the capacity of a product to maintain its quality under specific conditions.

Defective product often involves considerable expense incurred mutually by manufacturer and user, therefore, quality has a definite influence on sales, production increases, and eventually decreasing unit cost. Thus, users express concern about quality and reliability of MC-MOS and should be informed on reliability screening methods and MC-MOS reliability data.

B HANDLING PRECAUTIONS

Caution must be exercised to avoid any electrostatic or high voltage charge from coming in contact with the MC-MOS gate elements. The gate oxide is approximately 1500Å thick and can be ruptured by potentials of 80 volts or greater. Most MC-MOS circuits employ various input protective schemes; however, an electrostatic charge may still cause damage to the gate oxide during the finite time required for the protective device to turn on.

The following handling precautions are recommended for CMOS circuits:

1. All MC-MOS devices should be stored or transported in conductive material so that all exposed leads are shorted together. MC-MOS devices must not be inserted into conventional plastic "snow" or plastic trays of the type used for the storage and transportation of other semiconductor devices.
2. All MC-MOS devices should be placed on a grounded bench surface and the operators should ground themselves prior to handling devices. This is done most effectively by having the operator wear a conductive wrist strap.
3. Nylon smocks should not be worn while handling CMOS circuits.
4. Do not insert or remove MC-MOS devices from test sockets with power applied. Check all power supplies to be used for testing MC-MOS devices and be certain there are no voltage transients present.
5. When lead straightening or hand soldering is necessary, provide ground straps for apparatus used.
6. Do not exceed the maximum electrical voltage ratings specified by the manufacturer.
7. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
8. Cold chambers using CO₂ for cooling should be equipped with baffles and devices must be contained on or in conductive material.

C RELIABILITY SCREENING

The gating method of quality control used at the Motorola CMOS facilities assures the production of reliable MC-MOS devices. From starting material, all the way through to end product shipping, MC-MOS products are processed (gated) through relevant inspection and monitoring steps. These gates provide the necessary built-in check points of the MC-MOS manufacturing process.

The outgoing quality of the MC-MOS product is guaranteed by controlling test procedure documentation and test equipment calibration. An internal detail specification is generated and controlled by the Quality Assurance Department and contains a test plan for the electrical, mechanical, and environmental conditions and/or limits of acceptability. All test documentation (i.e. test programs, procedures, etc.) subordinate to the detail specification is controlled by Quality Assurance. In addition, a Quality Assurance gate inspection during final test operations is designed to detect:

1. Procedure and/or documentation error
2. Equipment malfunctions (by correlation)
3. Operator error (by statistical sampling).

Reliability studies conducted so far on integrated complementary MOS logic units indicate extremely good process parameter stability under prolonged worst-case temperature-stress conditions.

Although stability and reliability are primary concerns during the circuit design phase, utilization of CMOS test patterns on each product wafer permits reliability testing and performance characterization during actual production. These test patterns provide complete device characterization on each wafer, giving information on such parameters as threshold voltage, hole and electron mobility, breakdown voltages, and contact resistances. In addition, other tests determine the fixed interface charge density, the substrate-area surface doping levels and the gate-oxide thickness. Devices in the test site are used to evaluate the extent of mobile ion contamination, and other device degrading phenomena.

WAFER PROCESSING

MC-MOS quality assurance begins with the gating of all starting material. As the material progresses, all critical equipment is monitored for performance within specification. Environmental data is taken on the process area to correct improper trends in air and water quality. Process parameters are charted by wafer lot to evaluate trends before the product is endangered. Primary electrical parameters are charted prior to wafer probe. The documentation of C-V plots provides a major indicator of device reliability.

ASSEMBLY

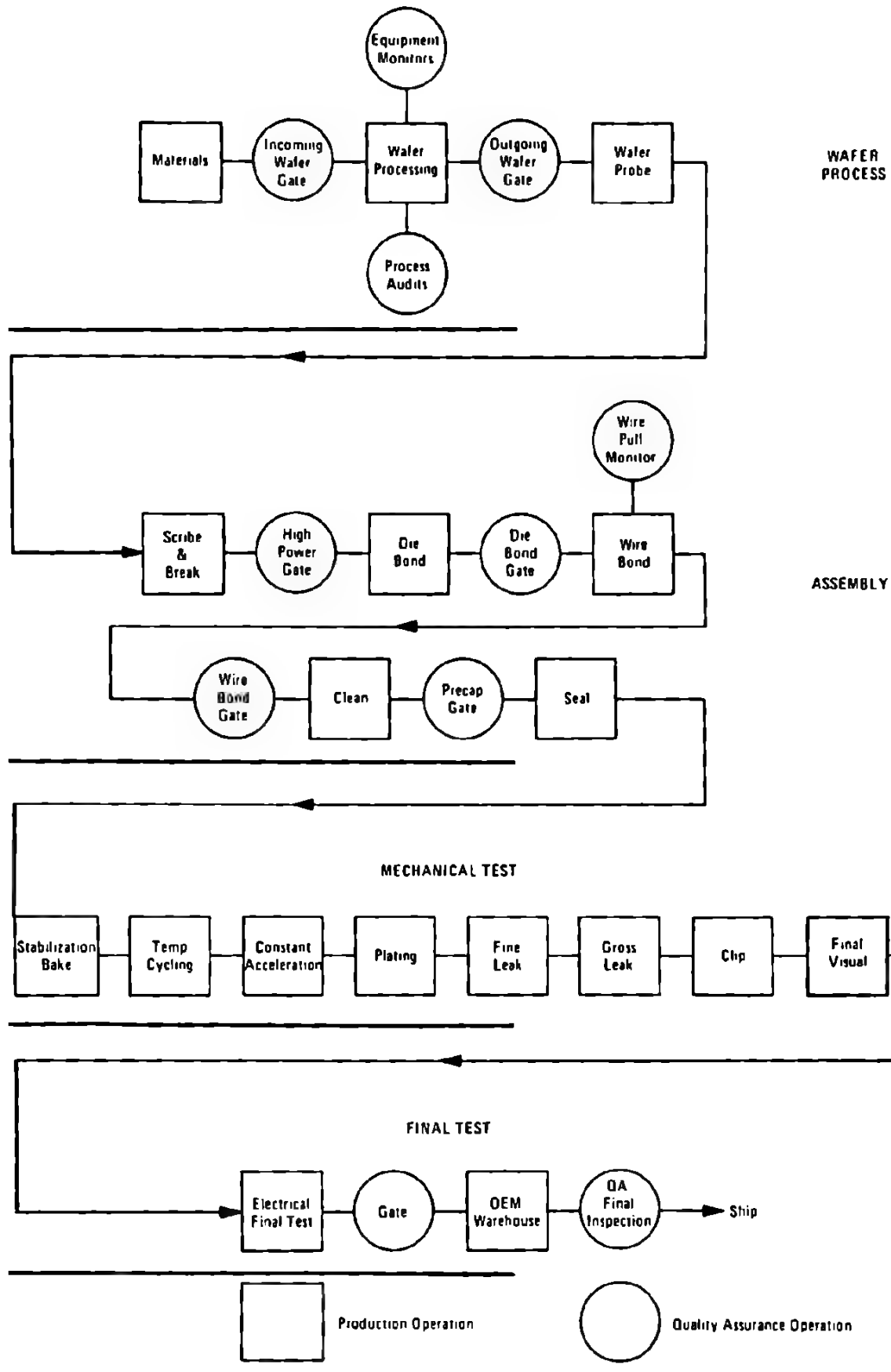
After wafer probe, wafers are scribed, broken, inspected and submitted to a high-power gate inspection. The die are then bonded and submitted to a die bond gate inspection. The units are sent to the wire bond operation next. Each bonding machine is tested when set up, and after every second hour of operation. Wire bond inspection follows the bonding operation.

MECHANICAL TEST

After assembly the product is submitted to a series of mechanical test operations, based on Mil. Std. 883. A 24-hour stabilization bake meets Method 1008 Condition C. It is followed by five temperature cycles in accordance with Method 1010, Condition C. Constant acceleration in the device Y1 axis is performed at Condition D of Method 2001, before the units are plated and leak tested. Fine leak, the only test not done on a 100% basis, is performed to Method 1014, Condition A. Gross leak testing is performed on a 100% basis, using pressure bomb techniques and FC-43 (or equivalent).

FINAL TEST

The final testing of complementary MOS logic circuits is similar to the testing of other digital circuits in that the parameters measured characterize a digital logic family. DC parameters such as V_{OH} , V_{OL} , noise margin, power and input currents, and output sink-source currents are tested to specification.



D LIFE TEST RESULTS

This paragraph gives the detailed data resulting from life tests that were carried out on different MC-MOS devices. It would, however, be too long to explain all test conditions in detail. They can be obtained from MOTOROLA in the form of a complete reliability report, which furthermore has the advantage of being updated periodically.

CMOS FAILURE RATE $125^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$

	Qty.	Device Hours	Rejects	Comments
Gates				
MC14001AL	125	327,200	1	Open, 18V stress
MC14002AL	249	350,000	1	Input gate short, 18V stress
MC14002AL	58	263,232	1	180nA channel, 10V stress
MC14002CP	244	732,000	1	Input gate short, 10V stress
MC14011AL	75	225,000	0	18V stress
MC14012AL	60	276,480	0	10V stress
MC14025AL	36	110,000	2	Degradation, functionally good, 18V stress
MC14501AL	20	10,000	0	18V stress
Total Gates	867	2,283,912	6	
Shift Registers				
MC14021AL	80	240,000	0	10V stress
Decoders, Latches				
MC14514AL	47	141,000	0	10V stress
Memories				
MC14505AL	48	144,000	0	5V stress
Total	1042	2,808,912	6	

CMOS Failure Rate: 0.26%/1000 hours (@ $T_J = 125^{\circ}\text{C}$ (60% confidence level)

MTTF = 380,000

Gates

MC14002AL	30	138,240	0	TA=100°C, 10V stress
MC14012AL	30	138,240	0	TA=100°C, 10V stress

Timepiece

MTD130F	70	150,000	0	TA=70°C, 1.3V stress
MTD134P	16	16,000	0	TA=70°C, 1.3V stress

E DERATING OF RELIABILITY DATA WITH TEMPERATURE

The world is governed by physical laws that all depend to some extent on the temperature. The temperature dependency of the molecular or atomic structure of matter is depicted by what is commonly called statistical mechanics. These statistical laws all depend very strongly on the temperature.

All kinetic processes, as for example chemical reactions, diffusion, evaporation, electromigration and many others exhibit, in general, a temperature dependency of the form:

$$J = A \cdot e^{-B/CT}$$

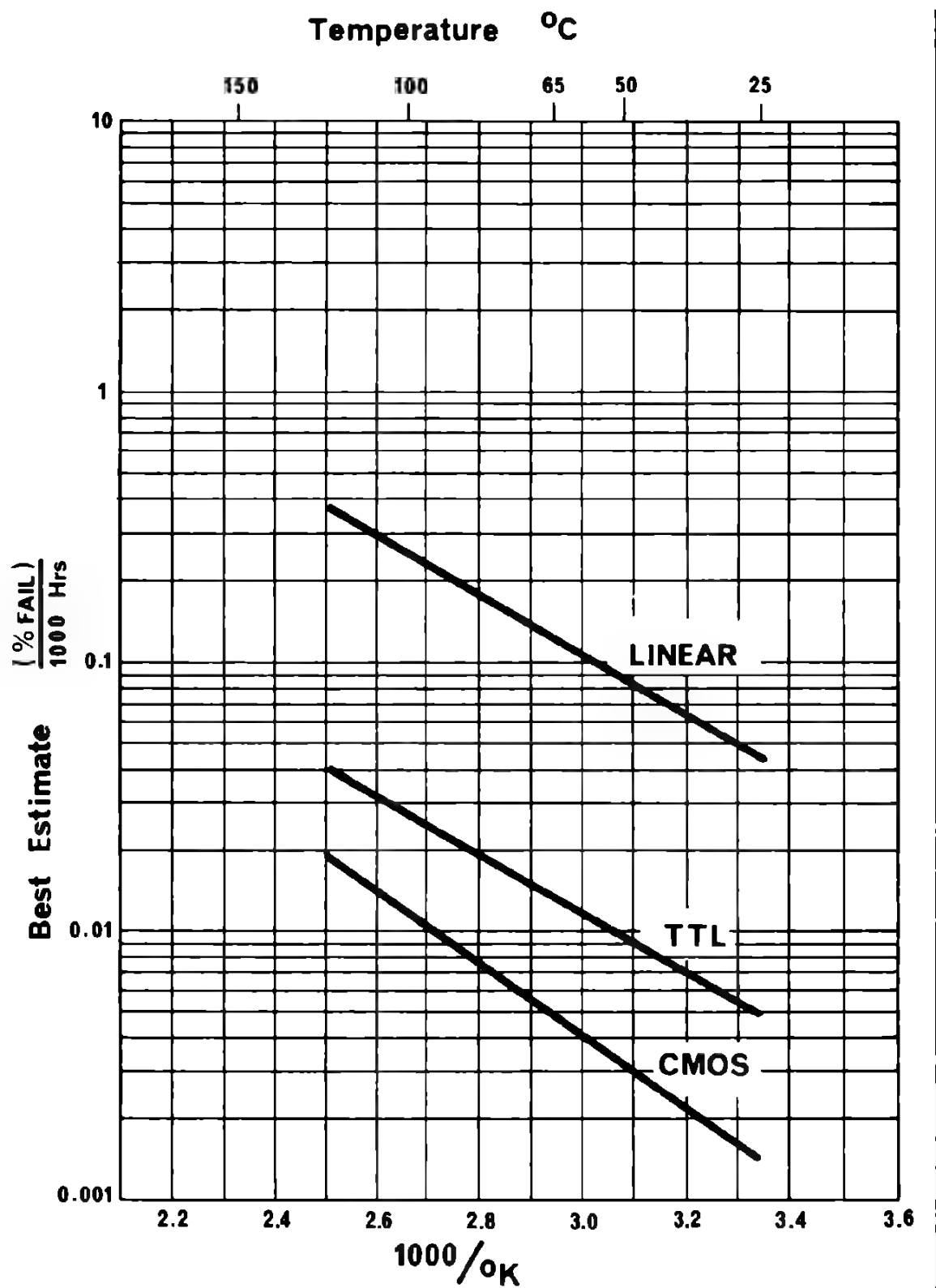
Where A, B and C are material dependent constants, T is the absolute temperature and J is the intensity of the considered process. The plot of the logarithm of J versus the reciprocal absolute temperature yields therefore a straight line with negative slope. These plots are often referred to as Arrhenius plots.

It is therefore not surprising that similar curves are found if the failure rate of semiconductor devices is plotted in the same way as a function of the reciprocal absolute temperature.

These failure-rate data, however, cannot in general be exactly calculated by theoretical means, because too many parameters are involved. The data have therefore to be obtained from practical life tests at different temperatures, a job that may take years of data collecting, logging and evaluation.

Nevertheless these data are very interesting to the design engineer and enable him to predict the reliability of a system at different temperatures.

We therefore give here some experimental data on the temperature dependency of the failure rate of CMOS. We also include, for comparison purposes, the corresponding curves for linear IC's and TTL IC's.



F SOME STATISTICAL TOOLS FOR THE DESIGN ENGINEER

BERNOULLI TRIALS, THE BINOMIAL DISTRIBUTION AND THE POISSON EXPONENTIAL APPROXIMATION

Repeated independent trials are called Bernoulli trials if there are only two possible outcomes for each trial and if their probabilities remain the same throughout the trials.

It is usual to denote the two probabilities by p and q . p and q are obviously not negative and $p + q = 1$.

One is frequently interested only in the total number of outcomes with probability p in a succession of n Bernoulli trials, but not in their order. It can be shown that the probability b_k in n Bernoulli trials with probabilities p for success and $q = 1 - p$ for failure resulting in k successes and $n - k$ failures equals:

$$b_k = p^k q^{(n-k)} \frac{n(n-1)(n-2) \cdots (n-k+1)}{k!} \quad \underline{\hspace{10em}} \quad \mathbf{1}$$

This function is called the binomial distribution.

Taking a sample of size n from a population of lot of transistors having p per cent defective corresponds to n Bernoulli trials; the probability b_k of finding k defective transistors in the sample is given by the formula stated above.

Quite often one seeks the probability of getting up to k successes in n trials. This probability, that may be denoted here by $b_{(0 \rightarrow k)}$, is found by summation of the individual probabilities given by equation (1):

$$\begin{aligned} b_{(0 \rightarrow k)} &= b_1 + b_2 + \cdots + b_k = \sum_{i=0}^k \binom{n}{i} p^i q^{(n-i)} = \\ &= q^n + q^{(n-1)} p \cdot n + q^{(n-2)} p^2 \frac{n(n-1)}{2!} + \cdots + q^{(n-k)} p^k \frac{n(n-1)(n-2) \cdots (n-k+1)}{k!} \end{aligned} \quad \underline{\hspace{10em}} \quad \mathbf{2}$$

The probability of getting more than k successes, denoted herewith by $b_{(k+1 \rightarrow n)}$, is again found by summation of equation (1), but this time from $(k+1)$ to n :

$$\begin{aligned} b_{(k+1 \rightarrow n)} &= b_{k+1} + b_{k+2} + \cdots + b_n = \sum_{i=k+1}^n \binom{n}{i} p^i q^{(n-i)} = \\ &= p^{(k+1)} q^{(n-k-1)} \cdot \frac{n(n-1)(n-2) \cdots (n-k)}{(k+1)!} + \cdots + p^{(n-1)} q + p^n \end{aligned} \quad \underline{\hspace{10em}} \quad \mathbf{3}$$

The probability to find anything between 0 and n successes is obviously equal to:

$$b_{(0 \rightarrow n)} = b_0 + b_1 + \dots + b_n$$

4

It may be noticed here that the sum given in equation (4) is equal to:

$$b_{(0 \rightarrow n)} = (p+q)^n = 1$$

5

This result is not further surprising, because it is obvious to find any number between 0 and n successes in n trials.

However, these summations are somewhat cumbersome and fortunately the binomial distribution can be approximated by the so called Poisson distribution, if the following conditions are satisfied:

p must be relatively small ($p < 0.1$), n has to be fairly large ($n > 16$), but small compared to the lot size (less than $1/10$).

Using the Poisson approximation, equation (1) becomes:

$$b_k = \frac{(pn)^k}{k!} e^{-pn}$$

6

It is easier to sum this expression up than equation (1).

The probabilities $b_{(0 \rightarrow k)}$ and $b_{(k+1 \rightarrow n)}$ become with equation (6):

$$b_{(0 \rightarrow k)} = e^{-pn} \left[1 + pn + \frac{(pn)^2}{2!} + \dots + \frac{(pn)^k}{k!} \right]$$

7

$$b_{(k+1 \rightarrow n)} = e^{-pn} \left[\frac{(pn)^{k+1}}{(k+1)!} + \frac{(pn)^{k+2}}{(k+2)!} + \dots + \frac{(pn)^n}{n!} \right]$$

8

Again

$$b_{(0 \rightarrow n)} = b_1 + b_2 + \dots + b_n = 1$$

$$b_{(0 \rightarrow n)} = e^{-pn} \left[1 + \frac{pn}{1!} + \frac{(pn)^2}{2!} + \dots + \frac{(pn)^n}{n!} \right] = e^{-pn} [e^{+pn}] = 1$$

9

RELIABILITY ENGINEERING AND QUALITY CONTROL TERMINOLOGY

In quality control and reliability one is in general interested in knowing the probability of acceptance P_a of a lot having p percent defectives, by taking a sample of size n from the lot. The sampling criteria are established such that the lot is accepted if the number of defectives found in the sample is equal or less than the so called acceptance number c . In terms of the former paragraph, P_a is equivalent to $b_{(0 \rightarrow k)}$ and c is equivalent to k . As it has also been shown in the former paragraph, the acceptance probability P_a has to be computed from the Poisson density function by summation. Fortunately the results are available in the graphical form shown below. This graph of the so-called Poisson curves is of fundamental interest and allows calculation of:

confidence levels of failure rate data

reliability of systems

AQL's and LTPD's.

The Poisson curves yield the probability P_a of not rejecting a lot with p or less percent defectives, if a sample of size n is taken from it that exhibits not more than c failures. The conditions n and c are referred to as the sampling plan.

Obviously $(1-P_a)$ is the probability of rejecting the lot. $(1-P_a)$ is therefore the probability of elimination of the lots having equal or more than p percent defectives. $(1-P_a)$ can be called confidence level and we will introduce the notation $P_c=1-P_a$.

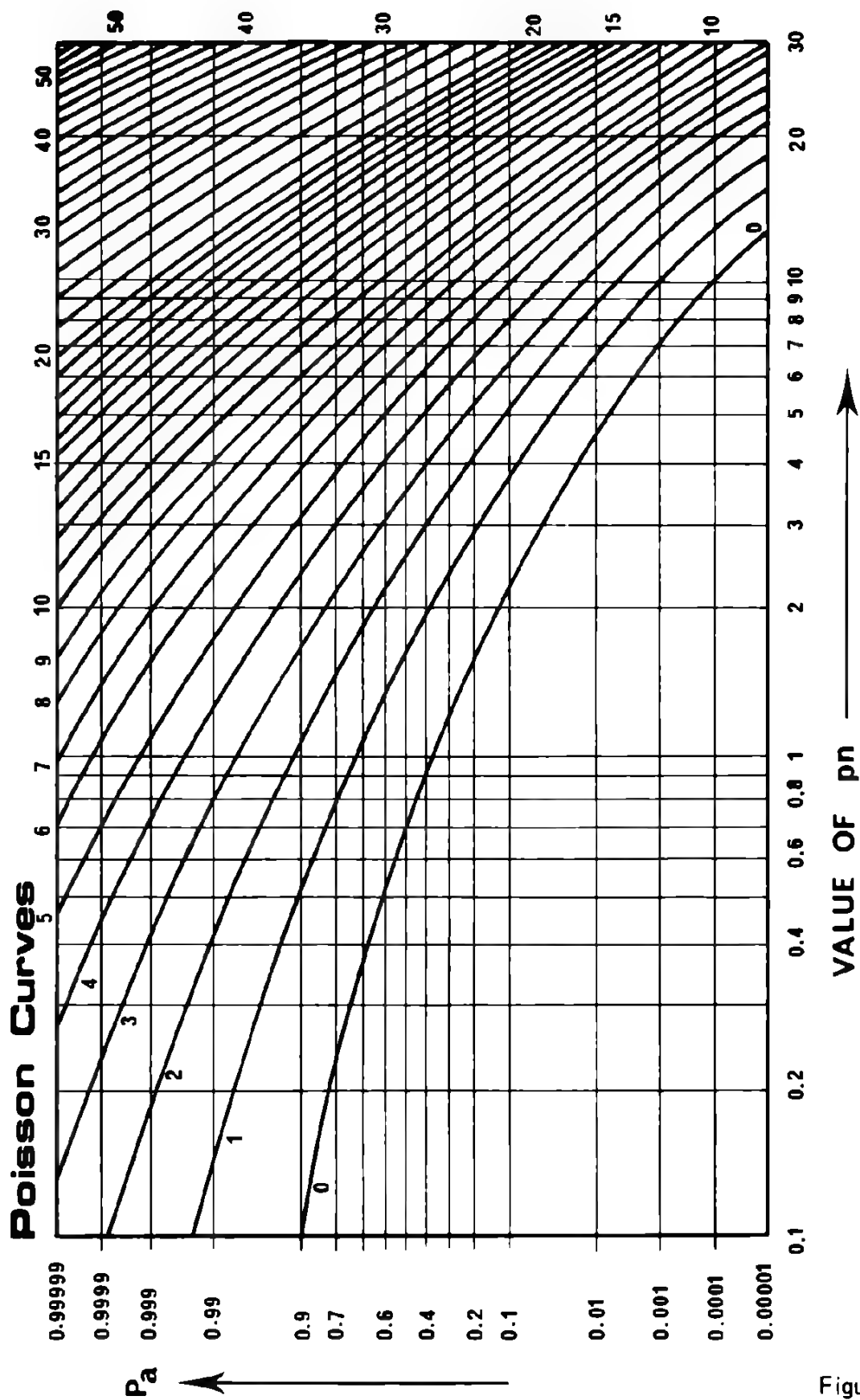


Figure 1

EXAMPLES

1. Determining the confidence level of life test data:

Assuming that in a life test of $n = 1.5 \cdot 10^6$ device hours, 5 devices failed. What is the failure rate in percent per 1.000 hours at a confidence level $P_c = 75\%$?

The sample size n equals $1.5 \cdot 10^6$ device hours.

The acceptance number c equals 5.

Procedure:

- Enter the Poisson curves from the left at $P_a = 1 - P_c$. Draw a horizontal line and determine the intersection with the curve $c=5$.
- From this point of intersection draw a vertical line and determine the intersection with the abscissa. This yields the value of $p \cdot n = 7.5$.
- From the value of $p \cdot n$, p is easily calculated if n is known.

Example:

The above mentioned data yield a failure rate of 0,5% per 1.000 hours at a confidence level of 75%.

Note:

An indication of the failure rate and the confidence level only is not sufficient. The sampling plan must also be known.

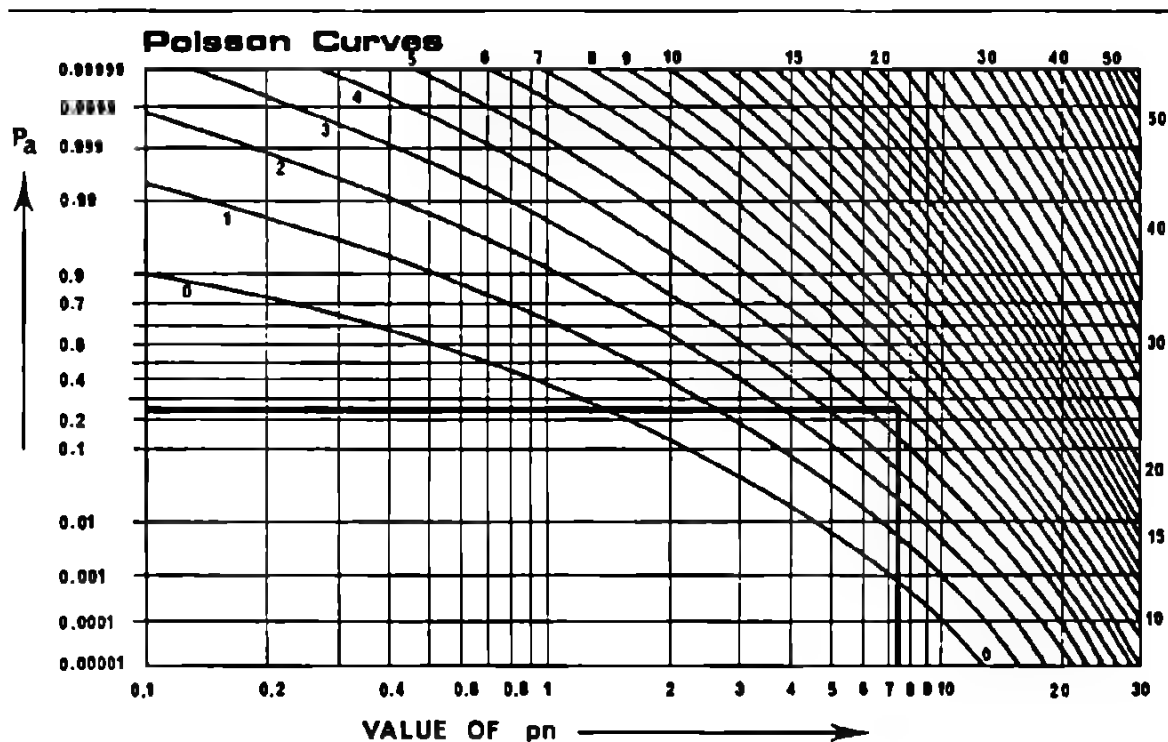


Figure 2

2. Determining the reliability of a system:

How many hours T can a system consisting of m devices be expected to work without any failure with a confidence of 90% if the failure rate is given by the life test data from the former paragraph.

Using the procedure from the former paragraph we find $p \cdot n = 9.5$ and consequently $p = 0.63\%$ per 1,000 hours for $c=5$ and at a level of 90%.

For $c=0$ at the same confidence level $p \cdot n = 2.3$. With p equal to 0.63% per 1,000 hours, n becomes $3.65 \cdot 10^5$ device hours. Because $n = m \cdot T$, T is equal to n/m . For $m=50$, T becomes:

$$T = \frac{3.65 \cdot 10^5}{50} = 7,300 \text{ hours.}$$

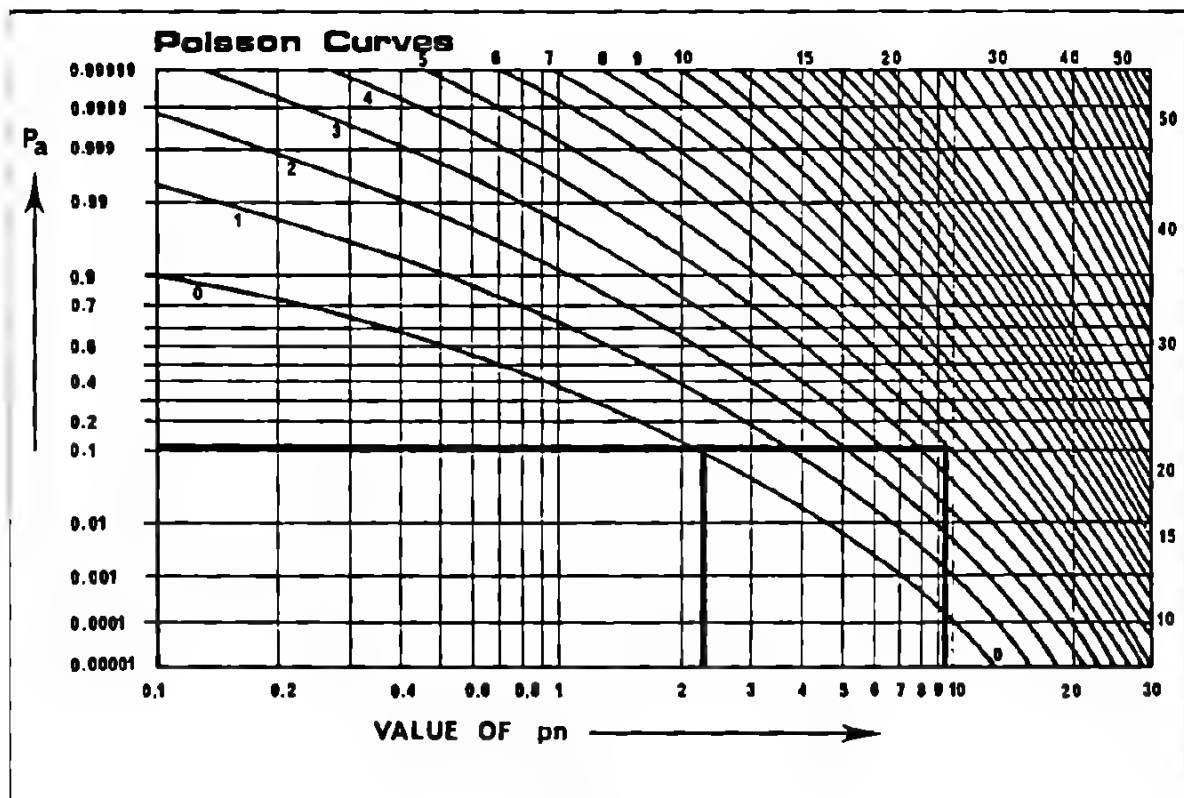


Figure 3

3. Acceptance sampling:

Assuming that from a population or lot with $p_1 = 5$ percent defective units a sample of size $n = 100$ is drawn. How many defective devices can be tolerated in that sample, if 95% of the lots shall be accepted having equal or less than 5% defective units.

Starting with $P_a = 95\%$ and $p_1 \cdot n = 5$ we find from the poisson graph by drawing the corresponding vertical and horizontal lines that $c = 8$.

For this sampling plan ($n = 100$, $c = 8$), the number p_1 is called Acceptance Quality Level (AQL), which in this case is equal to 5%.

If we seek for this same sampling plan ($n = 100$, $c = 8$), the percentage p_2 of defectives corresponding to an acceptance probability P_a of 10% we find that p_2 must be equal to 13% by drawing a horizontal line through the point $P_a = 0.1$ and by determining its intersection with the curve $c = 8$. p_2 is called the Lot Tolerance Percent Defective (LTPD).

This sampling plan obviously guarantees the manufacturer that he rejects only 5% of lots having equal or less than 5% defective (AQL). On the other hand it guarantees the customer that the risk of receiving a lot with more than 13% defectives is only 10% (LTPD).

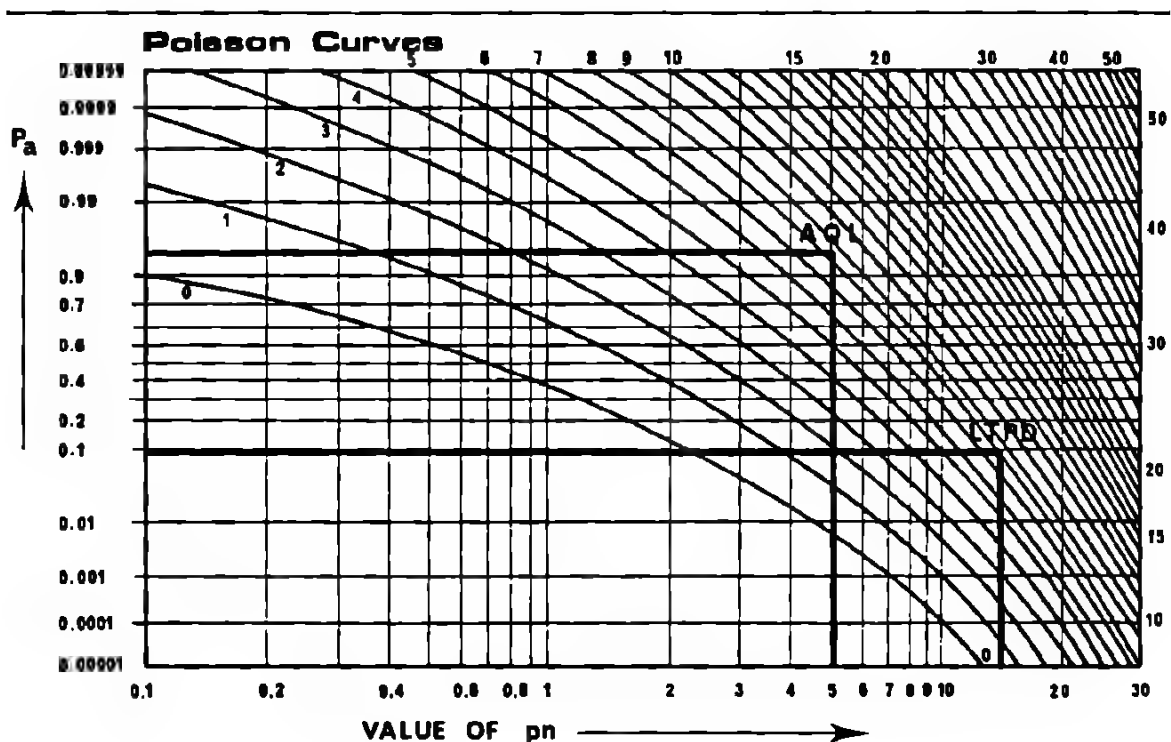


Figure 4

CHAPTER 8



Analog Basic
Circuits

ANALOG BASIC CIRCUITS

A INTRODUCTION

B CMOS INVERTER AS AN AMPLIFIER

1. BIASING CIRCUITS
2. STABILITY OF THE BIAS POINT
3. POWER SUPPLY REQUIREMENTS
4. LINEARITY
5. VOLTAGE GAIN AND PHASE CHARACTERISTICS

C PRACTICAL AMPLIFICATION CIRCUITS

1. D.C. AMPLIFICATION
2. A.C. AMPLIFICATION
3. CASCADE CONNECTION OF CMOS INVERTERS
4. NOISE IN CMOS INVERTERS

D OSCILLATORS USING CMOS INVERTERS

1. FREQUENCY SELECTIVE FEEDBACK OSCILLATOR
2. CRYSTAL OSCILLATOR
3. ASTABLE MULTIVIBRATORS

E MONOSTABLE MULTIVIBRATORS

1. DISCRETE GATE MONOSTABLE MULTIVIBRATORS
2. MONOSTABLE MULTIVIBRATOR MC 14528

F SCHMITT TRIGGERS

1. CMOS AMPLIFIER WITH POSITIVE FEEDBACK
2. 2-INPUT GATES AS SCHMITT TRIGGERS
3. DUAL SCHMITT TRIGGER MC 14583
4. MULTI-INPUT GATES

G ANALOG SWITCHING

A INTRODUCTION

The family of CMOS logic devices is primarily intended for use in handling digital signals. The fact that the elements of the family may be used for analog signals also, should be regarded as an additional bonus. As will become evident, there are few analog parameters that could not be better realised individually in using presently available linear microcircuits. However, the major advantage of CMOS in this context lies in the combination of its various parameters, which is unique to the family. Very often it is desirable to process analog signals in systems which otherwise contain only CMOS digital blocks. Situations may arise where it is inconvenient to provide the additional power supplies required by many linear microcircuits, or where there are already a number of unused gates available in a complex logic block.

It is important to realise at the outset, that the specifications of the digital elements are not presented in the data-sheets in a form which permits a guaranteed performance to be obtained in an analog circuit. For this reason, a number of measurements have been performed on various commonly used gates in order to indicate some "typical values" of the parameters usually used when specifying linear microcircuits. The gates discussed in this chapter are NAND ($\frac{1}{4}$ MC 14011) with one and two active inputs, NOR ($\frac{1}{4}$ MC 14001) with one and two active inputs and invert ($\frac{1}{3}$ MC 14007). The parameters measured are used to describe various analog type circuits which may frequently be found in juxtaposition with CMOS logic.

There is one kind of CMOS circuit that is intended specifically for analog/digital use. This is the analog multiplex circuit, using transmission gate switches that are digitally controlled, such circuits are briefly discussed in the last section of this chapter.

B CMOS INVERTER AS AN AMPLIFIER

A fundamental unit used in CMOS logic is the inverter. This has been described in great detail earlier, in discussing CMOS characteristics; but to set the scene again, a brief summary follows here.

The inverter consists essentially of a pair of complementary MOSFETs connected across the supply voltage. The gate inputs to the MOSFETs are connected together to form the inverter input, whilst the output is taken from the common source/drain terminal between the pair, as shown in Figure 1.

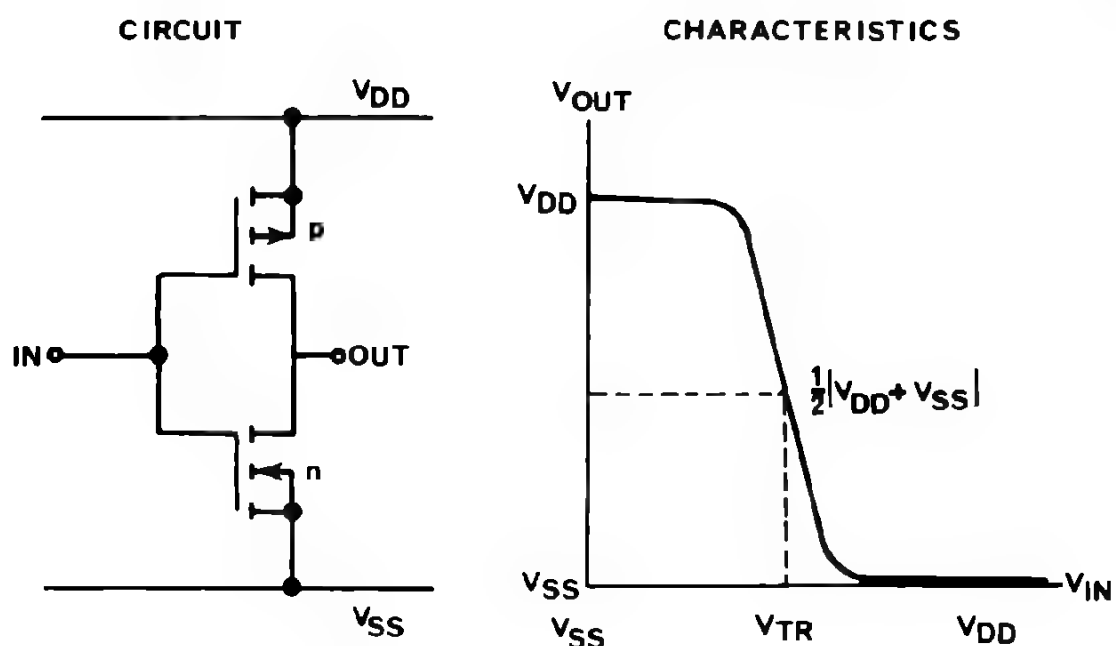


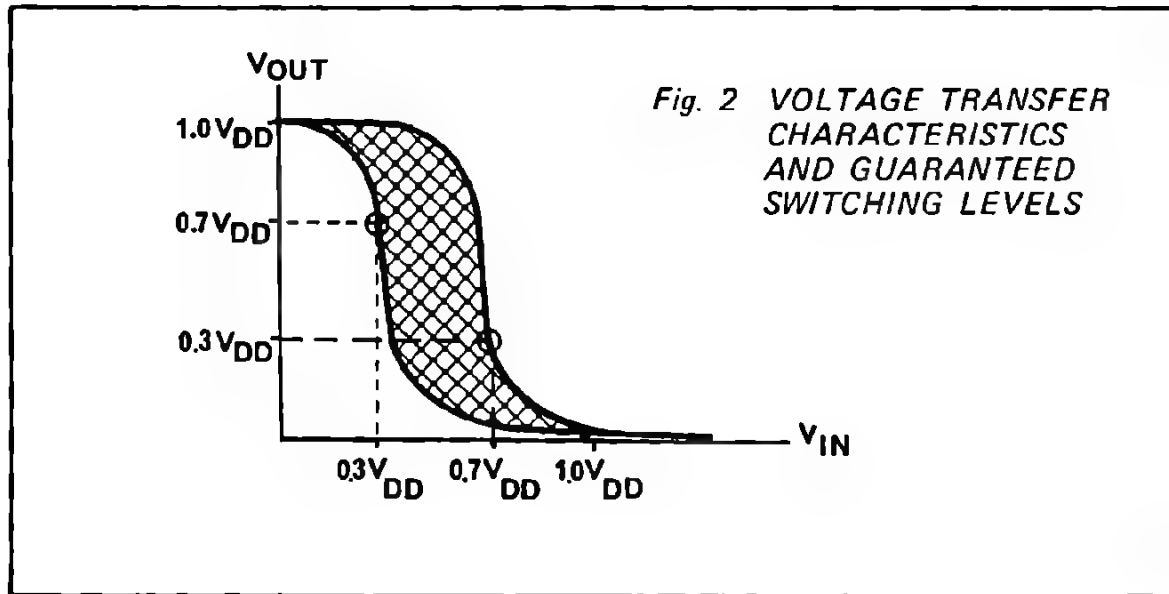
Fig. 1 CMOS INVERTER

The steady-state voltage transfer characteristics of this inverter are evidently those due to the pair of complementary MOSFETs.

In logic circuits, it is required that changes in input level cause the inverter output to switch between V_{DD} and V_{SS} (in the rest of this chapter, for the sake of simplicity, V_{SS} is assumed to be zero volts and V_{DD} the positive voltage supply). In switching, the inverter should spend the minimum possible time in transition between the logic levels.

The slope of the transfer curve in the transfer region (around $V_{DD}/2$) should therefore be as steep as possible. In contrast, for analog applications, the inverter is deliberately biased into this region, and the slope of the transfer characteristics at the bias point gives the small-signal a.c. gain of the inverter.

Before proceeding further in this discussion, it must again be emphasised that, from the specifications of CMOS gates as digital circuit elements, it is only possible to guarantee the transfer voltage, V_{TR} , within a very wide tolerance ($V_{DD}/2 \pm 40\%$). The slope of the transfer characteristics cannot be determined at all from the specifications on the data-sheet, since only two extreme values are used in checking the threshold limits. Figure 2 shows an envelope of the voltage transfer curves for CMOS with the two extreme values indicated.



This leads to the conclusion that, for analog applications, it is necessary to base the design upon values found in practice for a number of different commonly used gates, details of which will be enlarged on in subsequent sections of this chapter.

1. BIASING CIRCUITS

Depending on the amplification characteristics required, the bias point can, in theory, be chosen. However, in practice, owing to the large differences in the voltage transfer curve which may occur from inverter to inverter, biasing to obtain the required amplification can really only be achieved by selecting and adjusting an individual biasing circuit for each gate (Fig. 3).

This inevitable situation is undesirable, since it contravenes good electronic design practice, where all circuit parameters should, if possible, be defined by high tolerance passive components in the circuit.

A bias circuit which is very often used, because it requires no current drain from the power supply, involves a direct feedback from output to input through a high valued (e.g. 50 megohms) resistor, R_1 , as in Figure 4.

The inverter is then biased to the intersection point of the d.c. load line, $V_{OUT} = V_{IN}$, and the actual voltage transfer curve of the inverter. With this very simple connection, the bias point is established with $V_{IN} = V_{OUT} = \frac{V_{DD}}{2} \pm 40\%$ and this will usually be adequate for most a.c. amplification requirements.

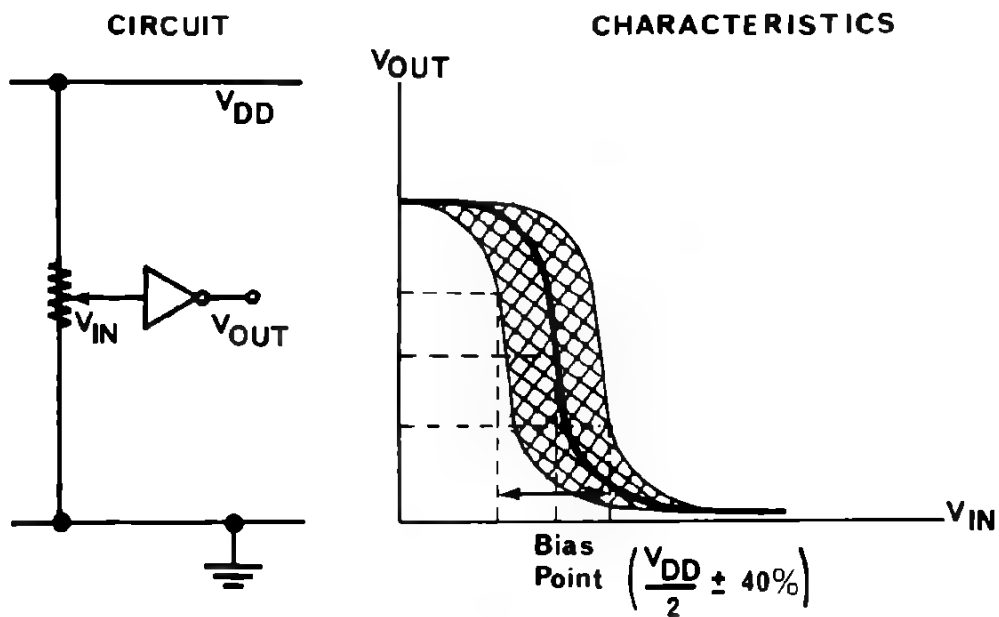


Fig. 3 INDIVIDUAL BIASING ADJUSTMENT FOR CMOS INVERTER

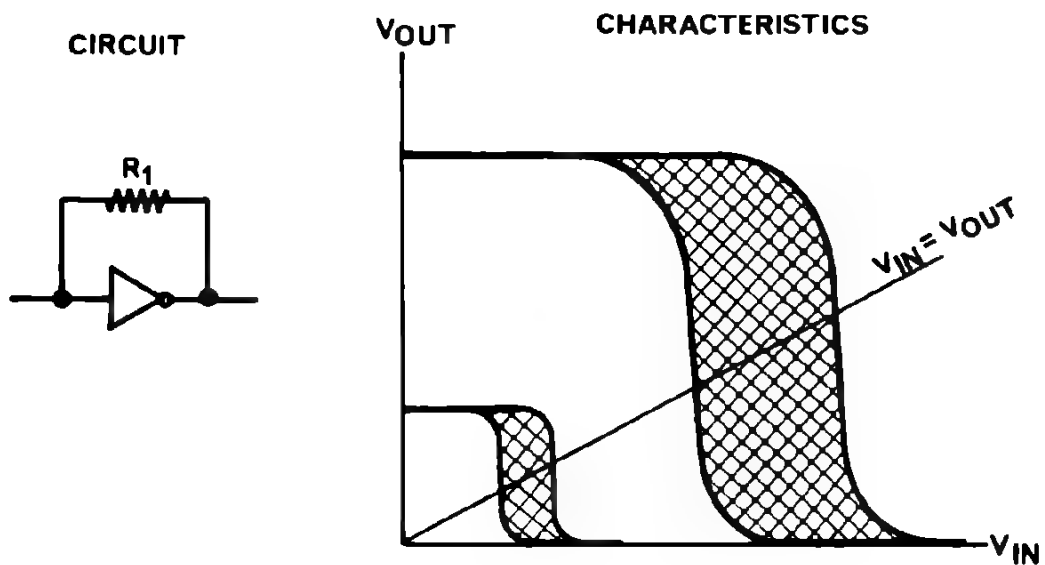


Fig. 4 SIMPLE SINGLE RESISTOR BIASING OF AN INVERTER

frequently, a combination of this circuit, Figure 4, and that of Figure 3, is encountered in the forms shown in Figure 5.

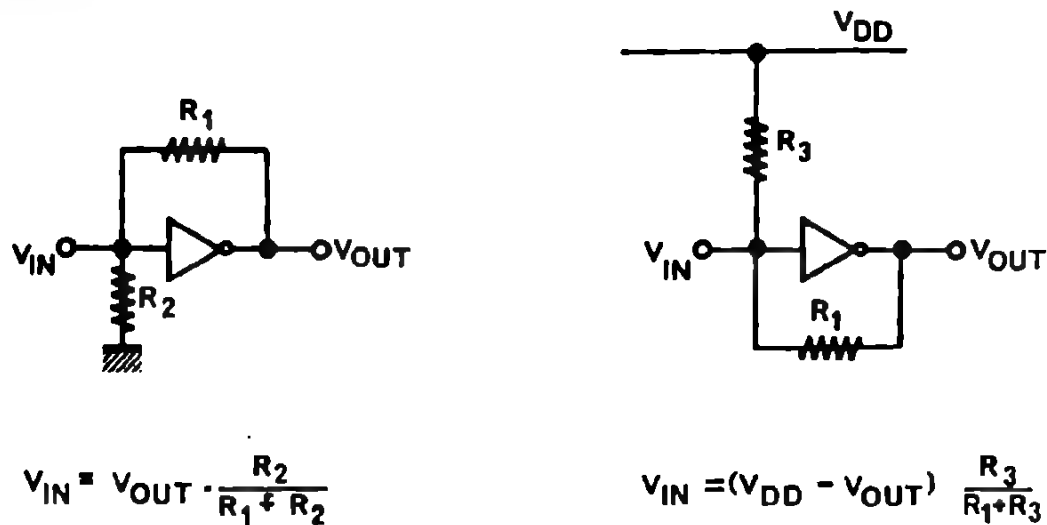


Fig. 5 CIRCUITS FOR ADJUSTING THE BIAS POINT

Effectively this allows variation of the slope of the d.c. load line by varying R_1 , and will permit individual inverters to be biased exactly at $\frac{V_{DD}}{2}$, or to any region of the characteristic curve desired.

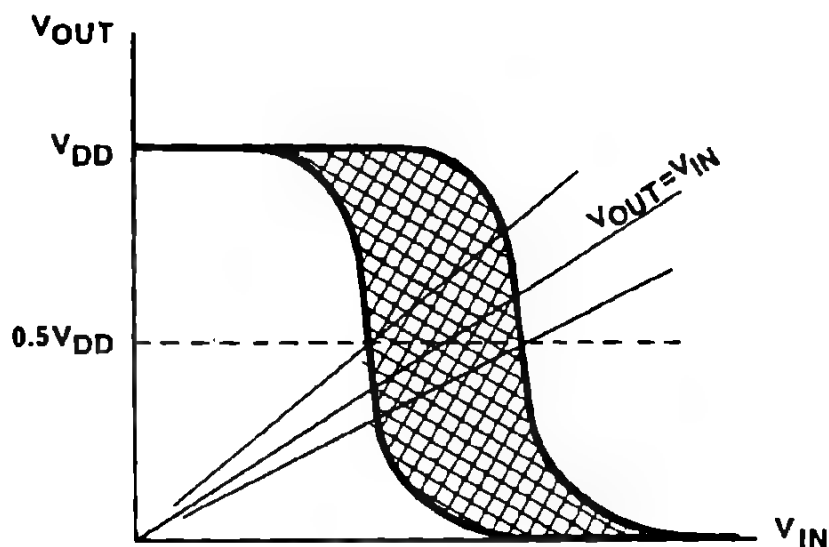


Fig. 6 USE OF BIAS TO OBTAIN $V_{OUT} = \frac{V_{DD}}{2}$

2. STABILITY OF THE BIAS POINT

Having established the bias, some measure is now required of the stability of this point when faced with variations of power supply voltage and also temperature.

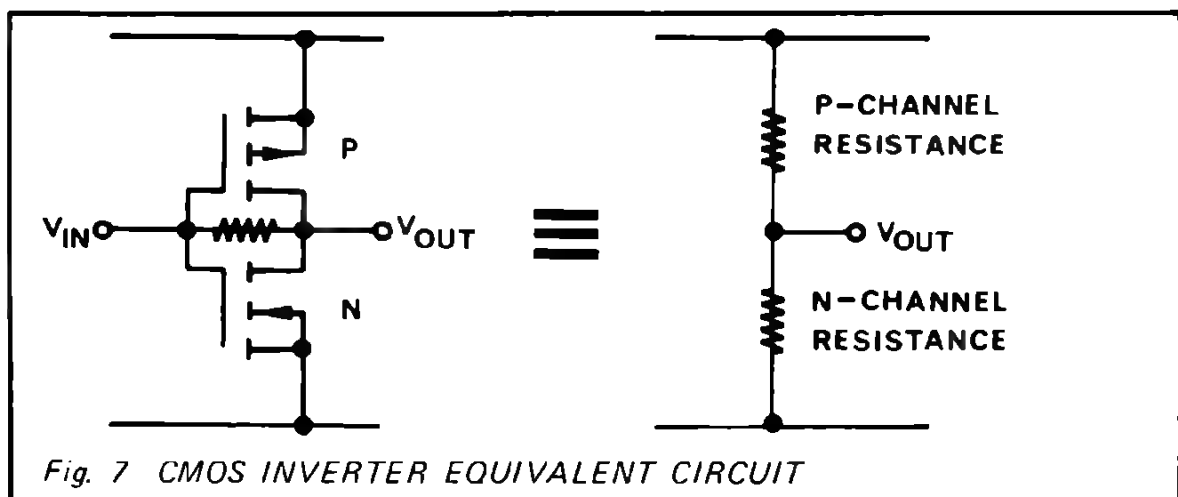
In principle, a small variation, ΔV_{DD} , of the supply voltage will result in a maximum change in the output voltage such that

$$\Delta V_{OUT} = \frac{\Delta V_{DD}}{2}$$

when the inverter is biased to $V_{OUT} = \frac{V_{DD}}{2}$

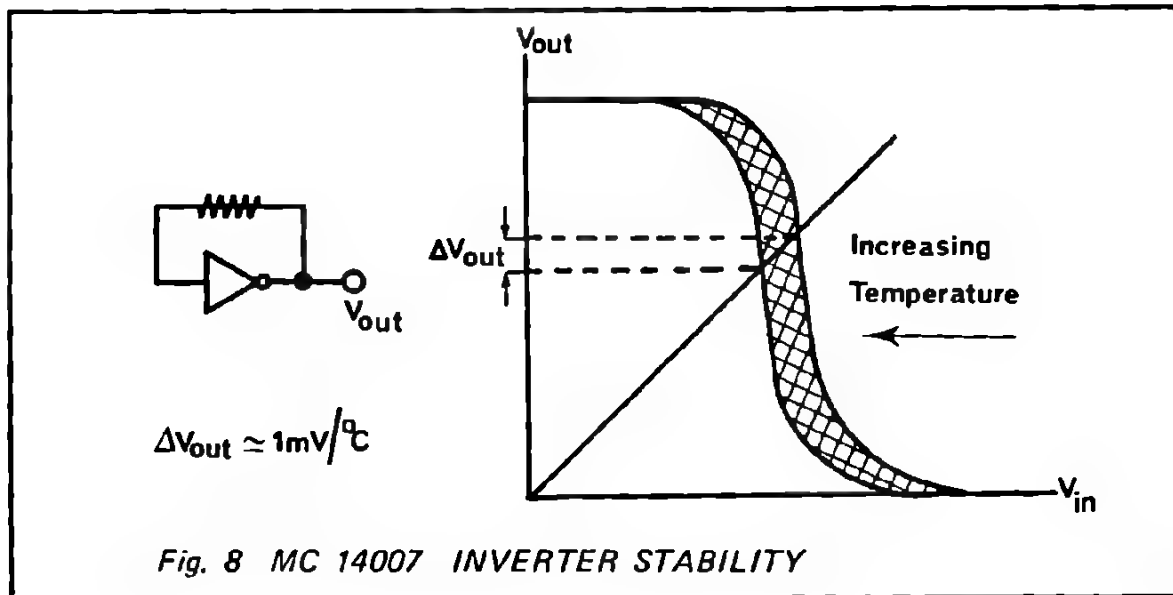
In comparison with operational amplifiers, usually having about 70 dB rejection of power supply variation, the 6 dB obtained here is extremely meagre. It could well cause some difficulty in a system designed primarily with logic in mind, since the power supplies used with CMOS logic do not necessarily need to be well stabilized.

In a biased inverter containing only one n-channel and one p-channel transistor, the variation of the output voltage with temperature evidently depends on the change of resistance of the individual transistors. The channel resistance itself depends on the applied voltage levels as well as on the physical dimensions of the transistors. Measurements have been made showing that the temperature coefficient of resistance of typical transistors is in the region of 0.3% per degree centigrade over a wide variety of operating conditions.



From the equivalent circuit shown in Figure 7 above, it can be seen that it is the differential temperature coefficient of n-channel and p-channel transistors which gives the stability of the bias point for the simple inverter.

Measurements carried out on the MC 14007 inverter with simple single resistor biasing showed that the stability appears to be nearly independent of actual voltage supply levels and can be specified merely by the temperature change, as indicated in Figure 8.



This effect appears as a distortion in the transfer characteristics, involving a gradual shift to the left of the curves. When there is more than a single pair of transistors, as in the MC 14011 NAND or MC 14001 NOR-gates, the form of external biasing will have some influence on the output voltage stability. An indication of the effects can be obtained from the approximate equivalent circuits shown in Figure 9. The figures for ΔV_{OUT} are typical values determined in practice with V_{DD} at 10 volts.

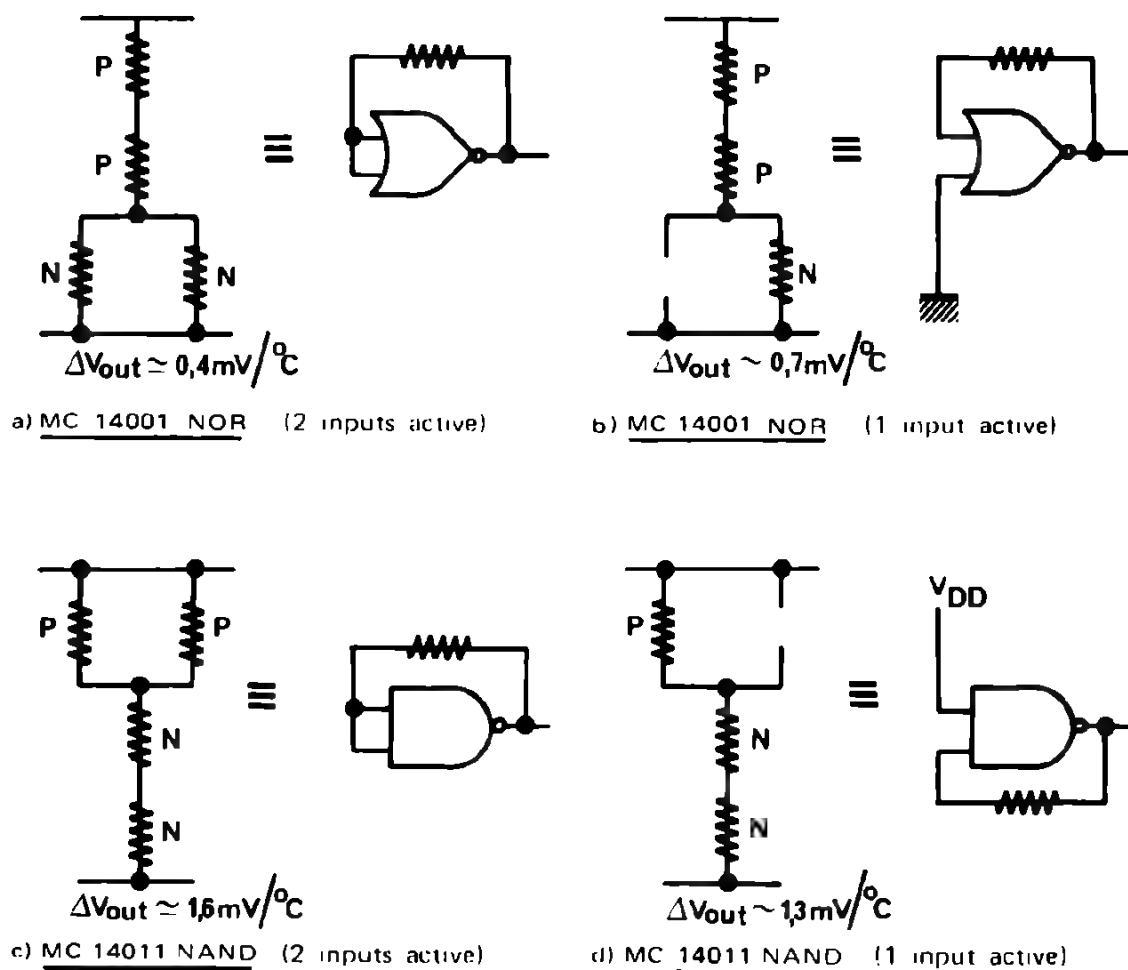


Fig. 9 INVERTER EQUIVALENT CIRCUITS

I. POWER SUPPLY REQUIREMENTS

The voltage range of the power supplies used for logic gates, when connected as amplifiers, will be somewhat different from the range specified on the data-sheet for digital switching applications.

In digital circuits, the lower voltage limit for the supplies is based on the threshold voltage of the individual MOSFETs. In the MOTOROLA MC 14xxx family, it is guaranteed that the inverter will switch with a 3 volts (minimum) power supply.

Analog applications require that the supply voltage be greater than the sum of the threshold voltages of the p-channel and n-channel transistors making up the CMOS inverter. This is necessary in order to have both transistors conducting simultaneously, to fix the bias point. In analog applications at least 4 volts is usually required practically for operation of these circuits.

In digital applications, the upper voltage limit is set by the breakdown voltage of the junctions (for MC 14xxx, 18 volts). For analog applications, this remains the same, however, a more practical limitation is imposed in that the current drain per pin of the CMOS block should be less than 10 mA. In addition, consideration must be given to the maximum power dissipation capabilities of the chip. In an inverter with both n-channel and p-channel transistors conducting, the limit is almost certainly reached before the voltage approaches 18 volts. Because the channel resistances depend on the supply voltage and the current drain depends also on the bias, it is not possible to set safe upper voltage limits for all the CMOS family in analog circuits. Each application requires analysis to ensure that the current drain is not exceeded with the supply voltage chosen.

4. LINEARITY

Before entering into discussions on the voltage gain/phase characteristics of logic gates biased according to the techniques described in section 2, one should examine the linearity of such circuits. Most so-called linear microcircuits are not actually linear in open-loop operation, however, this is of small consequence because there is usually so much voltage gain available (100,000 is not unusual) that linearisation is achieved by applying a large amount of external feedback. In the case of CMOS gates, it is unlikely that voltage gains exceeding 100 times will be available from a simple inverter and therefore the linearity of the basic circuit becomes important.

When biased such that $V_{OUT} = V_{IN}$, the bias point is commonly assumed to be in the region of maximum gain and linearity for small signal amplification. It has already been pointed out in discussing CMOS characteristics that owing to the different surface mobilities of electrons ($400\text{--}470\text{ cm}^2/\text{volt-sec.}$) and holes ($180\text{--}200\text{ cm}^2/\text{volt-sec.}$), the characteristics of n-channel MOSFETs are not quantitatively complementary to p-channel MOSFETs. Adjustments have to be made to the channel length to width ratio ($\frac{L}{W}$) of the transistors to provide similar values for p-channel and n-channel. This is necessary in order to bring the CMOS transfer voltage to exactly $V_{DD}/2$, and should result in perfect complementation of the characteristics (all other factors being assumed equal). If this condition is not met (as seems unlikely with the transfer voltage tolerance set at $\pm 40\%$), then the region around $V_{DD}/2$, where there is maximum gain, must be highly non-linear. In any case, those gates with multiple transistors (MC 14001, MC 14011) can never be linear around this point due to the parallel/series combinations of transistors.

Some typical examples of the distortion obtained with the three different gates, biased as inverters by a single resistor (Fig. 7, 9a, 9c) are indicated here, for a 5mV pk-pk input at 10 kHz.

		Harmonic content in decibels below fundamental						
Inverter Type ($V_{OUT}=V_{IN}$)	V_{DD}	2nd	3rd	4th	5th	6th	7th	8th
MC14007	5	28	33	41	47	55	60	67
	10	28	35	46	52	62	68	74
	15	28	37	48	58	64	70	—
MC14011 (2 inputs)	5	28	35	44	52	60	66	73
	10	28	38	48	58	68	72	—
	15	26	38	52	62	—	—	—
MC14001 (2 inputs)	5	30	15	36	24	43	33	48
	10	30	14	36	22	42	30	46
	15	30	15	36	25	44	35	48

It is interesting to observe how the distortion changes according to the bias point chosen. The largest errors always occur when the biasing is such that $V_{OUT} = V_{IN}$, but this reduces as the gates are biased further into either the p-region or the n-region. The figures quoted below are taken with $V_{DD} = 10$ volts.

		Harmonic content in decibels below fundamental				
Inverter Type ($V_{DD}=10V$)	Bias Voltage	Gain	2nd	3rd	4th	5th
MC14007	2.9	26dB	28	36	46	55
	2.5	20dB	27	38	51	62
	1.1	0dB	—	—	—	—
MC14011 (2 inputs)	5.1	26dB	27	17	38	32
	7.3	20dB	29	27	50	55
	9.2	0dB	48	—	—	—
MC14001 (2 inputs)	6.2	26dB	25	35	46	54
	6.8	20dB	26	40	54	66
	9.5	0dB	—	—	—	—

i. VOLTAGE GAIN AND PHASE CHARACTERISTICS

Due to the high degree of distortion present in CMOS-gate inverters (20% harmonics not being uncommon), accurate measurement of voltage gain and phase is not feasible. As a guide though, the graphs in Figure 10 below give some indication of the typical small-signal gain/phase characteristics which may be anticipated. The different levels of voltage gain shown are obtained here by biasing the gate away from the point where $V_{OUT} = V_{IN}$, maintaining V_{DD} at 0 volts. The measurements were made with an input of 5 mV pk-pk at 10 kHz, and this is used throughout the tests described here, where a small input signal is required.

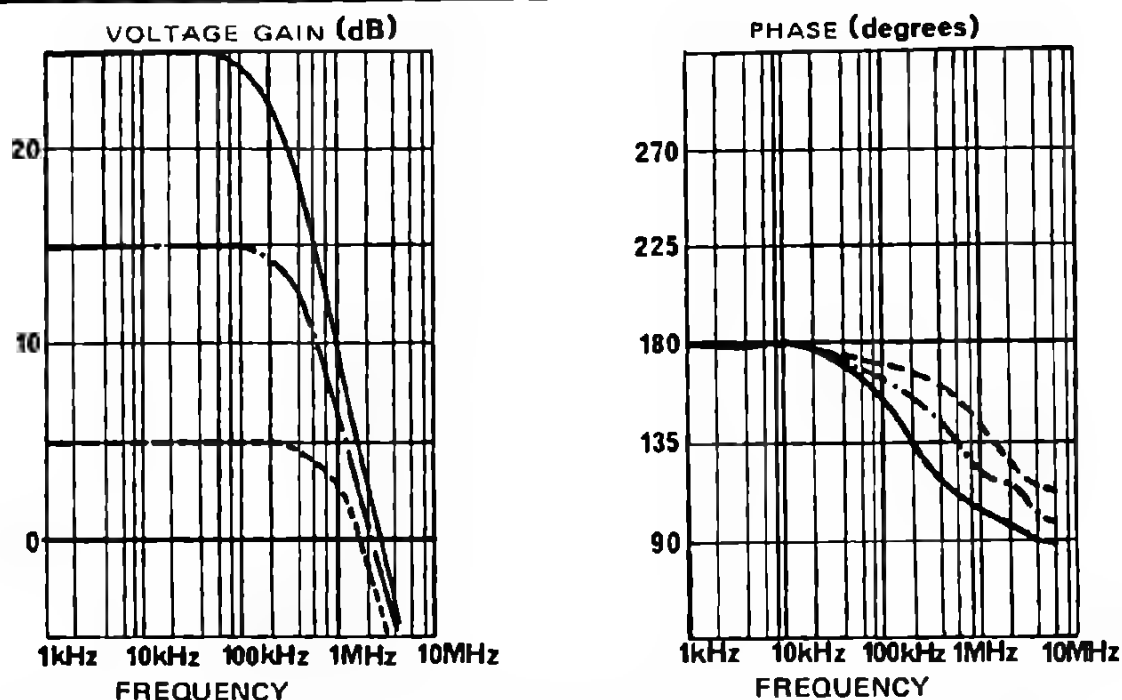


Fig.10 TYPICAL FREQUENCY RESPONSE OF A CMOS-GATE INVERTER

In some systems, it may be of interest to choose to use certain types of gates because of their particular amplification characteristics. The graph, Figure 11 shows some values of gain versus bias point for a number of different gates. This may prove useful in choosing a suitable circuit, although it must always be remembered that the tolerances are such that these curves may vary

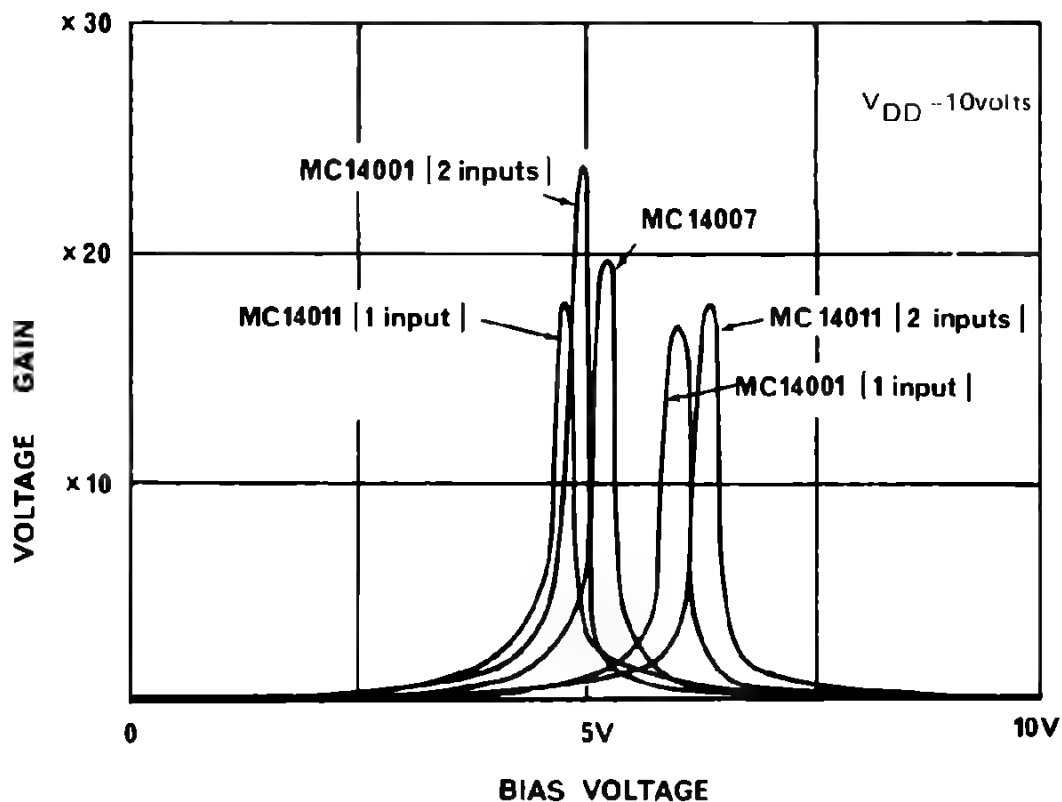


Fig. 11 GAIN CHARACTERISTICS OF DIFFERENT TYPES OF GATE

a particular gate is available for use as an amplifier, then one may have a choice of power supply voltage to be used (remaining within the limits discussed in 3). The curves shown below in Figure 12 give an indication of the variation of voltage gain characteristic brought about by changing the power supply voltages.

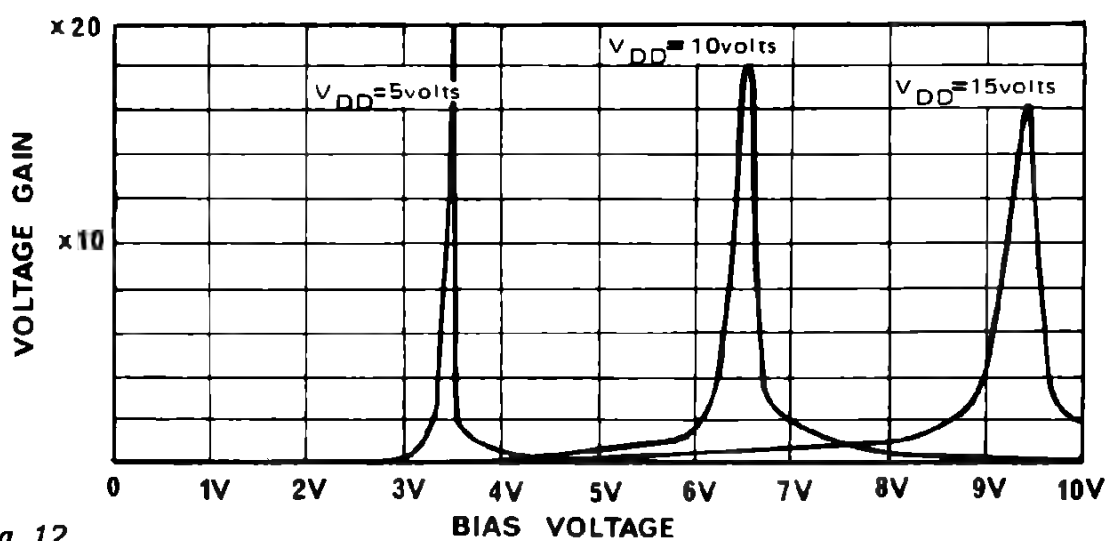


Fig. 12

GAIN CHARACTERISTIC OF MC14011 FOR DIFFERENT SUPPLY VOLTAGES

Sometimes it may not be possible to vary the supply voltage, so, often resistors are added between the CMOS inverter and the power supplies as in Figure 13, in order to reduce the current drain to acceptable limits.

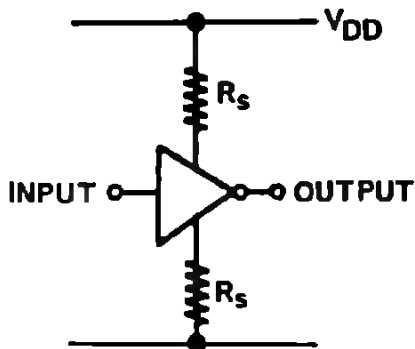


Fig. 13 LOW POWER CONSUMPTION INVERTER

The voltage gain of the circuit is effected drastically by this, and the curves in Figure 14 show the change of characteristics against the resistor value R_S .

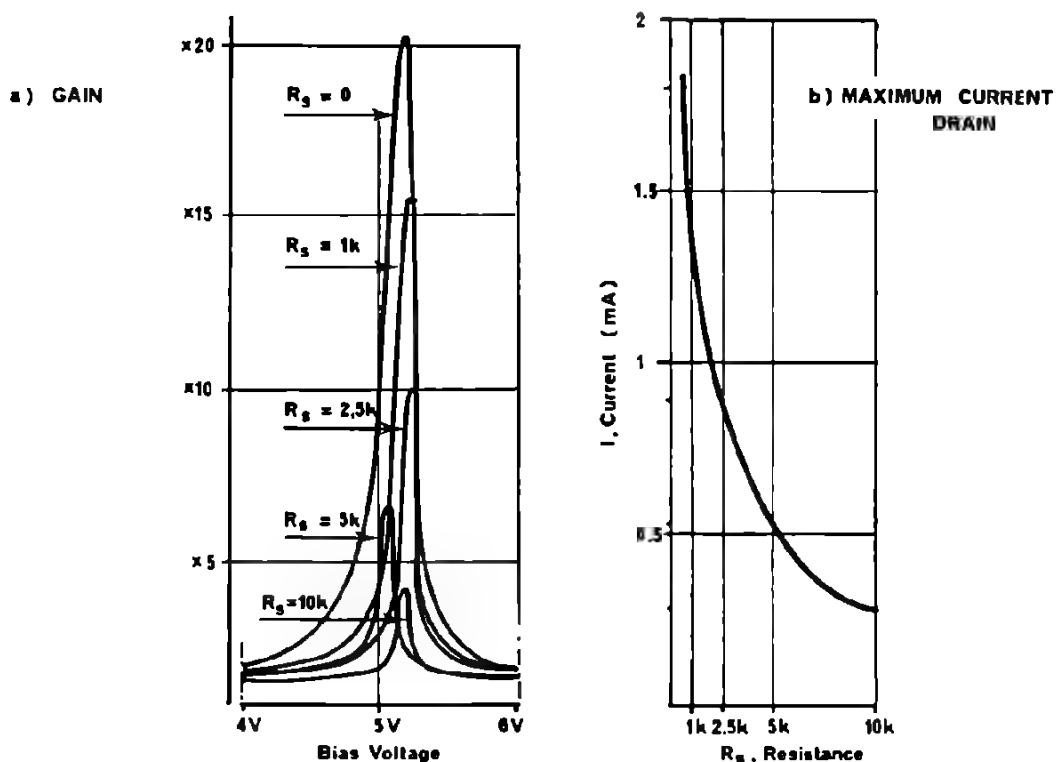


Fig. 14 MC14007 WITH DIFFERENT VALUES OF R_S AT $V_{DD}=10V$

There will of course be a variation of the gain as the temperature changes, in most cases due to the change of bias point with temperature (paragraph 2). Thus, each circuit must be analysed separately to determine the gain stability with temperature.

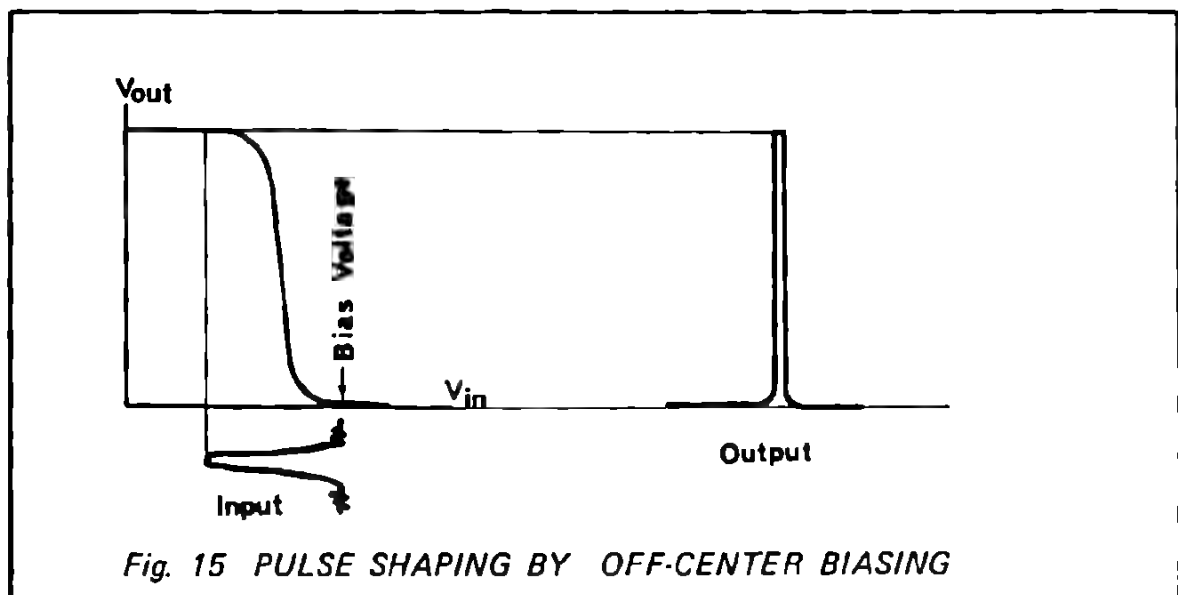
C PRACTICAL AMPLIFICATION CIRCUITS

Usually a CMOS-gate amplifier will be used where there is an interface between analog and digital circuits to be made involving pulse amplification/shaping.

1. D.C. AMPLIFICATION

In many systems a direct connection can be made between the analog voltage and the digital circuit, if the output level of the analog circuit can be adjusted to correspond to the desired voltage for biasing the inverter/amplifier. The advantage of this connection is that there is an extremely high input impedance of the CMOS device when no external bias resistors are added.

Often the non-linear characteristics of the CMOS inverters can be used to advantage, by deliberately biasing the inverter off-center. This provides a compression of low level signals (e.g. noise) while permitting amplification of the larger amplitude pulses without impediment. This is illustrated schematically in Figure 15.



2. A.C. AMPLIFICATION

Conventional linear a.c. amplification can be obtained, within the limits discussed earlier, by using a capacitively coupled input circuit.

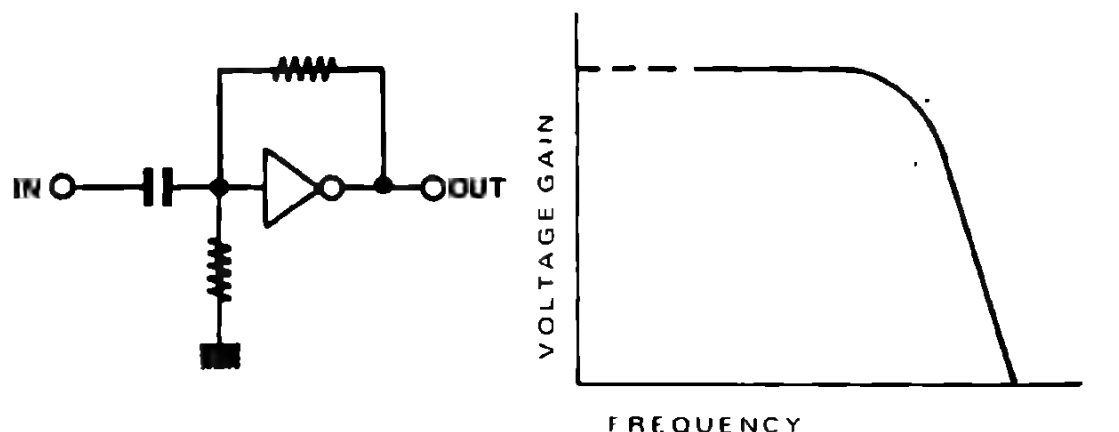


Fig. 16 CAPACITIVELY COUPLED A. C. AMPLIFIER

The lower cut-off frequency of this circuit will be given, as usual, by the value of the input capacitor/bias resistor combination. The upper cut-off frequency remains unchanged with the limits as discussed earlier in section B 5.

CASCADE CONNECTION OF CMOS INVERTERS

To obtain more gain, an obvious step is to cascade a number of CMOS inverters. However, the input transfer voltage of each inverter is defined within a very wide tolerance ($\pm 40\%$), so a direct cascading of two or more inverters is impractical, because the second amplifier could easily be biased completely off by the preceding stage.

Even if this were not the case, the output voltage drift of about $1 \text{ mV}/^\circ\text{C}$ for each inverter will be amplified by the second amplifier, rendering the characteristics too variable to ambient temperature change. A.C. coupling, as in Figure 17, should be used between individually biased stages in this case, to avoid such difficulties.

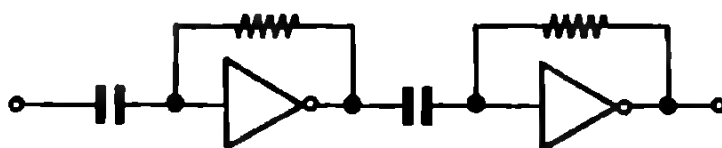
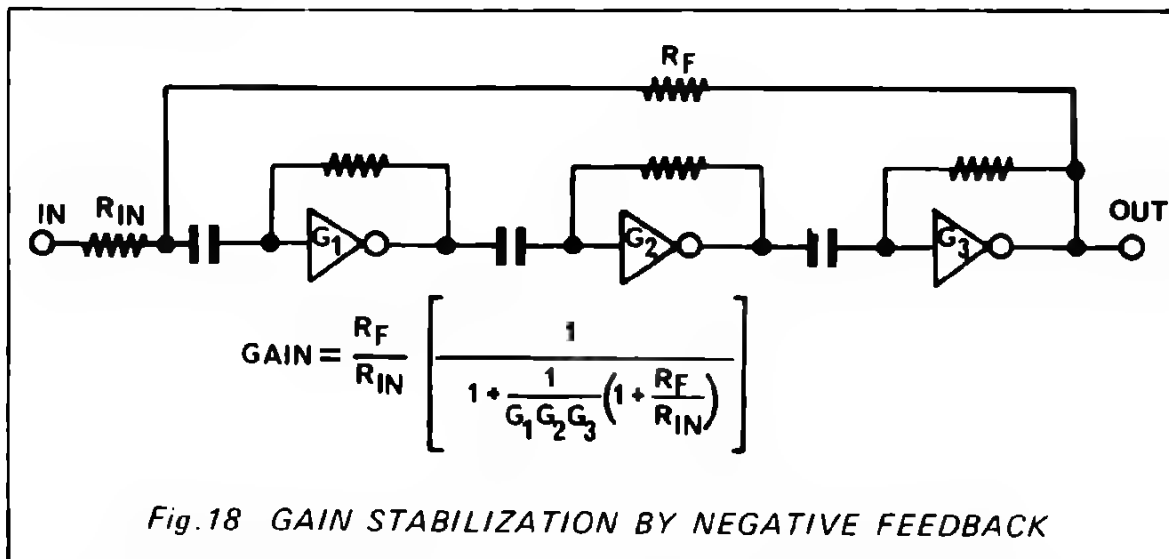


Fig. 17 TWO STAGE CAPACITIVELY COUPLED AMPLIFIER

Since each inverter provides a 180° phase change, gain stabilization and improvement in linearity requires an odd number of inverters to obtain the necessary negative feedback.



In the circuit illustrated in Figure 18, care is required in choosing the values of resistors and capacitors. This is to ensure that circuit does not oscillate owing to the effect of the three RC sections.

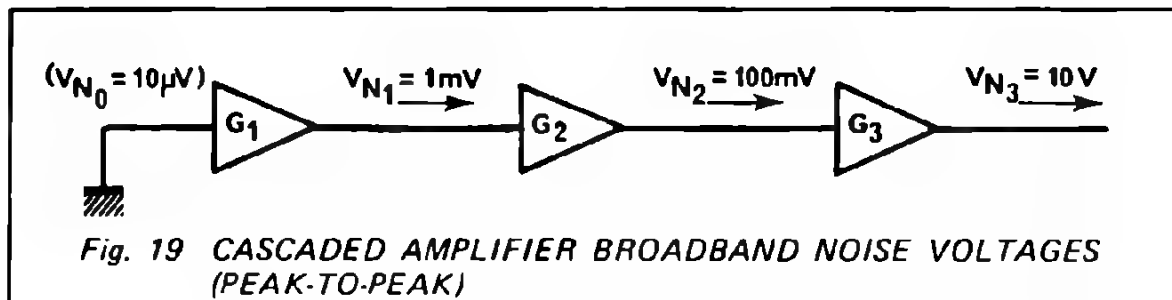
4. NOISE IN CMOS INVERTERS

The noise spectrum associated with a field effect transistor is considerably different from that of a bipolar transistor, owing to the difference in physical construction of the devices. A commonly used generalisation is that at low frequencies (below 1 kHz) a good bipolar transistor contributes less noise than a field effect transistor, but, the situation gradually reverses at higher frequencies.

The performance of a multiple stage amplifier will be limited by the noise output voltage from a single stage. Since capacitive coupling is inevitably used between stages of a CMOS amplifier, only the "broadband" noise (1 kHz–100 kHz) is considered here. In practice it is found that the amplitude of this noise varies from device to device, but it does, however, remain relatively constant against variations of supply voltage (and current drain).

The actual physical source of the noise in the CMOS inverter is normally due to surface noise in the channels themselves. Typical values of "broadband" noise voltage have been measured at around 400 μV r.m.s. output, for a typical CMOS-gate inverter with a gain of 100. This results in an equivalent input broadband noise voltage of about 4 μV r.m.s. which compares unfavorably against published figures for various other microcircuit amplifiers.

The significance of these figures comes when considering the effect of the noise as it is amplified in passing down the amplifier chain. If there are three similar amplifiers in the chain, then the gain per stage, G , must be less than 100 times (at $V_{DD} = 10$ volts) to prevent the final stage being saturated with noise.



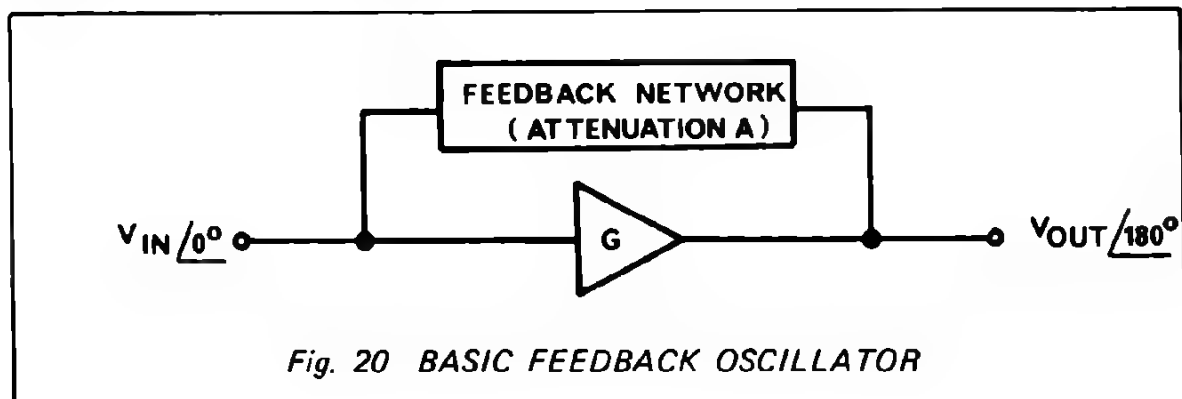
This shows that owing to noise, it may not even be possible to use three single stage inverters in cascade, without reducing the gain of the individual stages. Since the gain increases inversely with the supply voltage, the problem of noise saturation is more acute at low supply voltages.

D OSCILLATORS USING CMOS INVERTERS

Since the CMOS inverters, just described, have an extremely non-linear characteristic and relatively low gain, they are not suitable for use as sinusoidal oscillators. In general, oscillators built with logic elements are intended primarily as circuit clocks, where the actual wave shape is not too critical. Furthermore, it is often not necessary for the actual oscillation frequency to be precisely defined. In such cases, an astable multivibrator (paragraph D3) is the simplest and cheapest means of making the required clock. However, when there is a problem involving exact timing, a CMOS inverter amplifier with single resistor biasing and frequency selective feedback, provides an attractive solution.

1. FREQUENCY SELECTIVE FEEDBACK OSCILLATOR

Any CMOS amplifier (voltage gain G , phase shift 180°) can be converted (intentionally!) into an oscillator by adding a suitable feedback network (attenuation A) as in Figure 20.



The conditions for a self-starting oscillation of V_{OUT} , are that the amplifier gain (G) should be greater than the feedback network attenuation (A) where there is 360° phase change (or a multiple thereof) in the loop. This should be designed to occur at the desired oscillation frequency.

The feedback circuits usually encountered for sinusoidal oscillators (with linear amplifiers) can normally also be employed with CMOS-gate inverters. The amplitude of the oscillation is determined by the voltage swing of the CMOS amplifier (i.e. within 10 mV of the supply lines). The frequency stability will depend both on the stability of the phase shift in the feedback network, as well as on the phase characteristics of the inverters. A typical inverter phase characteristic has been measured against variation of supply voltage V_{DD} . The results are summarized in the graph of Figure 21.

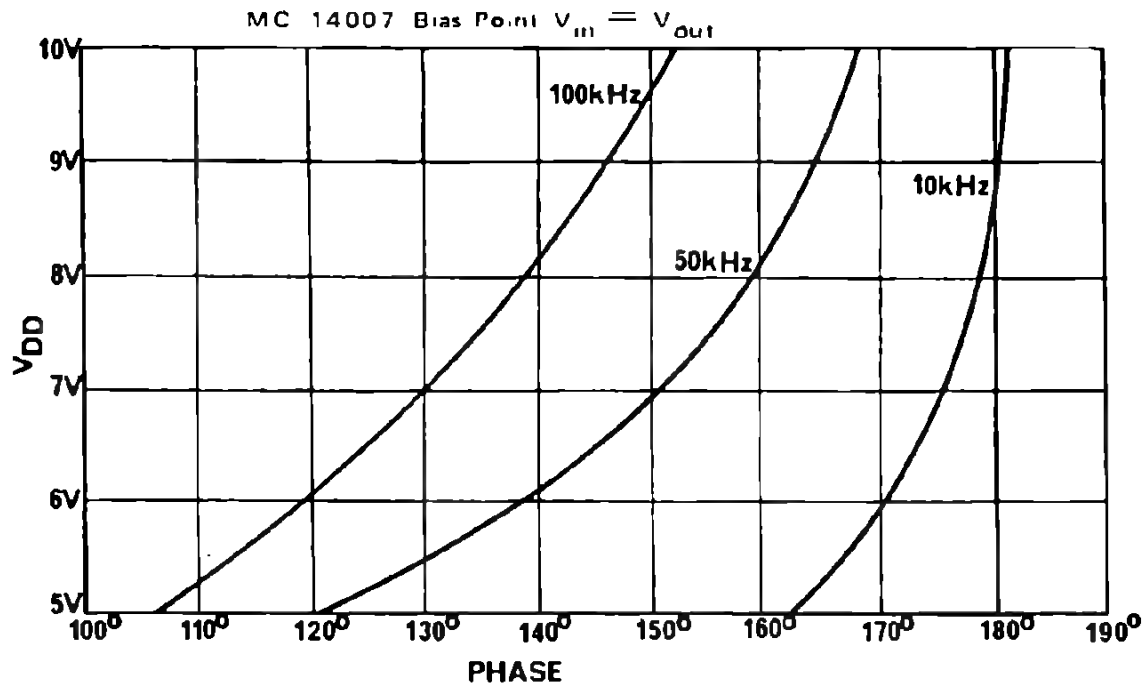


Fig. 21 PHASE CHARACTERISTIC OF CMOS INVERTER AGAINST V_{DD}

Since the CMOS-gate amplifiers, when biased centrally, may require considerable current from the supply, it is advantageous to use feedback networks with little attenuation, thereby forcing the inverter output to remain at one or other logic level as much as possible and so reduce the power demands of the oscillator. The feedback network for an oscillator featuring high stability, low power consumption, and well defined rising and falling edges, may be identified as one with low loss and a rapidly changing phase/frequency characteristic.

CRYSTAL OSCILLATOR

A well known and much used feedback network is that using a crystal, where the equivalent circuit is represented by the schematic in Figure 22.

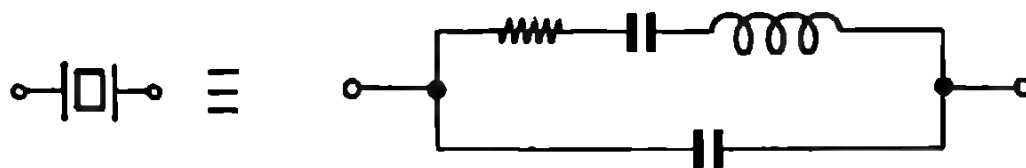
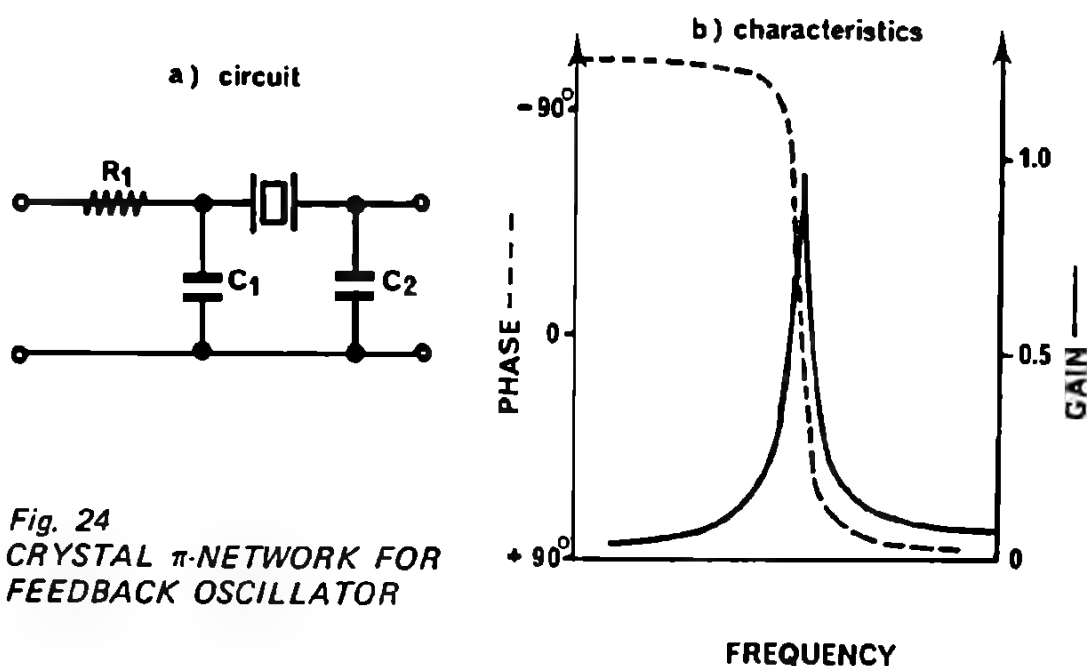
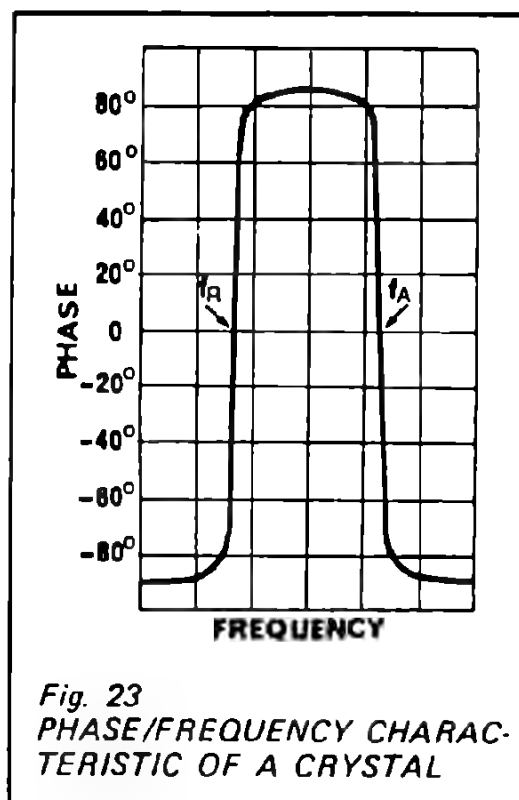


Fig. 22 CRYSTAL EQUIVALENT CIRCUIT

The phase/frequency characteristic as the form shown in Figure 23. The two near vertical portions of the curve represent the resonant (f_R) and anti-resonant (f_A) frequencies of the crystal.

A feedback network should be chosen in which the crystal is operated near series resonance and the attenuation is small. The circuit normally adopted is the crystal π -network as shown in Figure 24a. The form of the transfer characteristic of this crystal network is indicated alongside (Fig. 24b).

The optimum values of the components R_1 , C_1 , C_2 when used as the feedback elements around a CMOS inverter, depend on the crystal chosen.



A typical circuit is shown in Figure 25 in which the output frequency may be adjusted by the trimming capacitor.

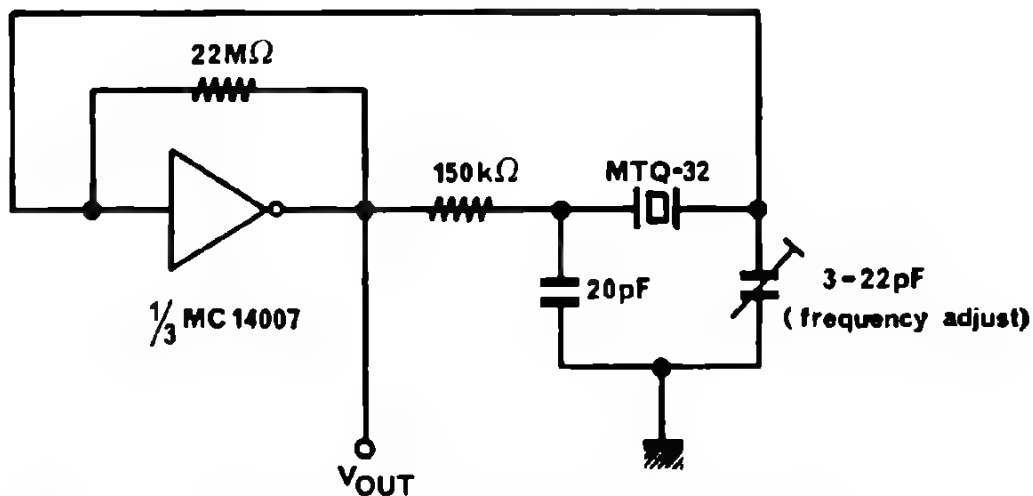


Fig. 25 A CMOS CRYSTAL OSCILLATOR FOR 32 KHz

A full discussion on stability of the crystal properties and other special crystal circuits, especially for use with low voltage supplies is to be found in the section concerned with Timepiece Electronics.

3. ASTABLE MULTIVIBRATORS

The frequency selective feedback oscillators described in the previous paragraphs are based on sustaining a 360° phase shift around a closed loop and can therefore be considered as "phase controlled" oscillators. Multivibrator circuits however are based on the charge/discharge time of RC circuits, so the astable multivibrator can be considered as a "time controlled" oscillator.

The basic resistor-capacitor circuits of interest are shown in figure 26. The principle of the multivibrator is the detection of a preset voltage across the capacitor, which will occur after a time defined by the values of the supply voltage, the resistor and the capacitor. When the required voltage is reached, the supply is abruptly changed and the cycle restarted. The multivibrator circuit can easily be realised in CMOS, the switching voltage being determined by the CMOS gate, and when its transfer voltage is exceeded, the change of voltage output occurs. The variation of time corresponding to the transfer voltage values within an inverter's guaranteed range (from the data-sheet) are also shown in the diagrams in Figure 26.

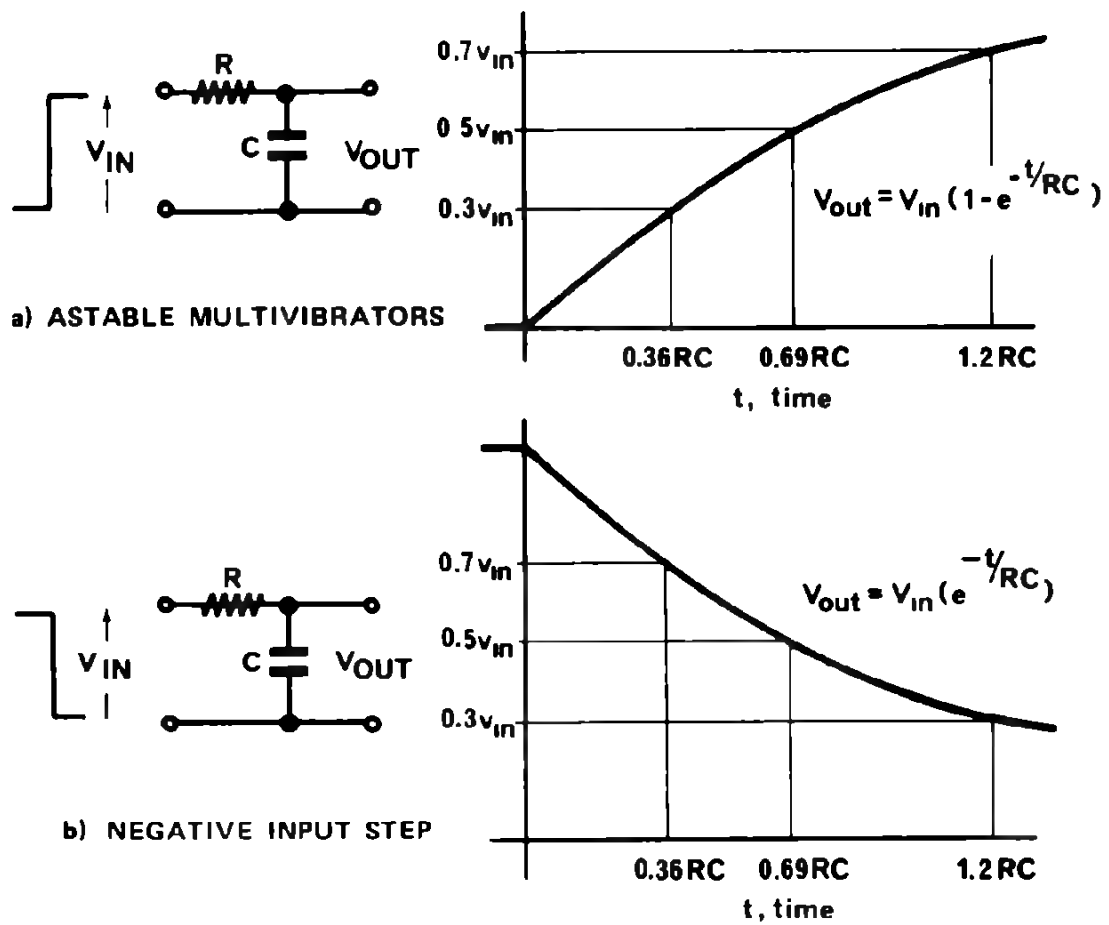
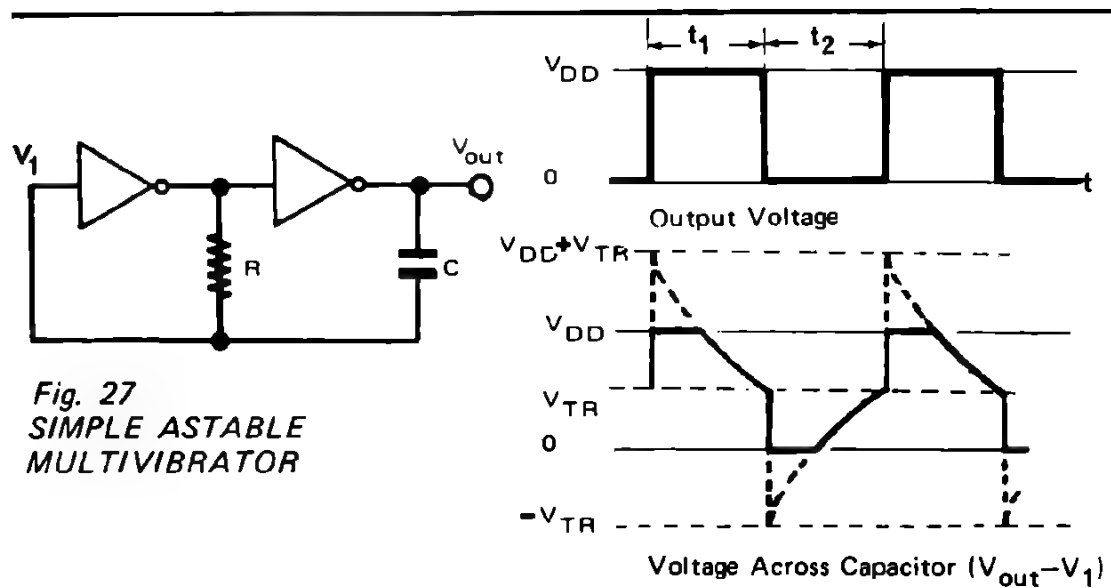


Fig. 26 STEP RESPONSE OF RC CIRCUIT



The output waveform can be specified in terms of frequency and duty cycle. These parameters are determined from the capacitor charging/discharging times t_1 and t_2 . Assuming that the transfer voltage is $\frac{V_{DD}}{2}$ ($\pm 40\%$), then, referring to Figure 26, the discharge time $t_1 = t_2 = 1.1 RC$ ($\pm 20\%$, -34%), giving a 50% duty cycle with a period defined as $2.2 RC$ ($\pm 20\%$, -34%). Appropriate waveforms are indicated in Figure 27.

In practice, however, the waveform will be considerably different, owing to the input circuit of the inverter, which includes safeguards in case voltages exceeding the power supply levels are applied to the input, as is the case here. Unfortunately the effects of the protection circuit on the frequency and duty cycle cannot be guaranteed owing to minor circuit differences from element to element. One means of minimising this problem is shown in Figure 28 where an extra resistor is added to the first inverter input, which will now permit V_1 to reach the voltages shown in figure 27, in practice.

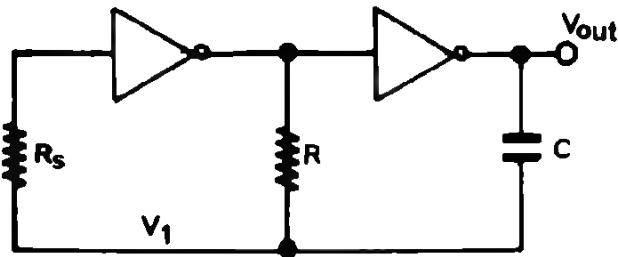


Fig. 28
ASTABLE MULTIVIBRATOR
INSENSITIVE TO INPUT
PROTECTION CIRCUIT

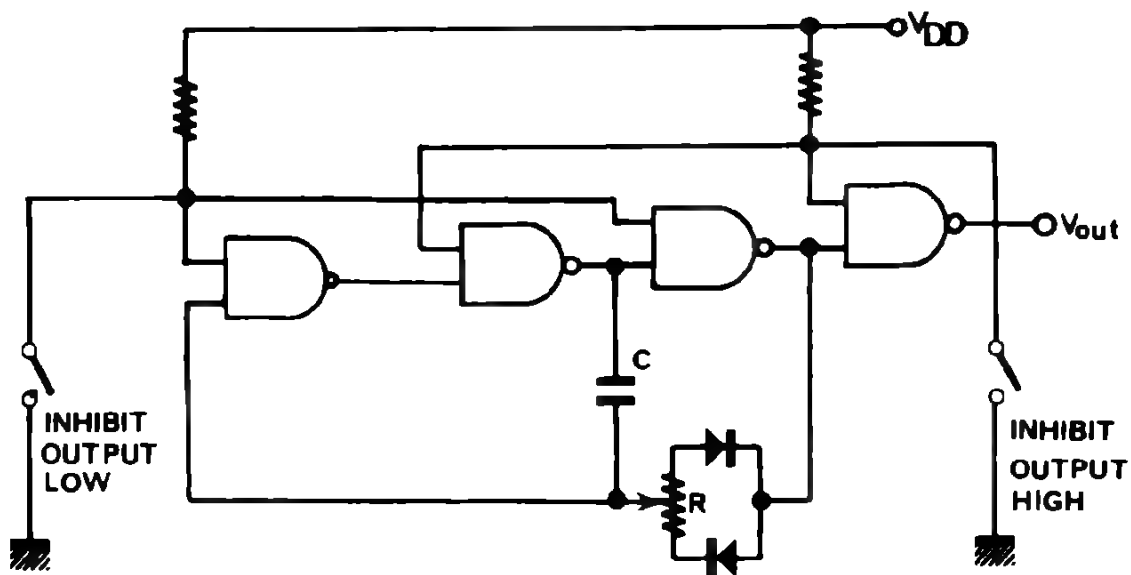


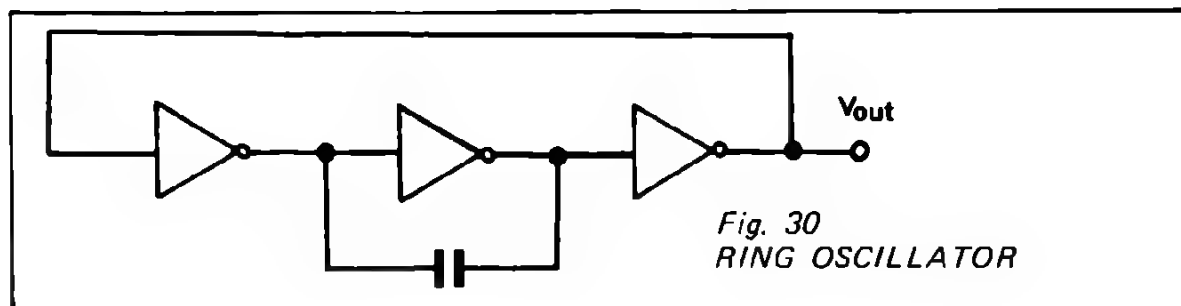
Fig. 29 ADJUSTABLE ASTABLE MULTIVIBRATOR

Typically R_S should be at least 10 times larger than R , so that microcircuit blocks may be exchanged without causing large variations in multivibrator frequency or duty cycle. Frequency corrections can easily be performed by varying R , but duty cycle variations require different capacitor charging times for the two portions of the square wave.

A useful circuit which permits frequency adjustment, duty cycle alteration and inhibition of the circuit with the output in either high or low logic state is shown in Figure 29, using MC 14011.

The frequency is adjusted by changing the value of the potentiometer resistance R , whilst the duty cycle adjustments require movement of the potentiometer slider. The upper frequency limit of this oscillator is determined by the propagation delays through the gates, whilst the lower limit essentially depends on the quality of the external R and C . In practice, by changing R and C the frequency has been made to vary between about 1 MHz and 1 μ Hz. Duty cycles up to a million to one have also been obtained with this circuit.

If such adjustments are not of interest for the application under consideration, another variation on the basic multivibrator circuit, shown in Figure 30, requiring only one capacitor is often useful (even though it does need 3 inverters).



For this circuit, the capacitor is charged or discharged through appropriate p- or n-channel transistors. The variation in frequency and duty cycle will depend on the resistance of these channels. An immediate implication is that for this circuit there will be a strong dependence on the temperature and supply voltage used (features not present in the other previously described circuits).

The effect of temperature on the frequency can be predicted, since the channel resistance has a known temperature coefficient (see paragraph B2). This results in variation of frequency of 0.3% per degree centigrade. The effect of variations of supply voltage can also be predicted from the p- and n-channel characteristics but necessitates quite an involved calculation. It is probably sufficient to accept that between 5 and 15 volts an increase of 10% to 20% in frequency occurs per volt increase of V_{DD} .

The curve shown in Figure 31 gives typical values of the capacitor needed for various oscillation frequencies with V_{DD} at 10 volts, for the MC 14011 (2 inputs active) inverter.

For the multivibrators described here, the inverters used may be any of those mentioned previously (paragraph B) but without the bias circuit connected.

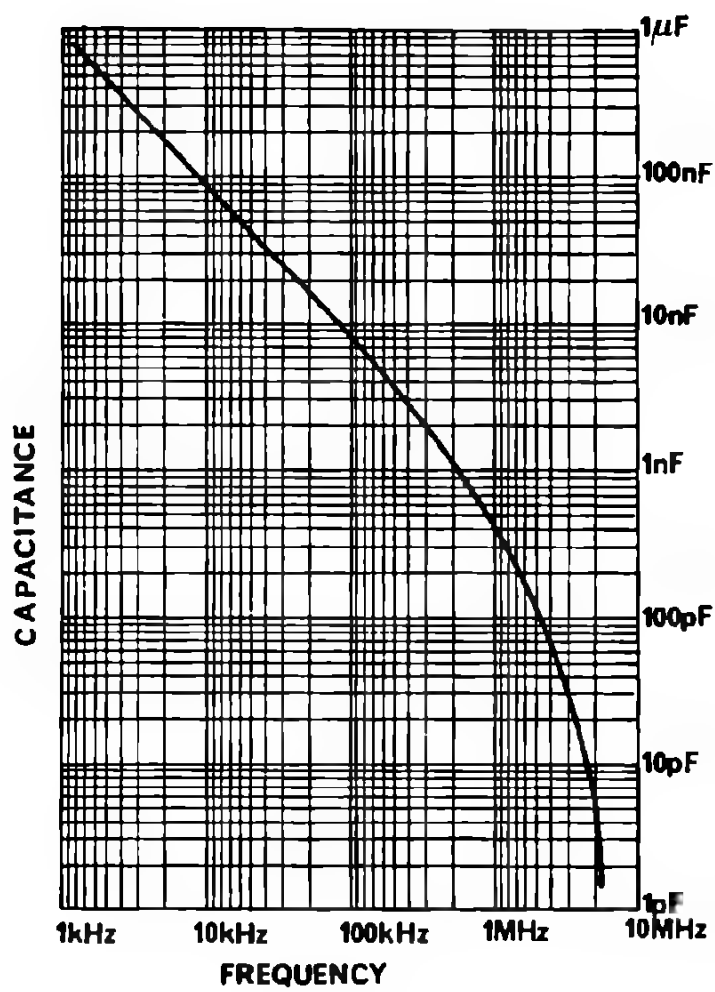


Fig. 31
**CAPACITOR VALUES
FOR THE RING
OSCILLATOR**

3 MONOSTABLE MULTIVIBRATORS

The monostable (or one-shot) multivibrator, like the astable, is based on the charge/discharge of an RC network. However, once triggered, the output is made to change and remain at the new logic level for a time determined by the component values of the RC network.

1. DISCRETE GATE MONOSTABLE MULTIVIBRATORS

A basic monostable in CMOS is shown below, Figure 32, using one NOR gate and one inverter.

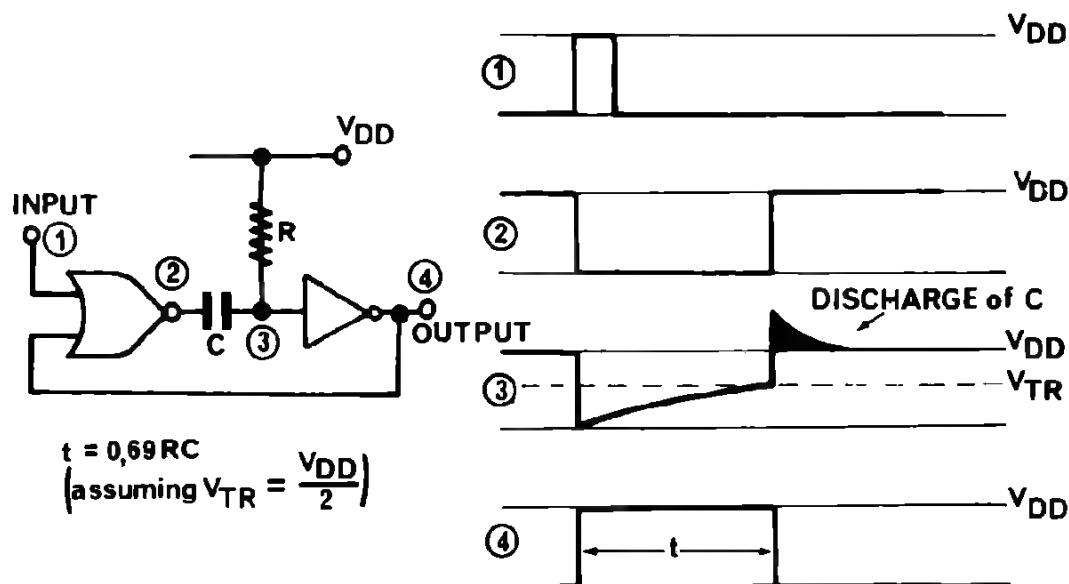


Fig. 32 MONOSTABLE MULTIVIBRATOR

In the initial steady state (input = 0), the capacitor is completely discharged. When the input goes positive the output changes and the capacitor is slowly charged. The output remains high until the voltage across the capacitor, in charging through the resistor, passes the threshold of the output inverter. If the threshold is exactly $V_{DD}/2$, the output will return to zero after $0.69 RC$, discharging the capacitor completely through R (and the inverter input protection circuit) and making the circuit ready for the next input trigger pulse.

As for the astable described in the previous section (D3), any variation in the transfer voltage of the inverter ($\frac{V_{DD}}{2} \pm 40\%$ according to the data-sheet) will give rise to a change in time delay ($0.69 RC - 47\%$, $+ 60\%$). A considerable improvement on this may be obtained by using the circuit shown in Figure 33 using two similar inverters.

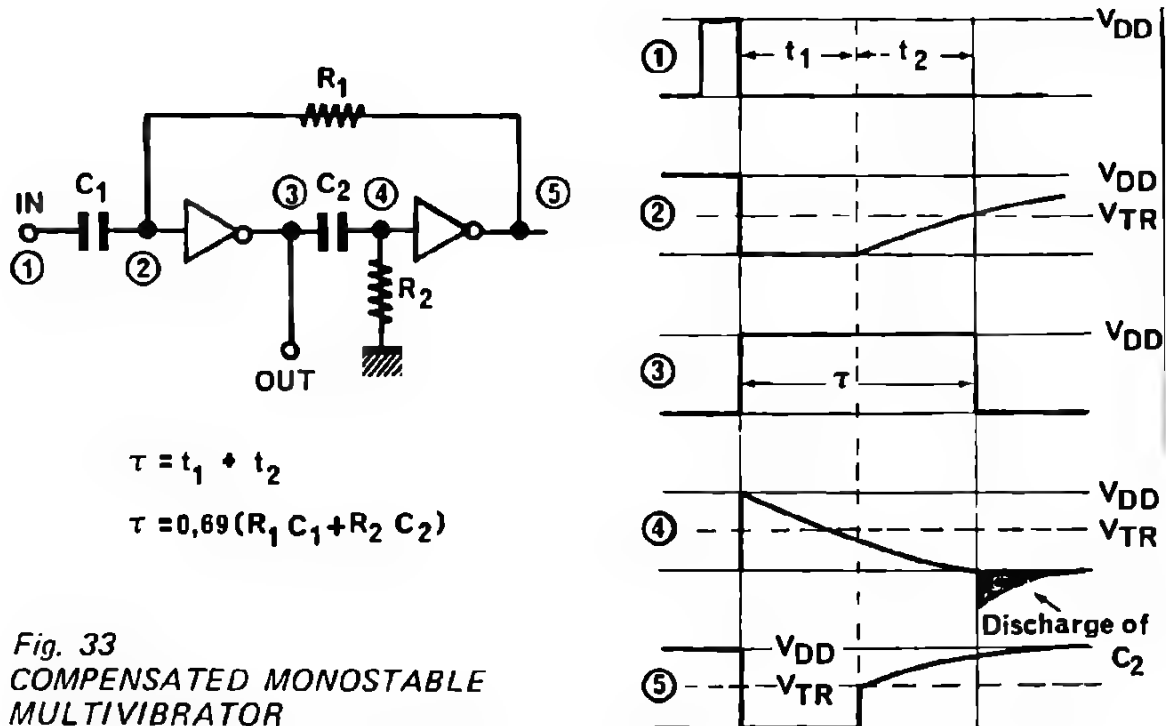


Fig. 33
COMPENSATED MONOSTABLE
MULTIVIBRATOR

If $R_1 C_1 = R_2 C_2$, then the output pulse $\tau = 1.4 RC$ and the precision will depend now on the difference in threshold voltage between the two inverters. A series of tests on a small number of MC 14011 quad 2-input NAND gates (from different production batches) showed that, whilst between all the gates the transfer points measured varied by $\pm 20\%$ (well within the $\pm 40\%$ specification), between gates on the same chip the variation was only $\pm 2\%$. These represent typical manufacturing tolerances, so, using gates on the same chip, the circuit in Figure 33 should have an output pulse width precision of about $\pm 3\%$.

2. MONOSTABLE MULTIVIBRATOR MC 14528

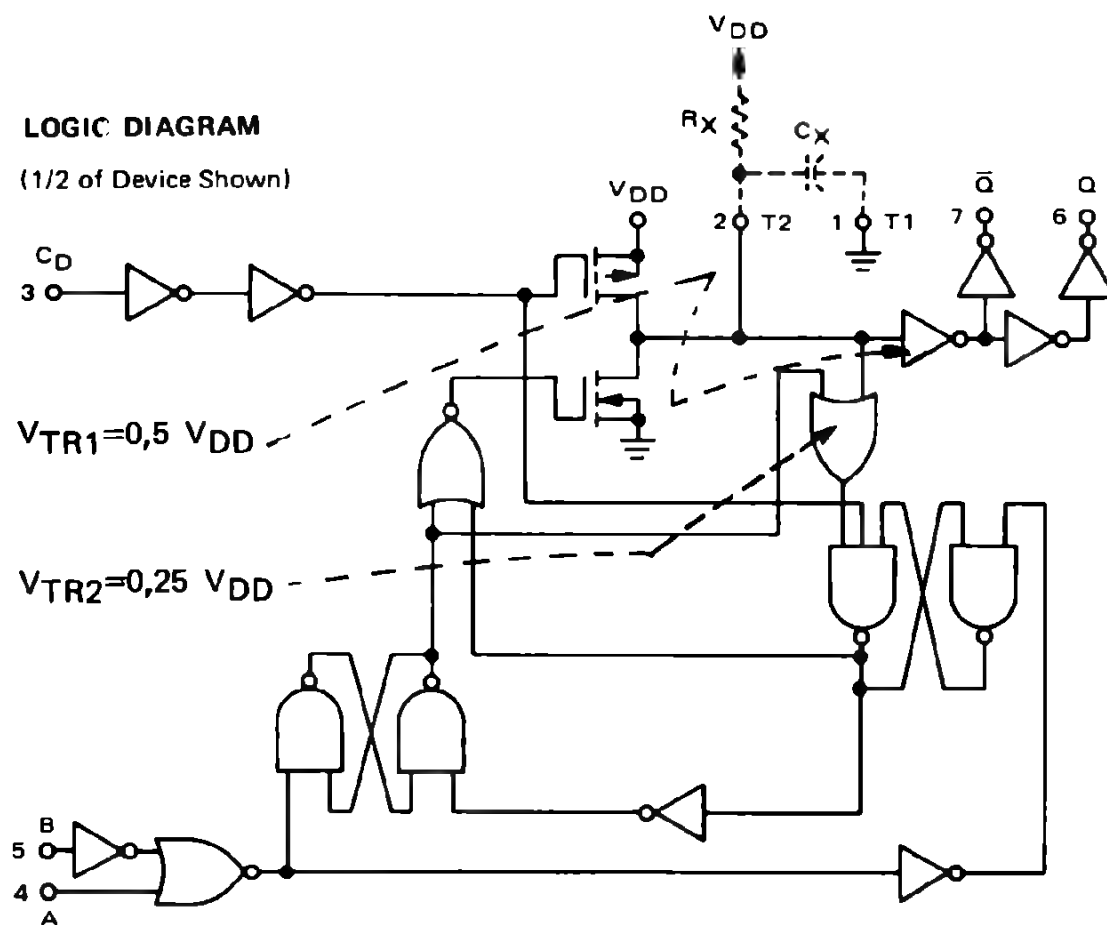
In practical circuits, it is very often required to reset or retrigger the monostable during its operating cycle. Additional gates are required for this purpose, so the CMOS integrated circuit MC 14528 has been designed to provide these functions for a dual monostable, all in the same package.

In the quiescent state ($A = 0$, $B = 1$, $C_D = 1$) point T_2 is floating and the capacitor C_X has been fully charged via R_X . $Q = 0$ and $\bar{Q} = 1$ in this state. When $A \rightarrow 1$ or $B \rightarrow 0$ (C_D still 1) point T_2 becomes 0, the capacitor is discharged rapidly through the n-channel MOSFET and when the voltage across the capacitor is equal to the transfer voltage ($TR1 = 0.5 V_{DD}$) of the inverter, $Q \rightarrow 1$ and $\bar{Q} \rightarrow 0$. The time required before Q and \bar{Q} change depends on the capacitance C_X , as well as the value of the n-channel resistance.

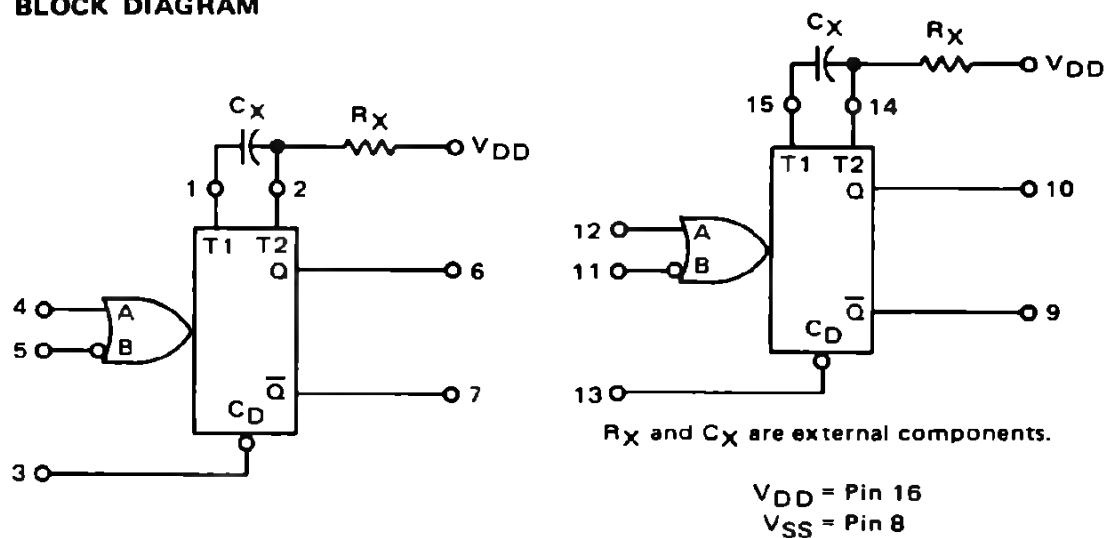
Fig. 34 DUAL MONOSTABLE MULTIVIBRATOR MC14528

LOGIC DIAGRAM

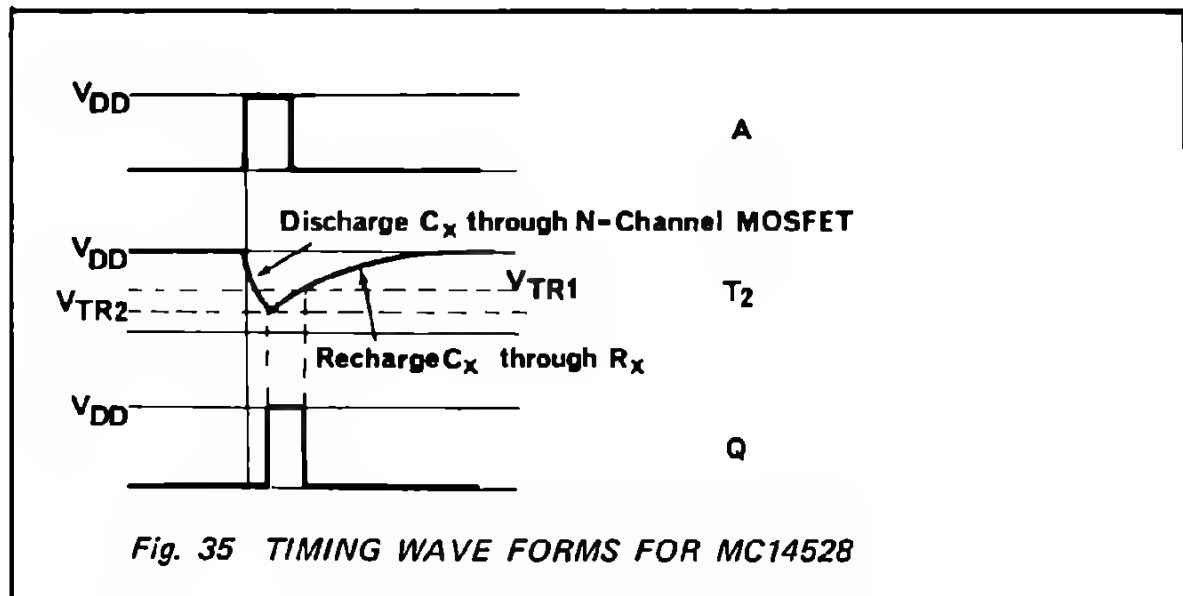
(1/2 of Device Shown)



BLOCK DIAGRAM



The discharge cycle is stopped when the capacitor voltage reaches another lower value ($TR2 = 0.25 V_{DD}$), causing the n-channel transistor to switch off abruptly. The capacitor is now recharged slowly through R_X until the transfer point ($TR1$) of the inverter is again passed, causing Q and \bar{Q} to revert to their original status. The appropriate waveforms are shown below in Figure 35.



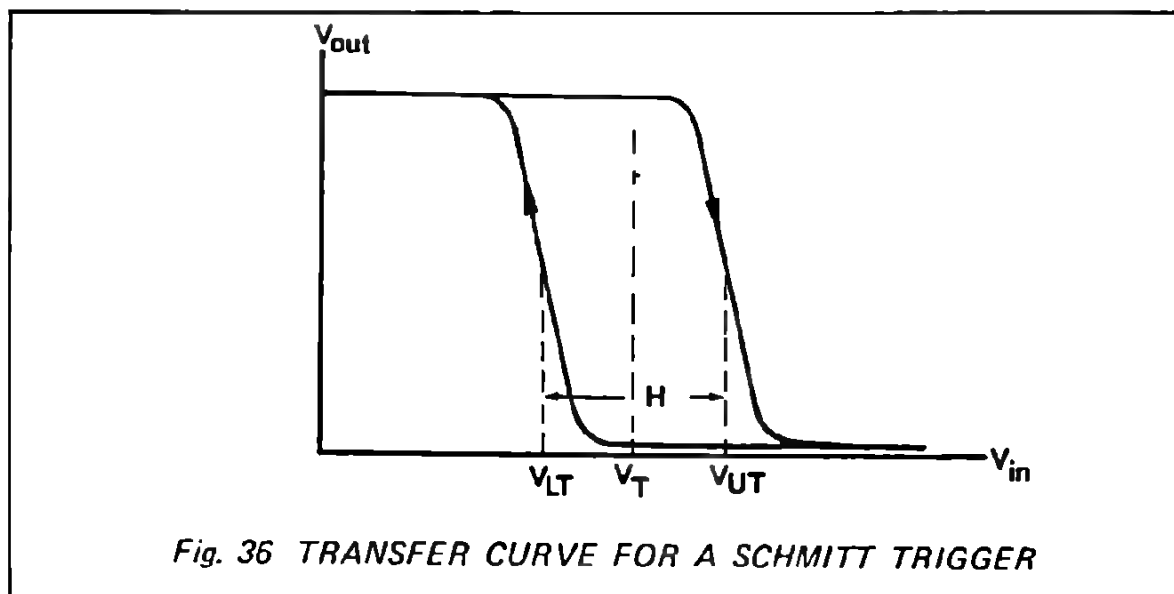
With this circuit, the monostable may be retriggered at any time after the initial change of Q , and the recharge time is again counted from the time when V_{TR2} is reached, following this latter trigger pulse. The input C_D is used to return the monostable to its initial state (C_X fully charged). When $C_D \rightarrow 0$, the capacitor is charged directly through the p-channel MOSFET, resetting the device rapidly. Curves and formulae are noted on the data-sheet to calculate the time delays obtained for different combinations of R_X and C_X .

Assuming R_X and C_X are known exactly, the precision with which the time delays can be estimated depends on manufacturing variations of the inverter, the OR gate and the internal propagation delays. Tests showed that there is a variation in timing precision ranging from $\pm 5\%$ for short delays (order of microseconds) and high supply voltages, to $\pm 20\%$ for long delays (order of minutes) and low supply voltages, for different microcircuit blocks. Variation against temperature is about 0.05% per $^{\circ}\text{C}$, which is probably due to the difference in temperature coefficient of the n-channel and p-channel transistors.

These figures of timing precision should all be viewed in the perspective of the circuit design and component selection. Although accurate resistors can easily be obtained for R_X (say $\pm 1\%$), accurate stable capacitors are not so easily obtained. Realistically C_X can not probably be defined better than $\pm 2\%$, showing that, in fact, almost any accurate monostable will have to have provision for adjustment to R_X , to obtain the exact output pulse width desired.

F SCHMITT TRIGGERS

These circuits are another commonly found interface between the analog and digital domains. Primarily their function is to convert a slowly changing analog voltage (sometimes noisy) into an abrupt digital logic change at required threshold levels. To eliminate noise and spurious oscillations elsewhere, the circuit is designed to have hysteresis between the upper threshold and lower threshold values, as shown in Figure 36.

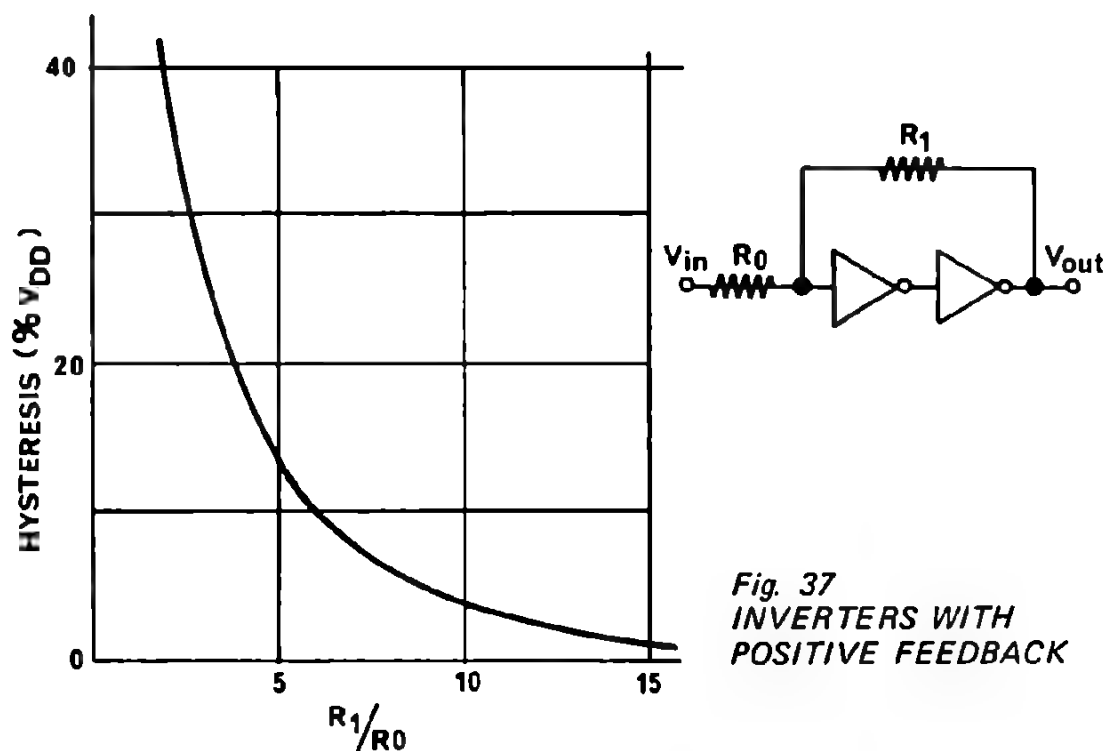


The thresholds are normally defined by the two switching voltages V_{UT} and V_{LT} , but in some cases are defined by a single switching voltage V_T and hysteresis H .

Conventional Schmitt triggers are analog amplifiers with positive feedback. However, CMOS technology allows other forms of circuits to be built which are unique to this microcircuit family.

1. CMOS AMPLIFIER WITH POSITIVE FEEDBACK

To obtain positive feedback, two CMOS inverters may be connected in cascade and feedback applied around. The degree of hysteresis is dependent on the ratio of the resistors R_1/R_0 as shown in Figure 37.



a switching voltage, V_T , for this circuit (with zero hysteresis) is defined by the voltage transfer characteristics of the first inverter. The value of V_T can be used by adding a suitable valued resistor R_2 as indicated in Figure 38.

Connections from the input to either the positive supply line (for $V_T > \frac{V_{DD}}{2}$) or ground (for $V_T < \frac{V_{DD}}{2}$) allows the transfer characteristics to be suitably fitted.

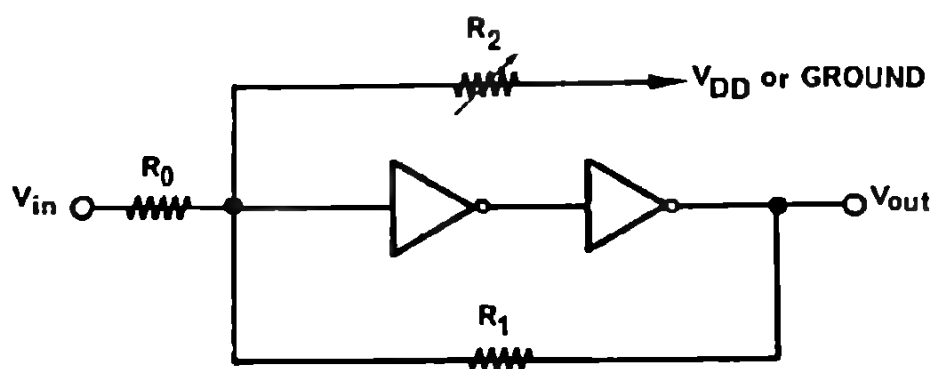


Fig. 38 A SCHMITT TRIGGER WITH ADJUSTABLE TRIGGER LEVELS

ly ing different voltages to the gate inputs of a modified gated R-S flip-flop cause the flip-flop to change states at two different voltages. For trigger s above $\frac{V_{DD}}{2}$, NAND gates may be used in the connection shown in fig.40.

lower value, V_{LT} , is always given by the threshold voltage of the gate 3, st the upper, V_{UT} , is given by gate 1 and may be varied by changing V_X . trigger levels below $\frac{V_{DD}}{2}$, NOR gates may be used. (Fig. 41)

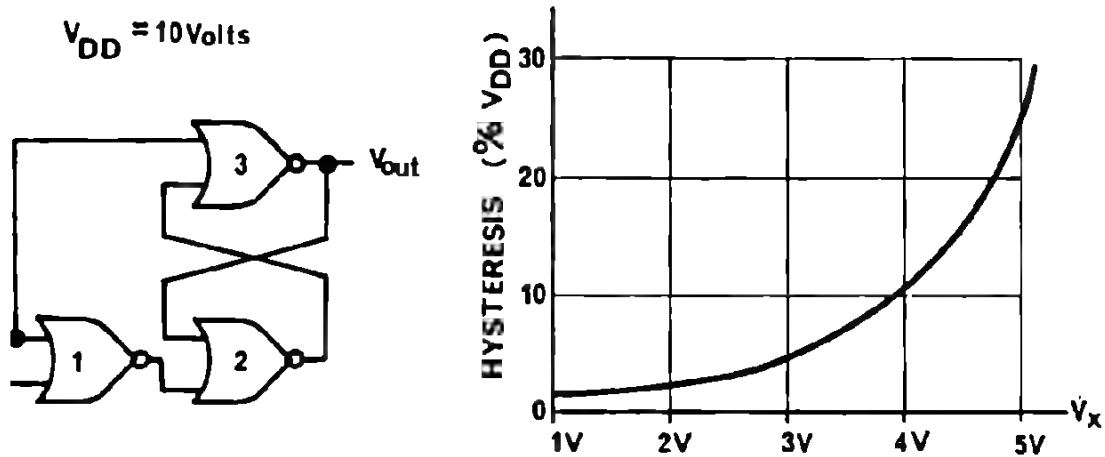


Fig. 41 SCHMITT TRIGGER MADE FROM NOR GATES

the upper value, V_{UT} , is always given by the threshold voltage of gate 3, st the lower value, V_{LT} , is given by gate 1 and may be varied by V_X . g one or other of these combinations, most applications requiring adjus- Schmitt triggers may be satisfied.

DUAL SCHMITT TRIGGER MC 14583

other basic configuration often encountered is a single inverter with a number different inputs interconnected as shown in Figure 42.

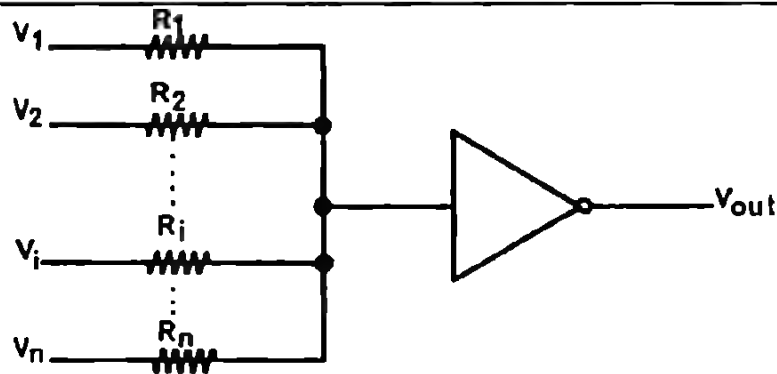


Fig. 42 MULTIPLE-INPUT INVERTER CIRCUIT

2. 2-INPUT GATES AS SCHMITT TRIGGERS

Since the Schmitt triggers discussed here involve use of logic gates with voltages at their inputs which are not at the logic levels 0 or 1, an investigation into the behaviour of the gates under such conditions is warranted.

Figure 39 shows the variations in transfer curve of a NAND gate (1/4 MC 14011) with one input (V_A) held at a voltage between the logic levels.

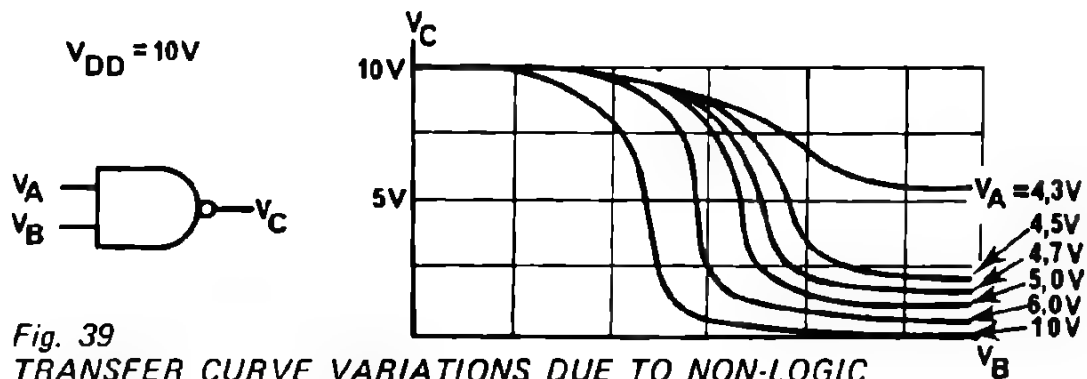


Fig. 39

TRANSFER CURVE VARIATIONS DUE TO NON-LOGIC LEVEL INPUT VOLTAGES

It is noticeable that although these curves do differ considerably from device to device (as would be expected), there is little detectable variation of the curves with temperature changes (see discussion paragraph B2). Otherwise stated, it is probable that Schmitt triggers employing these characteristics will be relatively stable against temperature change, although needing individual adjustment if the microcircuit block is exchanged.

The above characteristics permit a number of different Schmitt triggers to be implemented based on the simple R-S flip-flop.

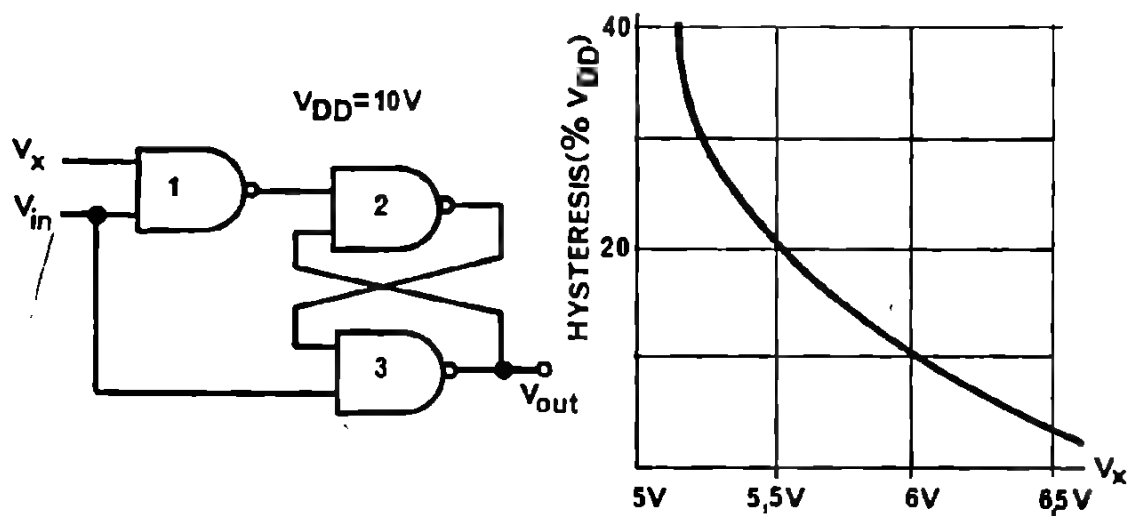


Fig. 40 SCHMITT TRIGGER MADE FROM NAND GATES

If the inputs are characterized by the voltages V_i and resistors R_i , since the input impedance of the CMOS inverter is extremely high, the voltage at the inverter input can be determined.

Supposing that one of the inputs is the varying signal, then adjustment of the resistor values and/or input voltages will permit considerable variation of the effective transfer characteristics.

If the inverter is connected with two inputs and one of the inputs V_X is varied by means of a circuit controlled also by the input voltage (as represented by the dotted line in Figure 43), then the connection can be made effectively to give positive feedback and the circuit acts as a Schmitt trigger.

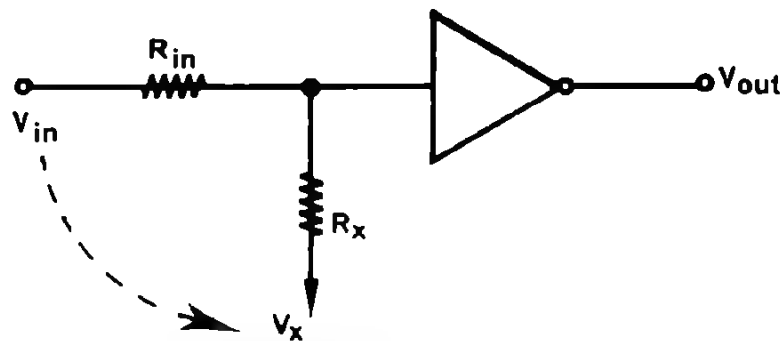


Fig. 43 VARYING THE TRANSFER CHARACTERISTICS OF AN INVERTER

Figure 44 shows a Schmitt trigger where the resistors are made to control the transfer voltages of the second inverter. The characteristics of this circuit are dependent also on the values of the resistance of the different p- and n-channel transistors making up the inverters.

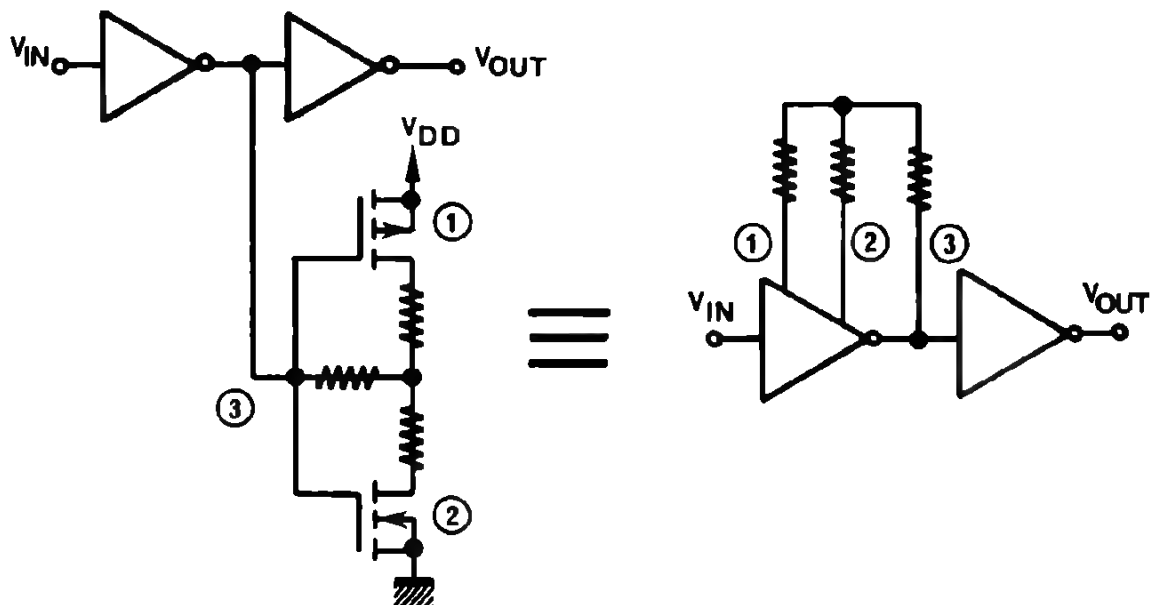


Fig. 44 SCHMITT TRIGGER CIRCUIT USED IN MC14583

This circuit is the basis of the Schmitt trigger circuit in the MC 14583. The actual values of the resistors required for various switching thresholds are quoted in the data-sheet for the device.
The MC 14583 contains certain other interconnecting logic elements as shown in Figure 45.

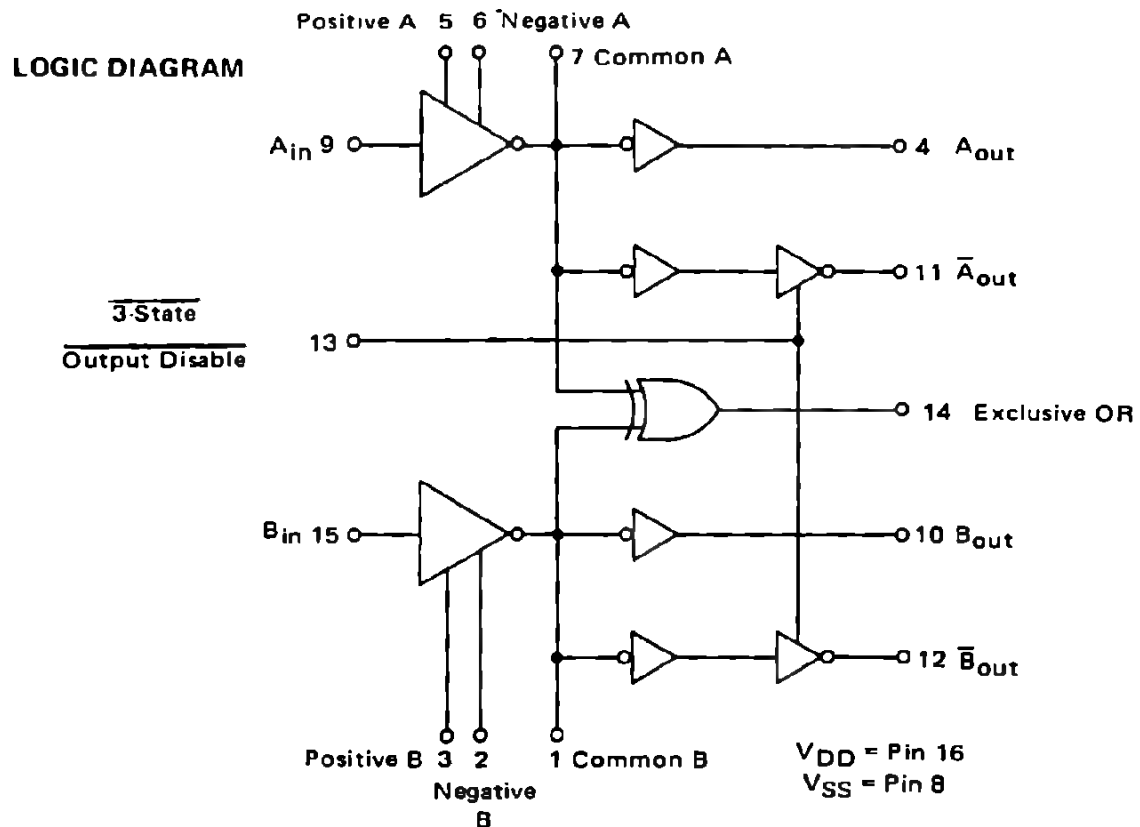


Fig. 45 LOGIC DIAGRAM OF MC 14583

One of the uses for this particular combination is in the application of these devices as pulse recovery receivers at the end of transmission lines. By using both Schmitt triggers and taking the output from the exclusive OR, the effects of common mode noise on the transmission lines can be minimized. Another interesting feature of this device is the tri-state output of each Schmitt trigger in addition to the standard outputs.

1. MULTI-INPUT GATES

The variation that occurs in the transfer characteristics of multi-input gates according to the input connections, has been fully discussed in earlier sections. These properties can be exploited to obtain a Schmitt trigger circuit as shown in Figure 46 for a 3-input NAND gate (MC 14023).

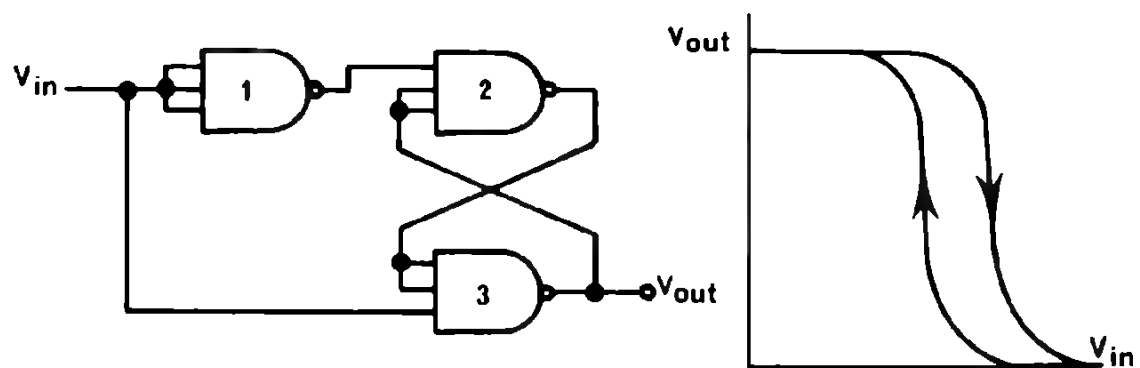


Fig. 46 MULTI-INPUT GATE SCHMITT TRIGGER

The upper trigger level, V_{UT} , is given by the threshold voltage of gate 1, the lower, V_{LT} , by gate 3. Typically the hysteresis of this circuit is around 30% V_{DD} , however, the value of V_{UT} , obtained in replacing the gate 1 connection by the alternative 1 (a) shown below in Figure 47, gives a reduced hysteresis of about 15% V_{DD} .

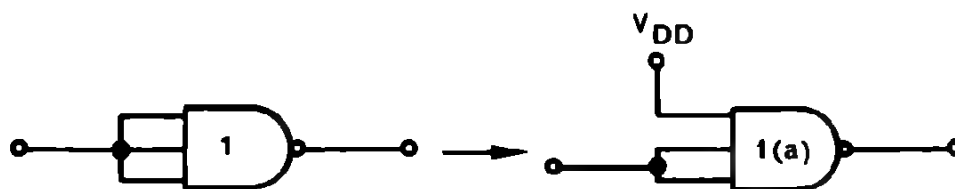


Fig. 47 ALTERNATIVE GATE CONNECTION FOR DIFFERENT SYSTEMS

In practice these circuits are useful, since large hysteresis is obtained without requiring individual adjustment of each circuit.

G ANALOG SWITCHING

Discrete MOSFETs have been in use for switching analog signals bi-laterally for a long time, so it seems natural to adapt the CMOS logic gates for this application also.

The basic element used is the transmission gate, which has been described earlier in detail, however, the main features will be recalled here.

The transmission gate (Fig. 48) consists basically of a parallel combination of p- and n-channel MOSFETs and is controlled by the gate electrodes.

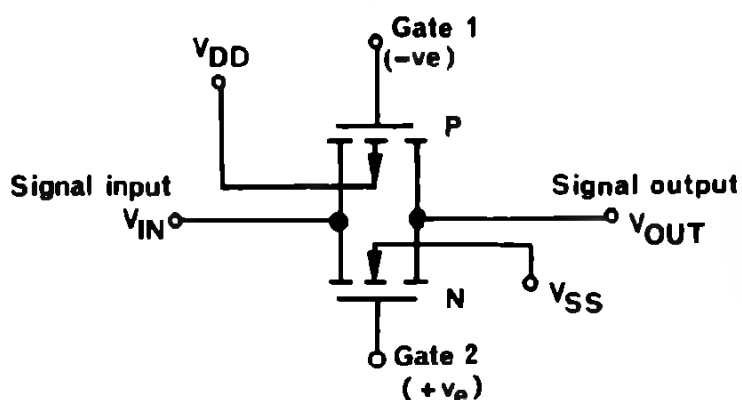


Fig. 48
SIMPLE
TRANSMISSION GATE

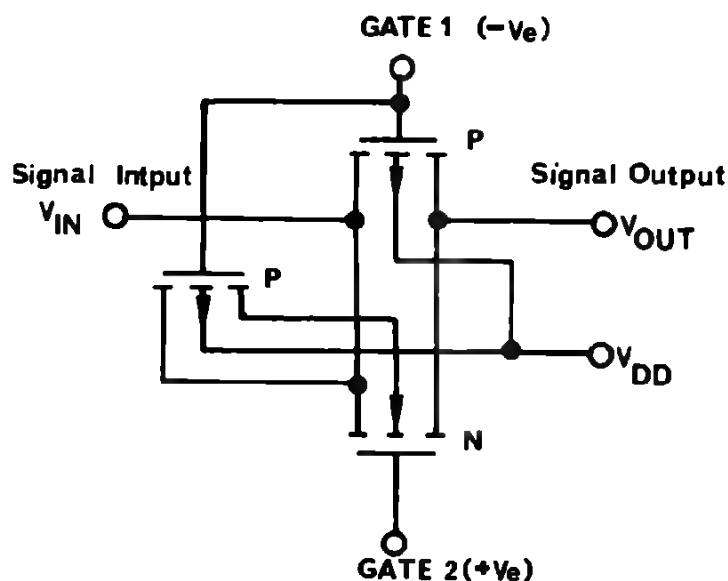


Fig. 49 COMPENSATED TRANSMISSION GATE

The transmission resistance will vary with the signal voltage (V_{IN}), the potential difference between the p- and n-substrates ($V_{DD}-V_{SS}$) and the output load. In analog switching it is desirable that the transmission resistance does not change with the input voltage level, so as to retain a constant ON/OFF ratio regardless of the input signal. By controlling the substrate potentials, it is possible to compensate for variations, balancing the effect of changing voltage input amplitude against substrate voltages. This is achieved by the circuit shown before in Figure 49, and is characterized by an almost constant ON resistance (about 350 ohms) practically independent of applied voltages. Introduction of the transmission gate into circuit design has led to the use of a new logic element symbol. (Fig. 50).

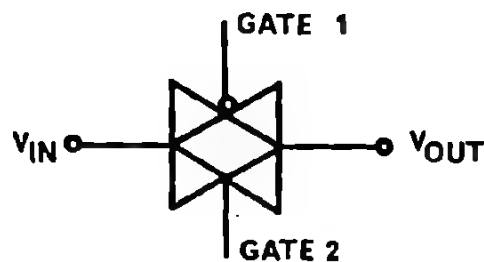


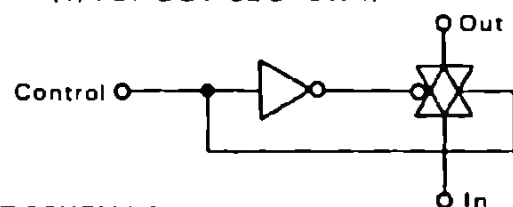
Fig. 50
LOGIC SYMBOL FOR A
TRANSMISSION GATE

For the MOTOROLA MC 14xxx series, in the circuits intended for analog switching applications, the transmission gates used are all those as shown in Figure 49. Typical of these devices is the MC 14016 quad analog switch, of which the circuit for one switch is illustrated in Figure 51 below.

Logic Diagram Restrictions
 $V_{SS} \leq V_{in} \leq V_{DD}$
 $V_{SS} \leq V_{out} \leq V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)

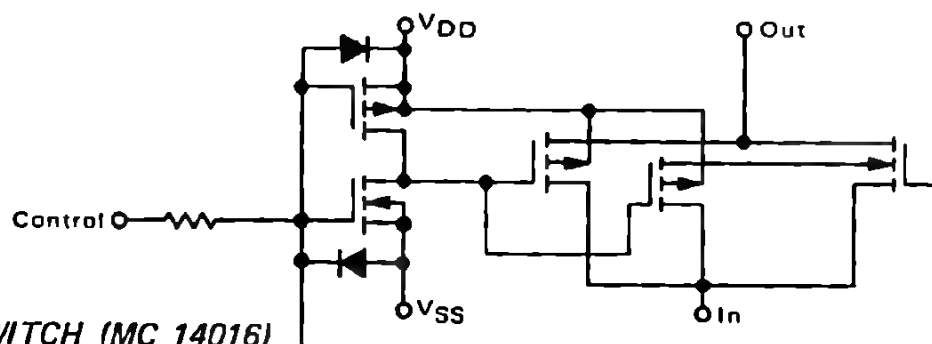


Fig. 51
ANALOG SWITCH (MC 14016)

It is essential that neither the analog voltages V_{IN} nor V_{OUT} lie outside the power supply voltages. If this restriction is not respected (even for short transients) the device is liable to enter a "latch-up" condition, which can only be removed by disconnecting both the power supplies and the offending analog voltage. Full details of the characteristics of the devices are to be found in the data-sheets for the circuits concerned.

Care is required in constructing transmission gates from CMOS "building blocks" such as the MC 14007, since the devices are characterized only as inverter pairs. There is therefore, no guarantee that the p-channel transistor of one "pair" combined with the n-channel of another, will result in a transmission gate working over the guaranteed range associated with the MC 14xxx family.

CHAPTER 9

Computer Applications

CMOS IN COMPUTER APPLICATIONS

In any application where low power, high complexity, high noise immunity and dense packaging are considered important, CMOS offers significant advantages compared to other logic families. Computer applications are not excluded simply because of the low speed of CMOS circuits. There are extensive applications in peripheral equipment where high speed may often be a disadvantage. The inherent noise immunity of slow circuits make them ideal to work in adverse environments where switching of solenoids, driving of stepping motors or servos may cause problems for any other logic. The phase locked loop speed regulation of a tape drive is one of the more obvious uses of CMOS.

Already now, the CMOS family is going to reach the critical mass, the range of MSI will soon make possible to realize more complex logic with less packages than with TTL. It would thus be possible to totally realize the computer main frames with CMOS circuits and, surely, there will be some critical applications where the existing TTL designs will be, for some reason, transformed into CMOS.

It is, however, far more reasonable to combine CMOS with large scale MOS integrated circuits, particularly with N-Channel MOS, where the compatibility is excellent.

There already exist one chip parallel microprocessors on the market. The average speed lies in the range of about $20\mu\text{s}$ per instruction and there is no problem to use CMOS logic around such a processor.

The typical applications are visual display intelligent terminals, point of sales terminals, parking house logic, elevator logic, price calculating balances to mention a few of them only.

The advantage of systems based on microprocessors is that they are easy to adapt to a particular application because the hardware can be tailored to any size needed. The ease of future expansion and the flexibility makes them even more attractive. It takes only a few minutes or even seconds to change a program without altering the existing hardware.

1

Often the programs are stored in read only memories. This is for price reasons and also because the ROM's are non-volatile. They do not lose information when switching power off.

The typical configurations start with 64x8 bits of READ-WRITE store with 1024 to 2048 words of ROM up to sophisticated systems which use up to 8k or even 16k 8 bit words.

The processors are slow and have a restricted set of instructions usually performing binary arithmetic only.

In order to demonstrate the power of CMOS MSI circuits when used to improve performance of microcomputers, a typical example of a hardwired circuit for decimal arithmetic will be shown. It is estimated that this relatively simple circuit may increase the calculating speed for at least a factor of 5.

The idea is to calculate in Binary Coded Centimal (BCC) system, while always handling two BCD digits at a time.

Let us consider BCC addition. Since the processor can only perform 8 bit parallel binary arithmetic, a conversion has to be made when the sum of two BCC digits exceeds 99. Then 156 has to be added to the existing result and a centimal carry should be shifted into the next higher significant position.

Example (least significant bit is the rightmost one):

Number	Correction	BCC Carry	Binary Equivalent
78			01001110
+ 37			+ 00100101
Exceeds 99 → 115			01110011
	+ 156		10011100
1 × 100 + 15		1	00001111

If the result of the previous addition was less than 100, there would be no BCC carry and no correction to add.

Although the detection circuit for $S \geq 100$ is easy to realize with a couple of gates, it is more attractive to use a ROM because the same ROM may be used to make correction, to generate BCC carry bit and, finally, to perform BCC to BCD conversion after calculations have been made to a desired precision.

The ROM is a binary-to-BCC converter where 8 bit binary code will be converted to a corresponding BCC equivalent and a centimal carry, if any. It is not necessary to consider the most significant bit with value 2×100 since the greatest sum of two BCC digits is

$$99 + 99 = 198$$

The final circuit for BCC correction is shown in Figure 1.

Two MCM 14524 with a pre-programmed mask for binary-to-BCC conversion are used. An input latch MC14508 performs the function of storing the sum. The circuits are connected via 3-state interfacing circuitry to the computers memory bus. They can be considered as a part of the computers' memory as they occupy three free consecutive storage locations. Since the latch has 3-state out-

puts, it could be a write-read location. The outputs of the ROMs and the BCC carry bit are read-only locations. The ROM has a dynamic access and needs a clock pulse which can be derived from write pulse when inserting a delay to allow the propagation through the latch. The set-up time from address change to the negative clock edge has to be considered, too.

It is assumed that a decoded address for the three particular locations is available.

In order to perform BCC subtraction, no external circuits are needed. The two's complement subtraction is made in an usual way by complementing the subtrahend and forcing the carry into the least significant position. If there was no carry output, the correction has to be made by adding 100 (binary:01100100) to the result while ignoring carry output bit resulting from this operation.

This operation can be carried out inside the central processor unit without difficulty, since the state of the carry flip-flop is the only criteria for correction. One normal storage location or an internal 8 bit register can be used to store number 100 which is then added to the result when there was no carry resulting from previous subtraction.

Note that the numbers handled by the system are in BCC code which is equivalent to binary code. When the numbers are entered via key-board, then the conversion from BCD to BCC has to be made after every two numbers keyed in.

A conversion table from BCD to binary could be stored in the other unused half of the ROMs. Figure 2 shows another simple approach of BCD to BCC conversion. Note that the more significant digit is shifted one place to the left and added to the low significant BCD digit. The same four bits are added again shifted into the fourth place from the right to the left. As every shift corresponds to the binary multiplication by two, the more significant BCD digit has thus been multiplied by two and by eight and both partial products have been added to the lower significant digit. The result is $S = (2B + 8B) + A = 10B + A$ which is the desired binary value for the two digits. As it is necessary anyhow to shift four bits to the left every time when a new BCD digit is keyed in, the saving of computation time, therefore, will not be greatly improved by using direct conversion technique. The shorter computation time results, however, from the fact that no carries will be generated at conversion time in the higher digit positions when BCC coding is used.

CONCLUSION

It has been shown on a particular example that the complexity of the CMOS circuits is high enough to realize a relatively complicated circuit for improving performance of a microprocessor. Combined with other advantages of CMOS, this will probably lead to new interesting developments in the computer industry. Where the speed is not critical CMOS will find wide acceptance.

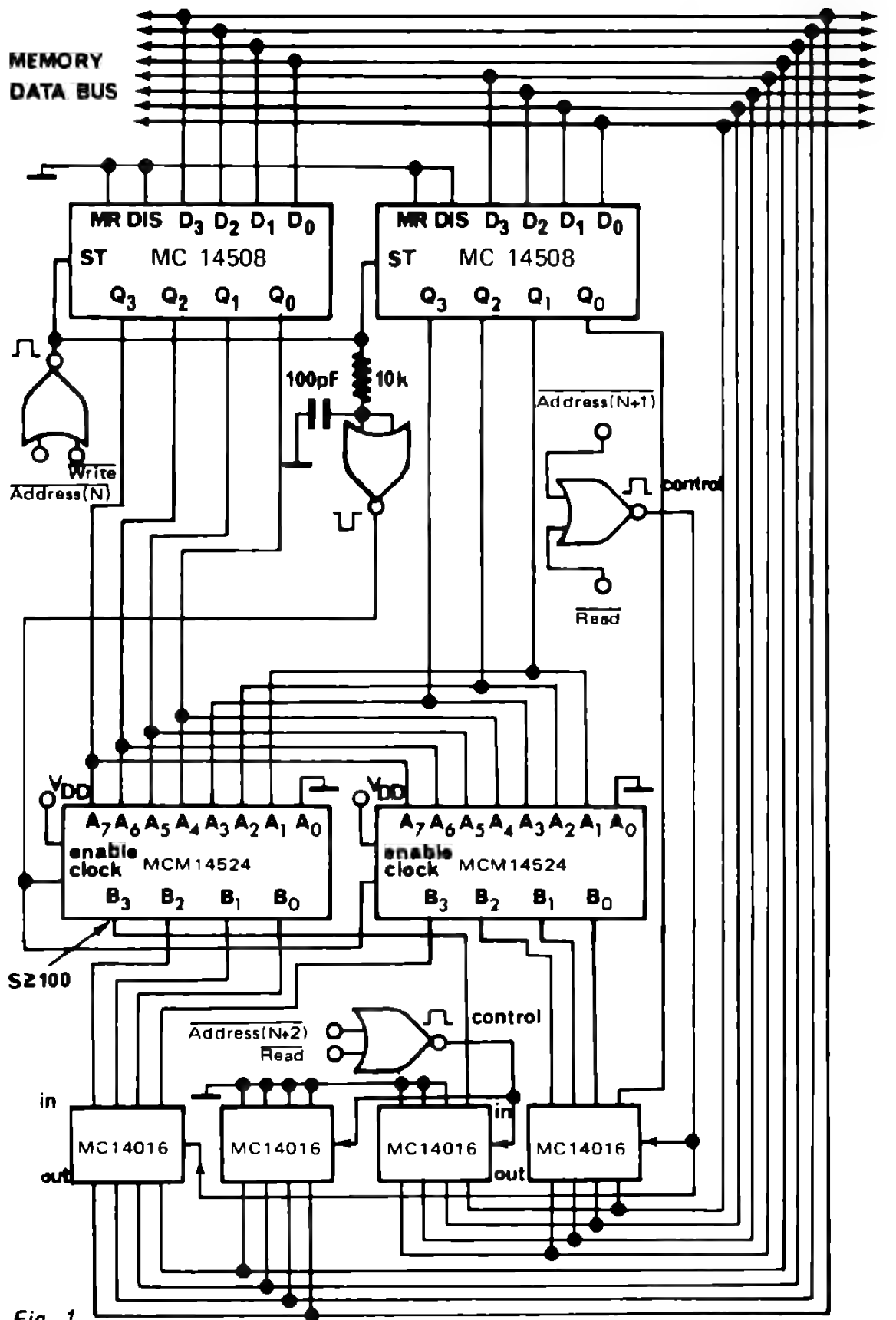
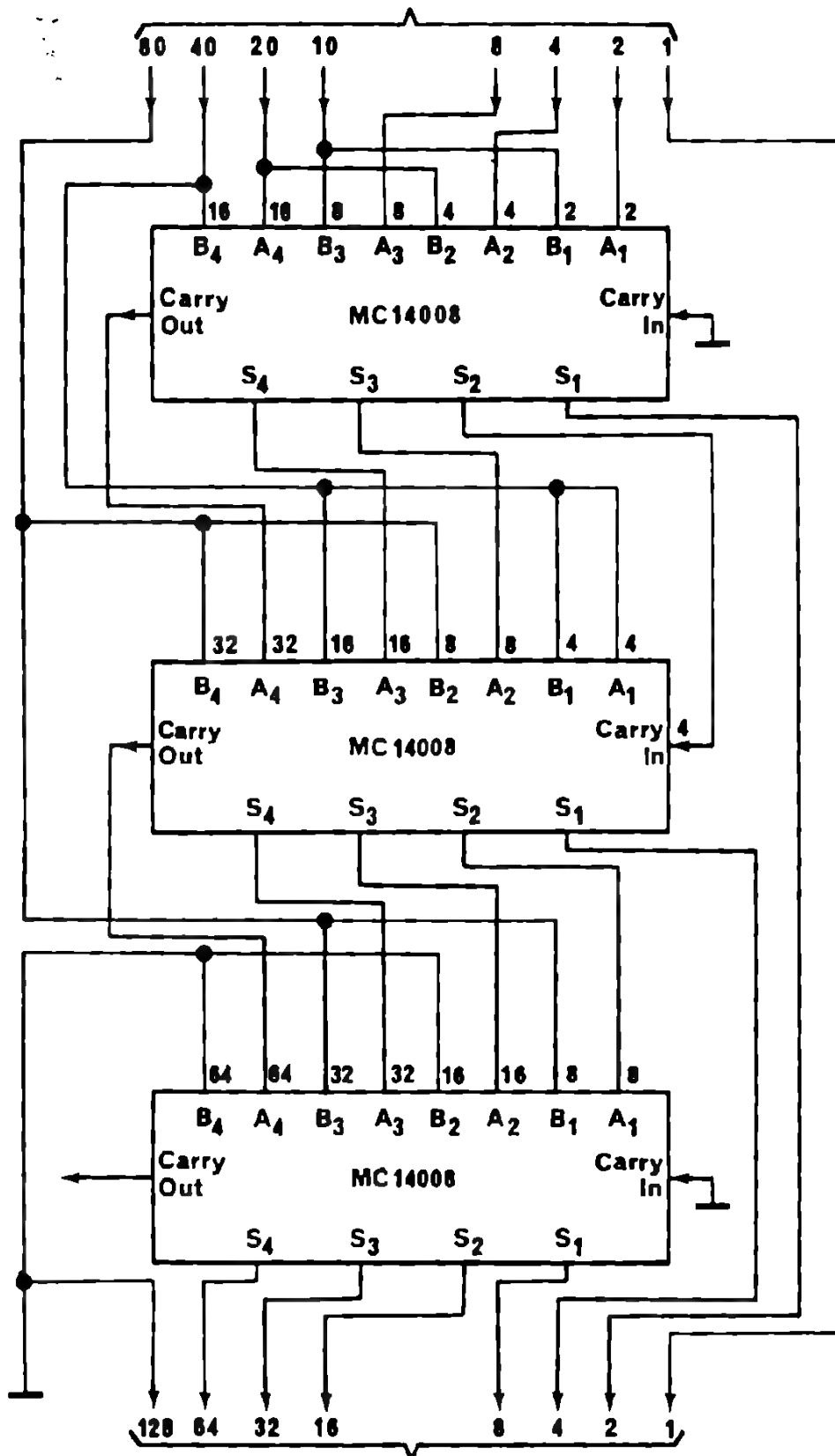


Fig. 1

B·C·D NUMBER TWO DIGITS



B·C·C OR BINARY NUMBER 8 BITS

...

ommunications
pplications

COMMUNICATIONS APPLICATIONS

A FREQUENCY SYNTHESIZERS

1. INTRODUCTION
2. VARIOUS TYPES OF FREQUENCY
 SYNTHESIZERS
3. PHASE-LOCKED LOOP
 BASIC RELATIONS
4. PRACTICAL EXAMPLES
5. REFERENCES

B PULSE CODE MODULATION

1. P.C.M. TRANSMISSION IN
 TELEPHONE NETWORKS
2. DIGITAL COMPRESSOR
 USING CMOS
3. DIGITAL EXPANDER
 USING CMOS
4. SERIAL-TO-PARALLEL
 CONVERTER
5. CONCLUSIONS
6. REFERENCES

C DATA TRANSMISSION

FREQUENCY GENERATOR
FOR LOW - SPEED
MODEMS USING CMOS
COMPLEX FUNCTIONS
(CCITT - Recommendation V-21)

A FREQUENCY SYNTHESIZERS

1. INTRODUCTION

Frequency generation realized by means of digital frequency synthesizers using a phase-locked loop is now a widely used technique. Many circuits in TTL or ECL technology presently exist, permitting satisfactory implementation of systems with frequencies up to 500 MHz.

There is nevertheless one point that has been, so far, not ignored but accepted: this is the relatively large dc-power required by these circuits. The introduction of integrated circuits in CMOS technology allows one to solve this problem at least partially.

Frequency synthesis, strictly speaking, is the generation of many equally spaced frequencies within a given band starting from a single frequency source. The speed of the circuits to be used is determined by the width of this band, and not necessarily by the absolute value of the output frequencies to be generated — depending on the type of configuration used.

The result is that with the CMOS integrated circuits presently available, the largest band that can be handled — without splitting it — is of the order of 5 MHz at most.

2. VARIOUS TYPES OF FREQUENCY SYNTHESIZERS

2. 1. PURELY DIGITAL ONE-LOOP CIRCUITS

Figure 1 shows the simplest form of a frequency synthesizer. This is a one-loop circuit with the reference frequency equal to the channel spacing.

The presently available programmable counters, the MC 14522 and MC 14526, have a guaranteed operating frequency of 3 MHz at 10V, which determines for that voltage the limits of use of this configuration with CMOS circuits only.

The addition of a frequency expander increases this limit by about 40%.

(Fig. 2). The principle of operation of such a circuit consists of detecting the "two" state of the least significant counter stage. The reset time of the counters can then be increased to two full cycles of the clock and consequently their speed be made higher. The only restriction is that it is no longer possible to divide by 2, 1 or 0 (Ref. 1).

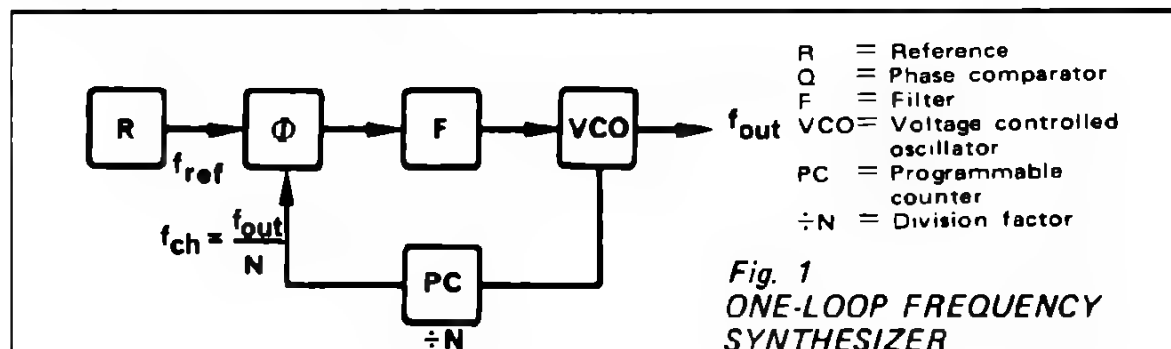
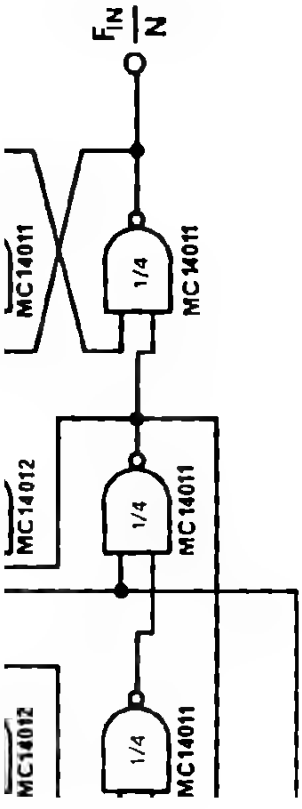


Fig. 2
FREQUENCY EXPANDER



the VCO frequency must exceed the capabilities of the programmable counter, fixed prescaler can be inserted as shown in Figure 3.

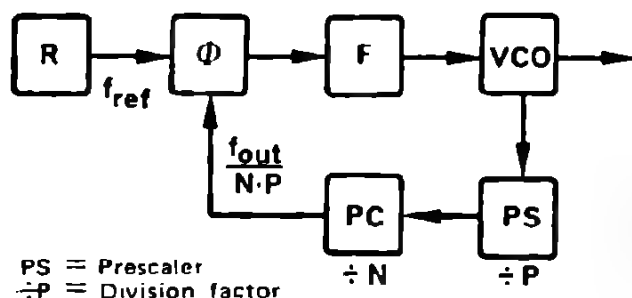


Fig. 3
FREQUENCY SYNTHESIZER
USING FIXED PRESCALING

The disadvantage of this configuration are:

1. The reduction of the reference frequency, which is no longer equal to the channel spacing and can be more difficult to filter out

$$f_{\text{ref}} = \frac{f_{\text{out}}}{N \cdot P} = \frac{f_{\text{ch}}}{P}$$

2. The increased total division factor ($N_T = N \cdot P$) which decreases the loop bandwidth and gain (Ref. 3).

As normally implemented, this would mean a hybrid solution using a prescaler in ECL or TTL technology and the remaining in CMOS technology.

A good solution to the above-mentioned problems is the use of a variable modulus prescaler, (e.g. the MC 12012 along with the MC 12014, Ref. 1 and 2). With this configuration, shown in Figure 4, the reference frequency is again equal to the channel spacing. The split between CMOS and other technologies will be made at the program counter level.

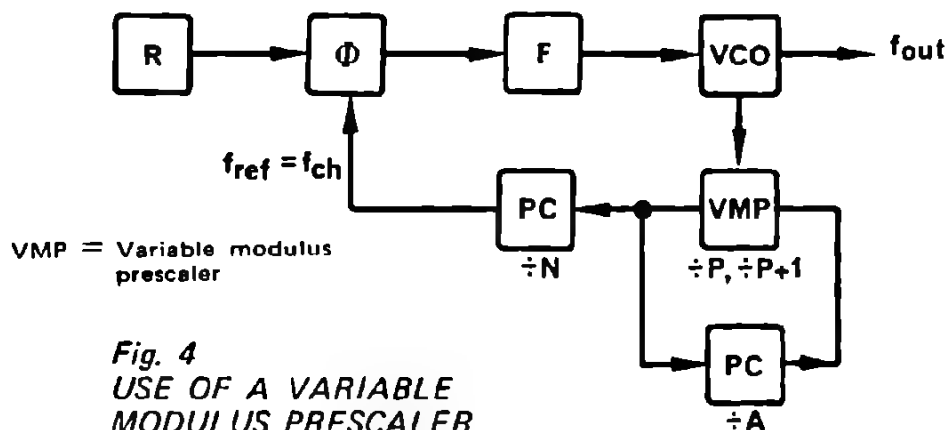


Fig. 4
USE OF A VARIABLE
MODULUS PRESCALER

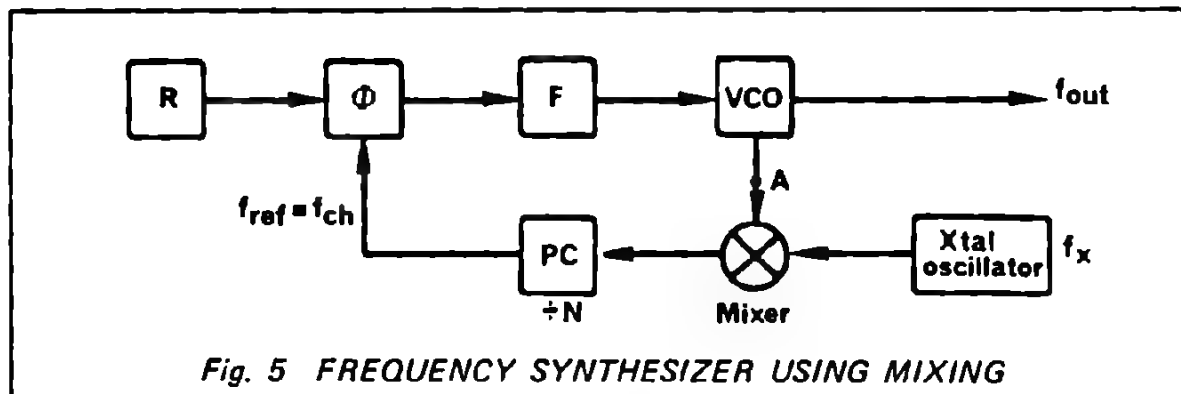
The total division factor N_T in this case is equal to:

$$N_T = (P+1)A + P.(N-A)$$

where P and $P+1$ are the dividing factors of the prescaler. Operation starts by using the higher count (A times) and then the lower count ($N-A$ times) depending on the required total division factor N_T .

2. 2. ONE-LOOP CIRCUIT USING MIXING

Figure 5 shows a mixer-type frequency synthesizer.



The output frequency is converted down and the highest operating frequency of the synthesizer is essentially determined by the bandwidth to be handled. In practice, a guard band must be added to avoid lock with the image frequency.

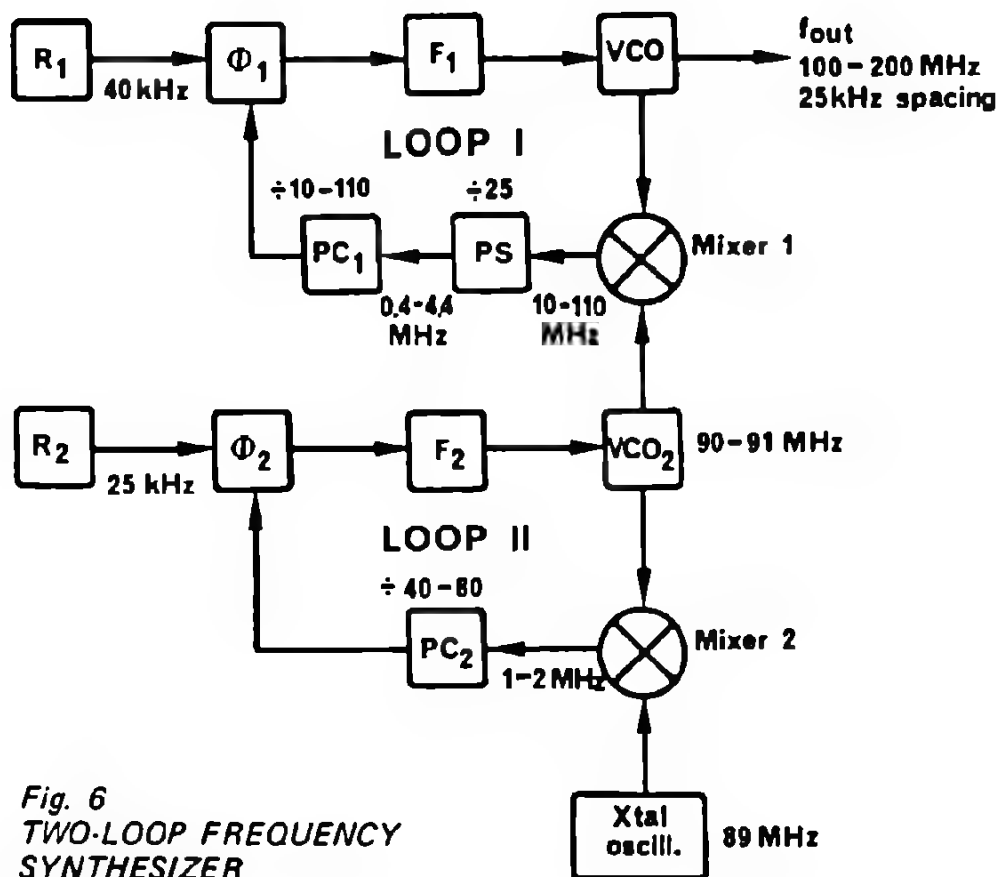
The advantages of this solution are that:

1. The reference frequency can be made equal to the channel spacing
2. The total division factor is greatly reduced, thus increasing loop bandwidth and gain
3. The frequencies to be handled are lower, thus allowing the widest use of CMOS circuits.

The only disadvantage is the creation of spurious beat frequencies that are within the band and difficult to reject. Normally an amplifier with high attenuation from mixer to VCO must be inserted at point A. An easier solution to implement is the use of a fixed prescaler (divide by 2) instead of the amplifier. This shifts by one octave the spurious beats but also decreases the reference frequency with respect to the channel spacing and makes necessary the use of a high frequency circuit (with higher power consumption).

2. 3. TWO-LOOP CIRCUIT

Two-loop circuits are useful for narrow channel spacing or in the case of very large bandwidths. Figure 6 shows the block diagram of a configuration using mixing.



The large steps (e.g. 1 MHz) are made by loop I. A fixed prescaler can easily be used in this loop without reducing the reference frequency to very low values. Loop II will be used for the small steps (e.g. 25, 12.5, 10 KHz or less). The divide factors are small in both loops thus retaining high loop bandwidth and gain.

The disadvantages of this configuration are:

- . The generation of spurious beat frequencies
- . The use of a second VCO for mixing, which never has as good spectral purity as a crystal oscillator.

Figure 6 also shows an example of a circuit for use between 100 and 200 MHz with 25 KHz channel spacing. The frequency generated by VCO₂ is used to convert the output frequencies down to 10–110 MHz. The fixed prescaler is in CL technology. This is the only digital circuit operating at very high frequencies. All other parts can be in CMOS, with the exception of the VCOs, where low noise discrete semiconductors are recommended. The two reference frequencies are high enough to make filtering easy.

3. PHASE-LOCKED LOOP BASIC RELATIONS

For a detailed analysis, see Ref. 3 and 4. It will just be mentioned here that the type or order of the loop needed for a given application must be first determined. This is done through the analysis of the loop stability for different inputs to the comparator. In case of frequency synthesizers, a type 2 loop is normally required. This means that the steady state phase error must be zero for a step velocity input (or sudden frequency difference between the signal and reference applied to the phase comparator).

Once the circuits are chosen (loop configuration, phase comparator, VCO, program counter), each having its own transfer function, the only variable left for determining the needed loop type is the filter.

The system is also fully characterized by two parameters: the damping factor ζ and the natural frequency of oscillation of the loop ω_n . ζ and ω_n depend on the parameters, or gain constants, of the individual circuits. ζ determines the overshoot and ω_n the speed of response of the loop. A system will be designed to have a prescribed value of overshoot and a certain settling time. The selection of ζ and ω_n allows the calculation of all other parameters.

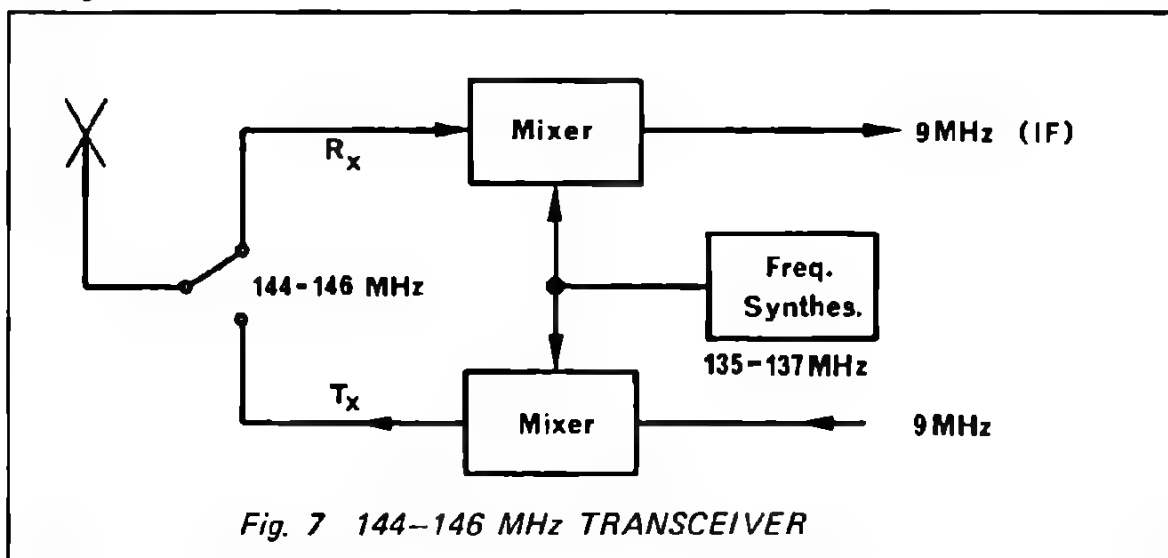
The loop bandwidth or cut-off frequency ω_{3db} is proportional to ω_n and ζ . Any frequency variation at the output is compensated for by a change of the VCO input as long as the speed of this change lies within the cut-off frequency of the loop. The main function of a loop utilizing phase lock between a very stable frequency reference and an oscillator of poor stability, is to transfer the properties of the reference to the oscillator. The higher the loop gain and bandwidth, the better this transfer becomes.

Frequency modulation applied to the VCO will be possible at frequencies beyond the loop cut-off frequency.

4. PRACTICAL EXAMPLES

4. 1. FREQUENCY SYNTHESIZER FOR THE BAND 144–146 MHz

The example shown below refers to a frequency synthesizer for the amateur frequency band 144–146 MHz. It is considered as a part of the system shown in Figure 7.



The main specifications for the frequency synthesizer are the following:

Output frequency : 135–137 MHz
Channel spacing : 10 kHz
Noise : 80db at ± 1 channel
Power dissipation : minimum possible.

The design has been made using only CMOS technology. The circuit consists of:

1. Three MC 14522 counters
2. One MC 14046 phase comparator
3. A balanced mixer
4. A MC 14518 divider
5. Two 2N918 for the VCO and the crystal oscillator
6. Two MC 1550G as buffers

The phase comparator guarantees that no lock will occur on harmonics. Its hold-in range is determined by the VCO frequency range. Its capture range is equal to its hold-in range.

Figure 8 shows the detailed circuit schematic of the synthesizer.

The synthesizer is controlled by thumbwheel switches. For a setting at 144.750 MHz for example, the three counters are pre-set at 4 (x1MHz), 7 (x100KHz) and 5 (x10KHz), since they are directly connected to the BCD switches. For this setting the synthesizer generates a frequency of 135.750 MHz. The division factor of the counter must then be:

$$\frac{135750 - 134500}{10} = 125$$

The total division factor varies between 50 and 250, in covering the desired frequency band.

Since the counters are set for counting 475, the count must be stopped at 350. This is possible with the MC 14522 counters connected as shown, making the design very simple.

Test results:

Power consumption at 135 MHz output frequency.

Supply voltage	7V	10V	14V
VCO and Buffers	70mW	150mW	304mW
134.5 MHz Xtal oscillator	4.2	18	56
1 MHz Xtal oscillator and $\div 100$ -divider	6	22	74
Program counters	7.7	32	63
Phase-detector and MC 14011	11.5	42	133
TOTAL	99.4mW	264mW	630mW

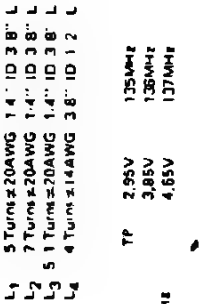
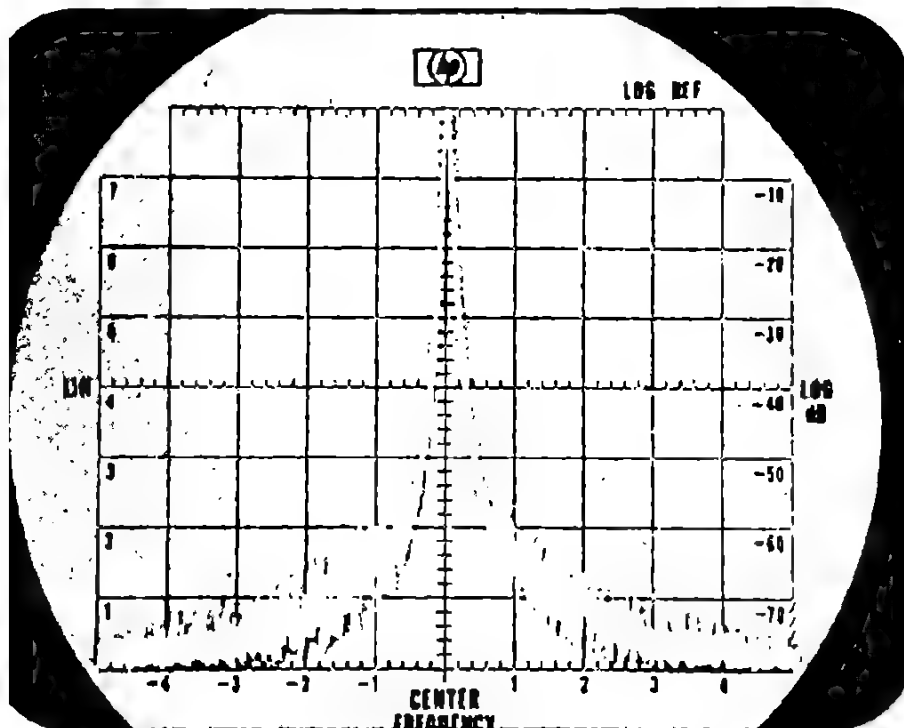
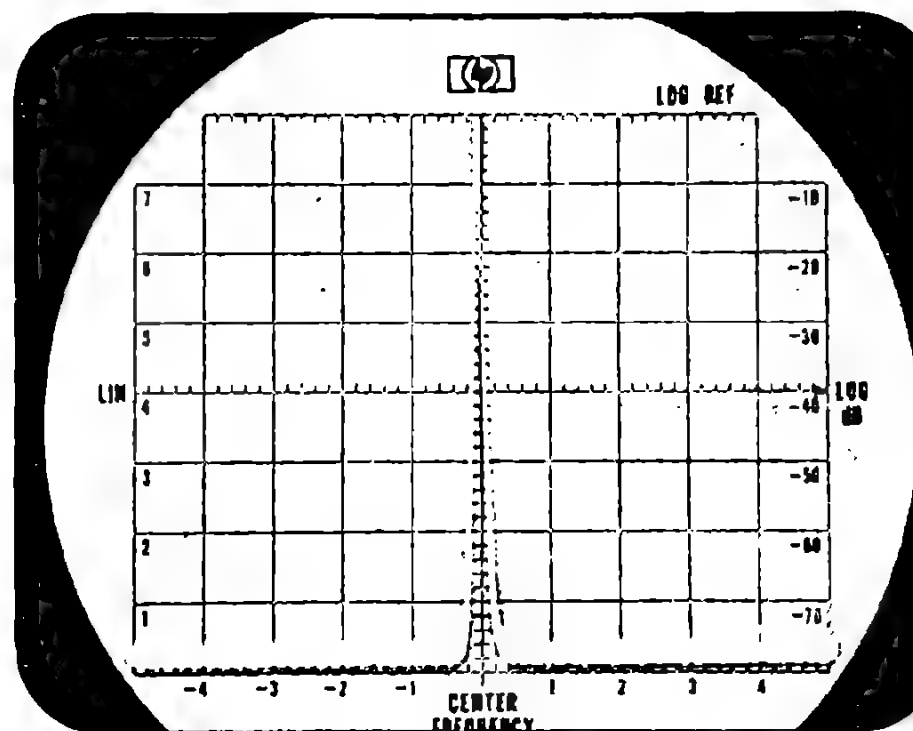


Figure 9 shows the spectral purity around the carrier. Figure 10 shows the complete band from 135 to 137 MHz, with the carrier at 136 MHz.



$f_{out} = 136 \text{ MHz}$
 $X = 5 \text{ KHz/div.}$

Fig. 9 SPECTRUM AROUND THE CARRIER



$f_{out} = 136 \text{ MHz}$
 $X = 200 \text{ KHz/div.}$

Fig. 10 SPECTRUM FOR THE BAND

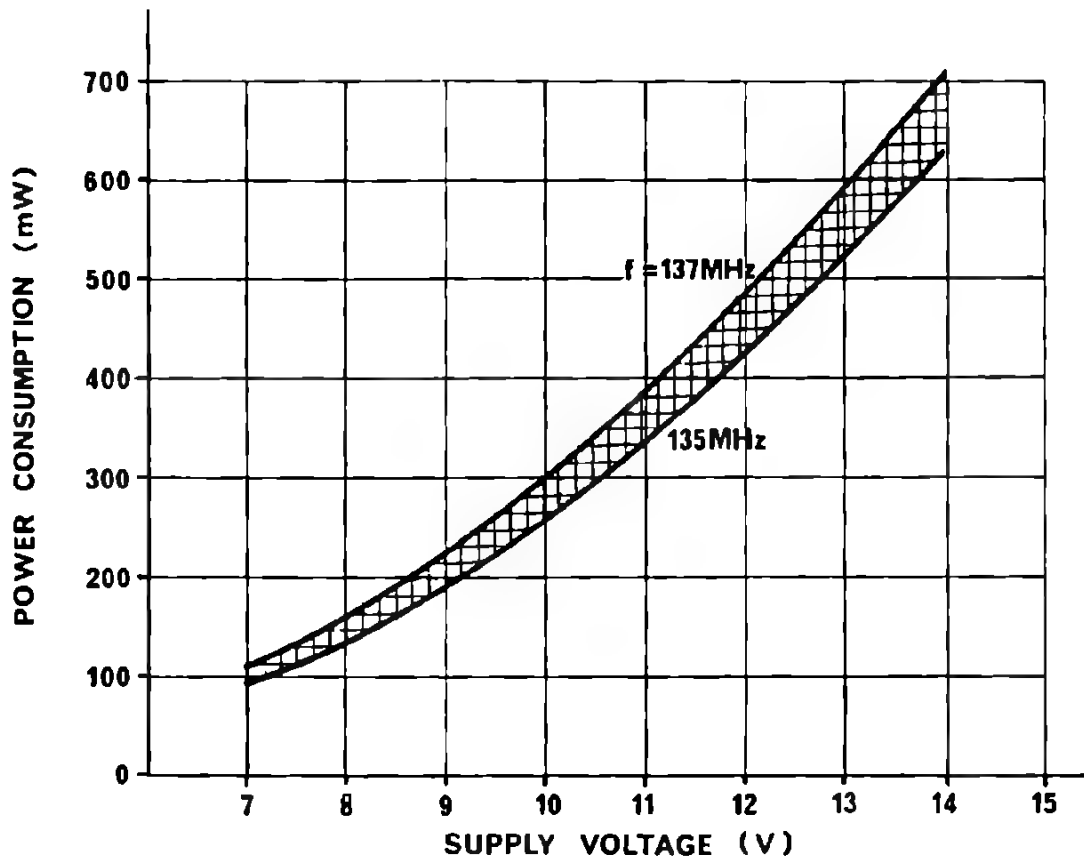


Fig. 11 POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

he circuit works correctly with power supply voltages ranging from 7 to 15V. he power consumption varies as indicated in Figure 11, as a function of the pply voltage and frequency.

REFERENCES

MC 12014 MOTOROLA Data-sheet
 MC 12012 MOTOROLA Data-sheet
 MOTOROLA Application Note AN-535
 MOTOROLA Application Note AN-532A

3 PULSE CODE MODULATION

1. P.C.M. TRANSMISSION IN TELEPHONE NETWORKS

1. FUNDAMENTALS

A P.C.M. transmission system is one in which the analog information of the speech is transmitted in a digital form (Fig. 12).

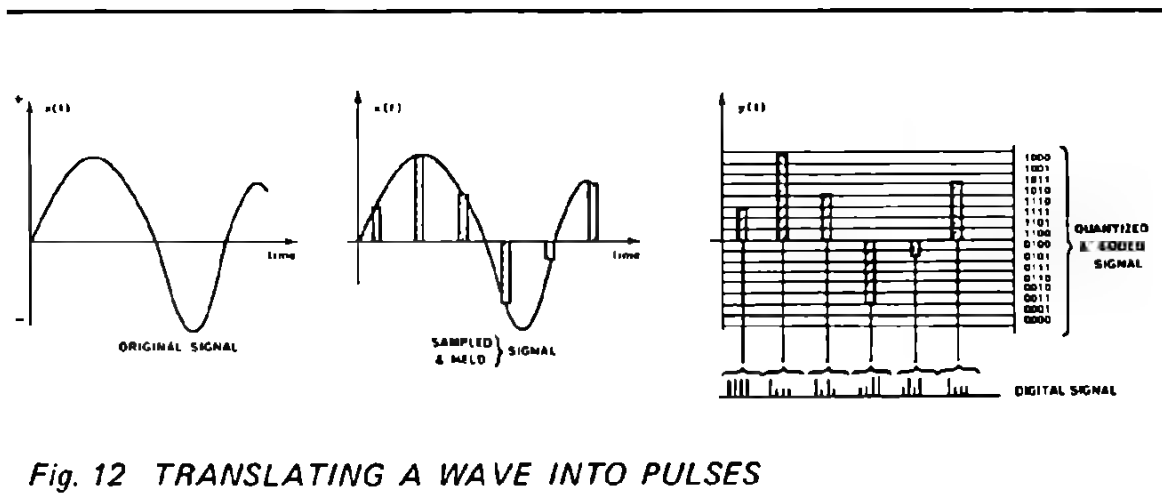


Fig. 12 TRANSLATING A WAVE INTO PULSES

The original speech signal is sampled at regular intervals. Thus, a series of pulses, modulated in amplitude, (P.A.M.), is obtained and submitted to an operation of quantisation and coding. The operation of quantisation consists of assigning a binary number to represent the amplitude of the sample.

As shown in Figure 13, the transmission of each sampled value requires only a short time, so it is possible to multiplex in time (Time Division, Multiplexing, T.D.M.) other samples from different sources on the same line. A main advantage of P.C.M. is that it is very easy to transmit either digital or analog data on the same link since the mode of transmission is digital in both cases.

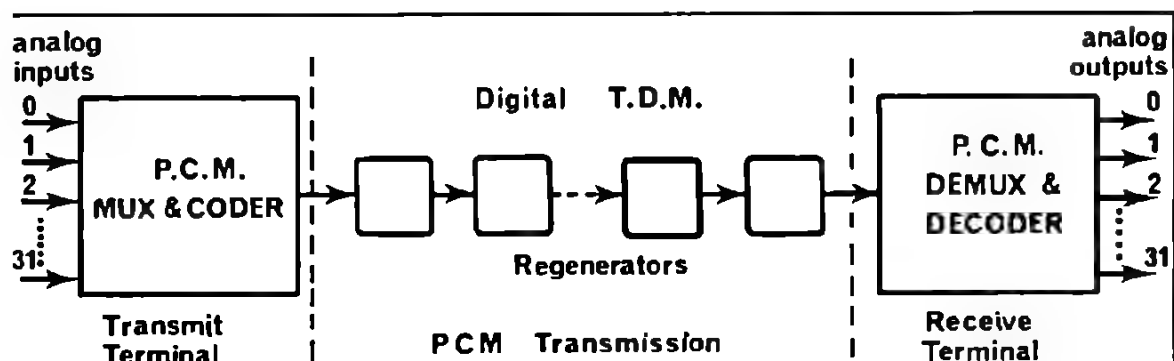


Fig. 13 OUTLINE OF A P.C.M. TRANSMISSION

Replacing the continuous function $x(t)$ of the speech signal by discrete values $y(t)$ implies that the signal will be reconstructed with an error. This error will be inversely proportional to the number of levels of quantisation employed. Thus, if n equals the number of pulses quantising the amplitude, the maximum number of discrete steps in a binary code will be 2^n , and the size of each step will be equal to $1/2^n$ of the total amplitude. The error incurred will result in a distortion called quantisation noise. The quantisation noise is a white noise, if n is a large number, and the mean square error E^2 is given by :

$$E^2 = \frac{q^2}{12} \text{ where: } q = \text{one quantum step} = \frac{1}{n}$$

n is a large number and all quantisation levels must be equally likely.

Uniform quantising is not usually the best choice for a P.C.M. codec (coder, decoder) and generally non-linear quantising is used. This is because the dynamic range of telephone speech signals can be as much as 40 dB owing to differences between talkers and also to the different lengths of the wires in the connecting circuit. Thus, if an uniform codec is used, the quantising noise power being constant for all signal levels, the signal-to-noise ratio for weak signals may be 40 dB less than for strong signals. In addition, the probability distribution of speech amplitudes is not uniform, small amplitudes being more likely to occur than large ones. The total quantising noise power can therefore be reduced by reducing the quantum step size at the low levels and increasing it at high levels. This operation corresponds to a signal compression for high amplitude speech and expansion for low level speech. Note that if the resolution adopted for low levels is kept constant over all the range of amplitudes, a large bandwidth is required for each channel. Therefore the compression allows a reduction in the bandwidth of the channel. There are three methods of realizing non-linear quantising (see Fig. 14) which give similar results.

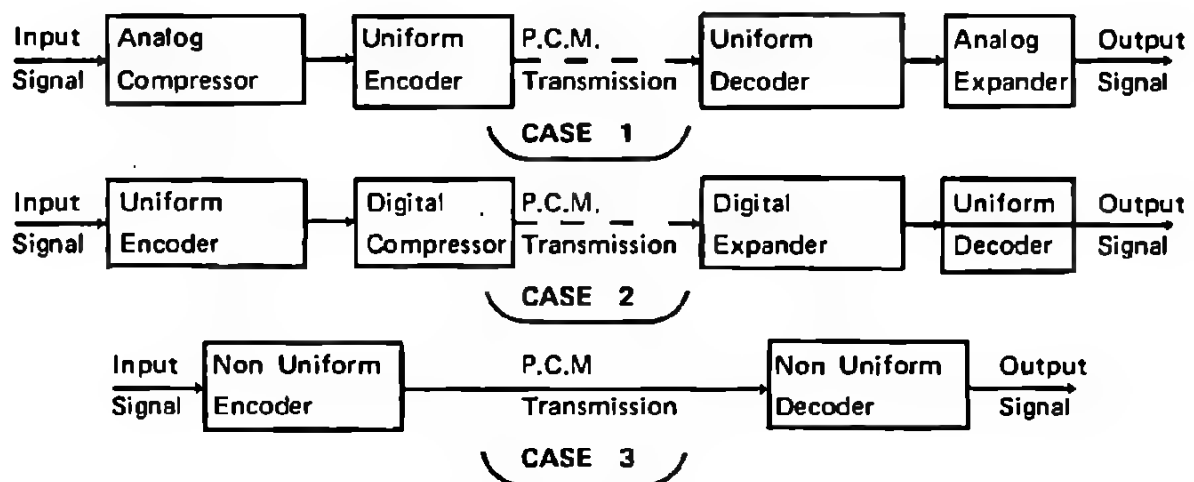


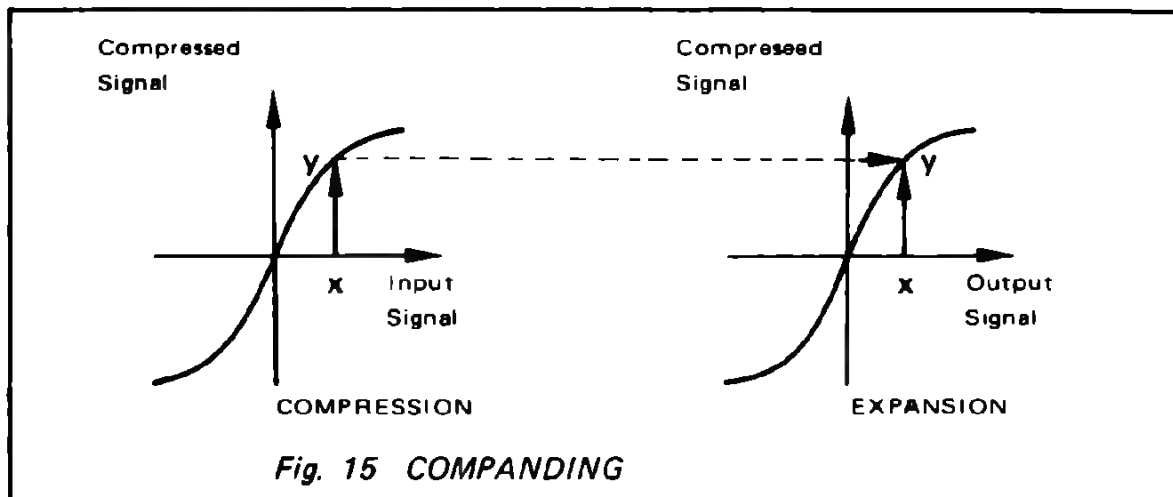
Fig. 14 SCHEMATIC OF P.C.M. CODECS

In the first of these, the input signal amplitudes' range is compressed by means of an analog circuit before the uniform encoding. A corresponding expansion is applied after uniform decoding and so the original signal is recovered at the output.

In the second method the process of compressing and encoding is reversed using a digital compressor after uniform encoding. This process is essentially digital and consequently more reliable than the first one, but it needs a more accurate and faster analog-to-digital converter.

The third method is a compromise between the first two and uses multiplying A/D and D/A converters such as current switches with variable references. This case is usually the least complex because the logic is very simple and also reduction of variation caused by temperature changes is easier than in the first case. The three methods give the same result and it is possible to have terminals working with any one of the three.

The complete process of compression and expansion, as can be seen in Figure 15, is called companding.



Two logarithmic companding laws have been widely used. Their principal characteristics are shown in the following table:

American law (μ law)	European law (A law)
$y = \frac{1 + \log(1 + \mu x)}{\log(1 + \mu)}$	$y = \frac{1 + \log Ax}{1 + \log A} \quad 1/A \leq x \leq 1$
$\mu = 255$	$y = \frac{A \cdot x}{1 + \log A} \quad 0 \leq x \leq 1/A$
Approximated by 15 straight lines.	$A = 87.6$
	Approximated by 13 straight lines.

$$x = \text{input level of the compressor} = \frac{V_{in}}{V_{in \text{ max.}}}$$

y = output level of the compressor.

Table 1

The normalized approximation of the "A law" shown below (Fig. 16) corresponds to a 12 bits linear quantisation. In this "curve" the slopes of the segments are related by powers of two (except for the first two). The different segments are obtained by successively dividing the horizontal axis by two for each 16 units in the vertical axis.

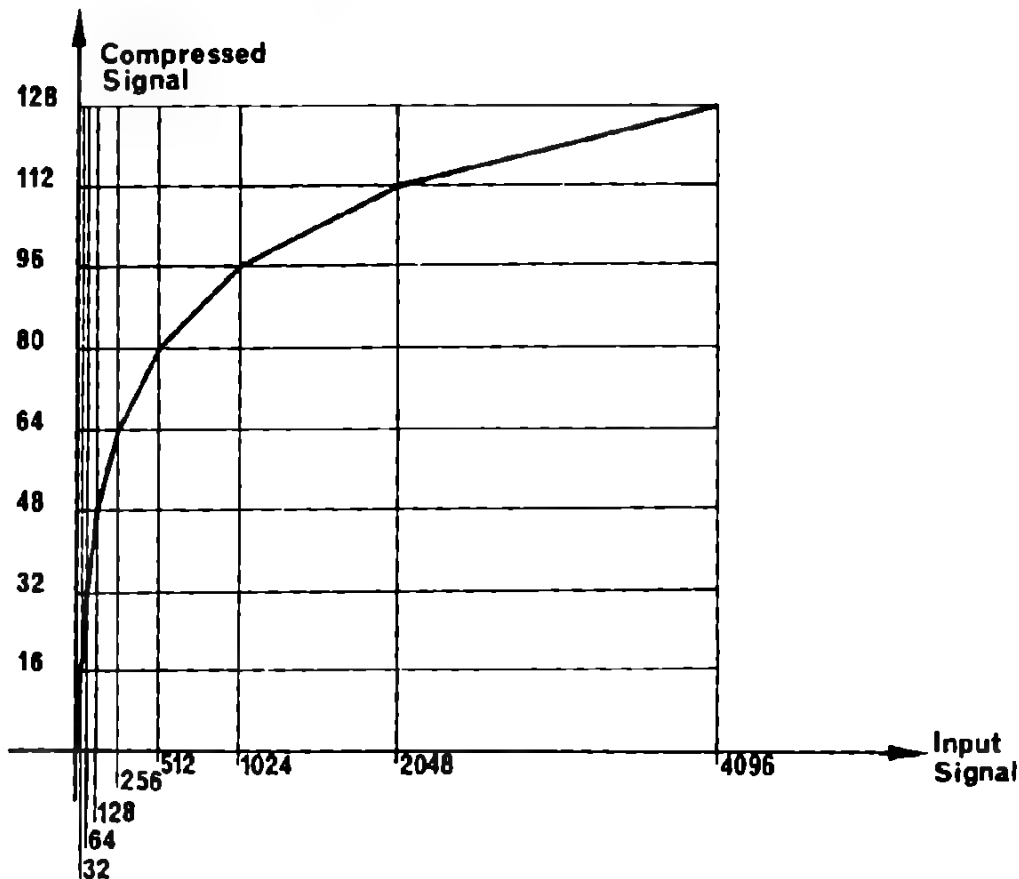


Fig. 16 NORMALIZED APPROXIMATION OF THE "A LAW"

2. DIGITAL COMPRESSOR USING CMOS

2. 1. FUNDAMENTALS

When the A-D conversion is performed by a 12 bit A-D-C (or an eleven A-D-C with polarity digit) it is still necessary to convert the 12 bit words to the proper 8 bit words adopted for transmission. The organization of such a word according to the CCITT-recommendation is as follows:



Fig. 17 8 BIT TRANSMITTED WORD

The first bit 0 gives the polarity of the signal, bits 1, 2 and 3 the segment and 4, 5, 6 and 7 assign the closest binary number within a segment to represent the level of the sample considered.

This operation of compression of 12 bits into 8 bits can be summarized by the following table, where bits A4, A5, A6 and A7 in the compressed code represent the inputs S to the D-A-C which must be activated according to the address given by the segment bits A1, A2 and A3.

LINEAR CODE													COMPRESSED CODE								
Seg- ment	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	A1	A2	A3						
7	POLARITY DIGIT	1	A4	A5	A6	A7	1	0	0	0	0	0	POLARITY DIGIT	1	1	1	A4	A5	A6	A7	
6		0	1	A4	A5	A6	A7	1	0	0	0	0		1	1	0	A4	A5	A6	A7	
5		0	0	1	A4	A5	A6	A7	1	0	0	0		1	0	1	A4	A5	A6	A7	
4		0	0	0	1	A4	A5	A6	A7	1	0	0		1	0	0	A4	A5	A6	A7	
3		0	0	0	0	1	A4	A5	A6	A7	1	0		0	1	1	A4	A5	A6	A7	
2		0	0	0	0	0	1	A4	A5	A6	A7	1		0	0	1	0	A4	A5	A6	A7
1		0	0	0	0	0	0	1	A4	A5	A6	A7		1	0	0	1	A4	A5	A6	A7
0		0	0	0	0	0	0	0	A4	A5	A6	A7		1	0	0	0	A4	A5	A6	A7

Table 2

Note that the above table corresponds to a truth table at the decoder input in which it is necessary to have a resolution one half LSB higher than in the A-D-C as explained later.

It is possible to implement a combining type digital compressor using MSI CMOS with only a few packages because of the many functions available in the MOTOROLA CMOS family. Such a compressor works in the parallel mode, therefore its speed may be eight times slower than in the serial mode. On the other hand, the speed of the compressor depends only on its time delay, not on any clock rate, and thus may be much faster than if a serial mode were used.

2. 2. REALIZATION OF A DIGITAL COMPRESSOR USING CMOS

Bits A1, A2, and A3 are easily obtained in one package by using the MC 14532 priority encoder. Indeed, from the eight inputs present the highest valued one causes the device to produce a binary output corresponding to the address. The lowest input of MC 14532 is connected to output S8 of the A-D-C (see Fig. 18).

As seen in table 2, bits A4, A5, A6 and A7 of the compressed code are obtained by shifting the four LSB's of the A-D-C successively by one bit. This operation provides the increase by a power of two, needed for every segment. Note that because the slope is the same for the first two segments, the internal code of the compressor is not the same as in transmission. The internal code produces the proper shift of the A-D-C's outputs. The simplest manner to achieve this is by using a second MC 14532 priority encoder having its lowest output connected to the output S7 of the A-D-C (Fig. 18).

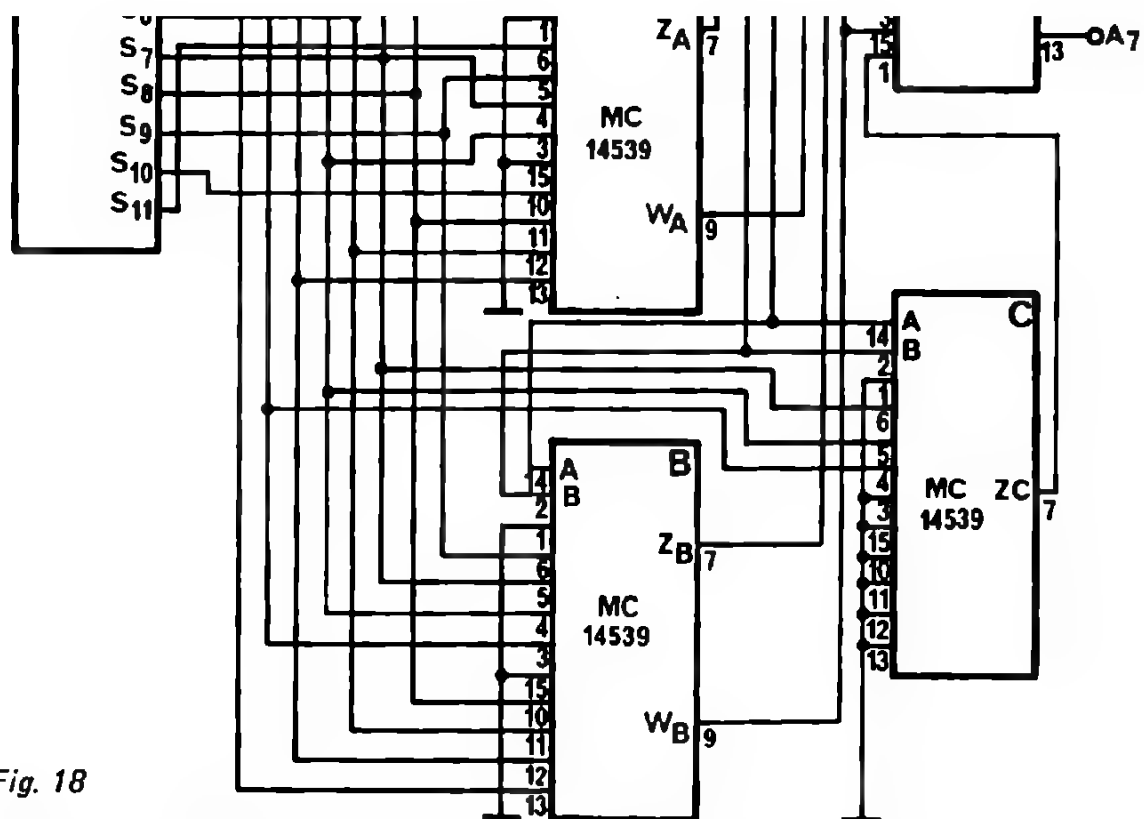


Fig. 18

DIGITAL COMPRESSOR FOR P.C.M. TRANSMISSION USING MOTOROLA CMOS

INPUT									OUTPUT				
E _{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E _{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

Table 3 MC14532 TRUTH TABLE

In the American system, the approximation of the "μ law" is made by 15 straight lines each having a ratio of a power of two. The second MC 14532 is not needed because the internal code is the same as the transmitted one.

To generate the proper staircase at each segment it is still necessary to switch the corresponding output of the A-D-C. This operation can be performed by an interesting method using three MC 14539 digital MUX and one MC 14519 four bit AND/OR selector. The following truth table gives the internal and external code and also the input code of MC 14539 and MC 14519.

Seg- ment	TRANSMITTED CODE								INTERNAL CODE									
	A1	A2	A3	A4	A5	A6	A7	A'1	A'2	A'3	KA	KB	AA	BA	AB	BB	AC	BC
0	0	0	0	S3	S9	S10	S11	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	S7	S8	S9	S10	0	0	0	1	0	0	0	0	0	0	0
2	0	1	0	S6	S7	S8	S9	0	0	1	0	1	0	0	0	0	0	0
3	0	1	1	S5	S6	S7	S8	0	1	0	1	0	1	0	1	0	X	X
4	1	0	0	S4	S5	S6	S7	0	1	1	0	1	1	0	1	0	1	0
5	1	0	1	S3	S4	S5	S6	1	0	0	1	0	0	1	0	1	X	X
6	1	1	0	S2	S3	S4	S5	1	0	1	0	1	0	1	0	1	0	1
7	1	1	1	S1	S2	S3	S4	1	1	0	1	0	1	1	1	1	1	1

Table 4 TRUTH TABLE OF INTERNAL AND TRANSMITTED CODES

Input code of MC 14519

KA = A'3

KB = A'3

Input code of MC 14539

AA = AB = AC = A'2

BA = BB = BC = A'3

1. 3. OPERATION OF THE DIGITAL COMPRESSOR

The schematic diagram below shows a circuit used for testing the operation of the digital compressor (D.C.). The MC 14040 simulates an A-D-C which converts a linear ramp (alternatively positive and negative) to a digital form. The P.C.M. decoder is one that was tested in an operational equipment and corresponds to CCITT-recommendations.

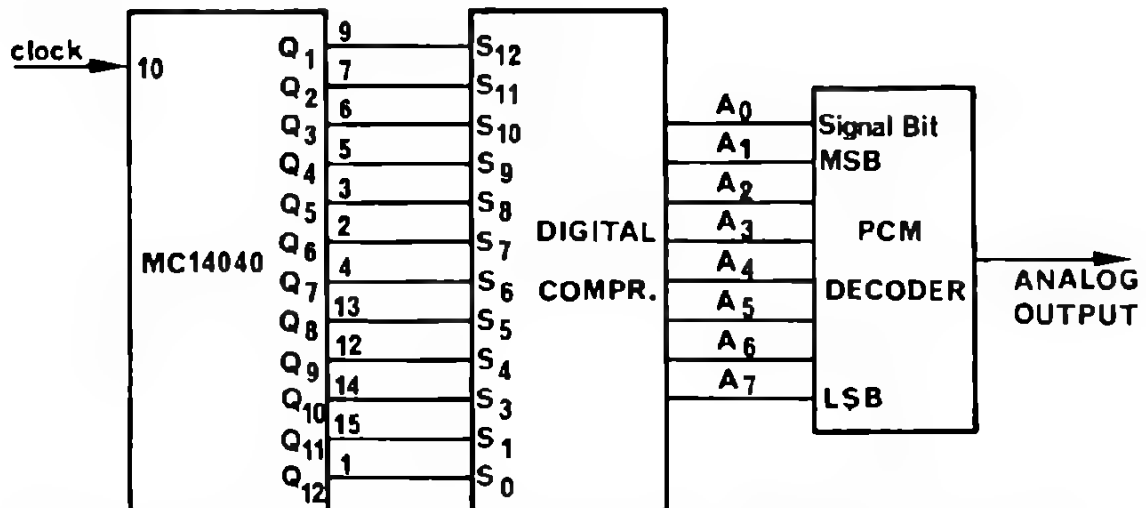


Fig. 19 SCHEMATIC DIAGRAM USED FOR TESTING THE TRANSFER CHARACTERISTIC AND THE TIMING DIAGRAM

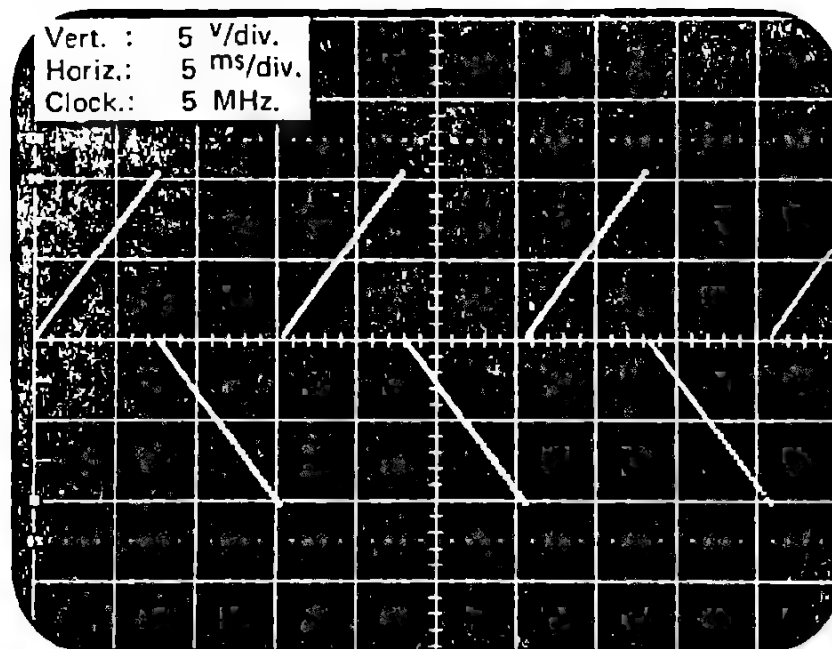


Fig. 20
TRANSFER CHARACTERISTIC
ACCORDING TO THE CIRCUIT

Fig. 21 TIMMING DIAGRAM OF THE 4MSB AT THE COMPRESSOR OUTPUT

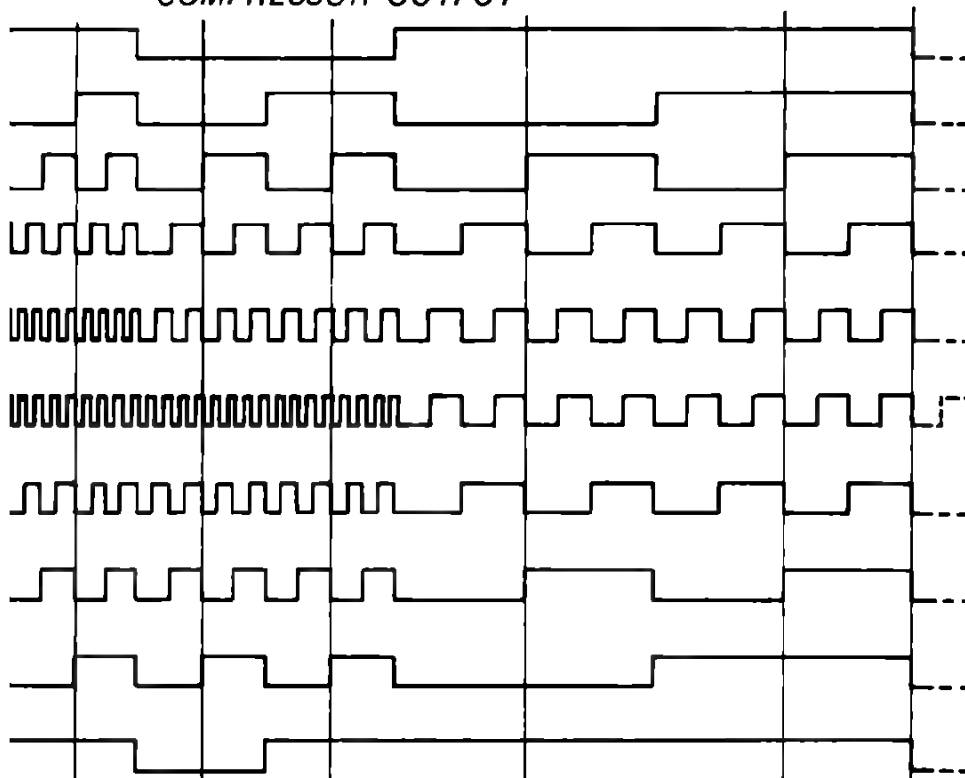
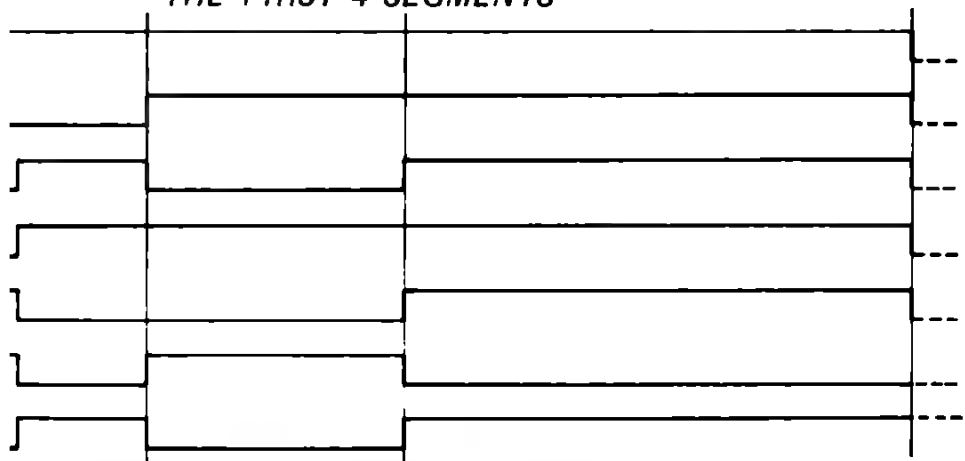


Fig. 22 TIMMING DIAGRAM CORRESPONDING TO THE FIRST 4 SEGMENTS



TIMMING DIAGRAM CORRESPONDING TO THE INTERNAL AND PARTIALLY TRANSMITTED CODE OF TABLE 3

**TRANSFER CHARACTERISTIC
OBTAINED WITH LINEAR RAMP
ON A 12 BIT A-D-C**

Switching time considerations:
Because the variation in time delay, due to the 5 pf or 15 pf i
very important, one can use the values given in the data sh
estimate the maximum propagation delay time of the D.C. I
total propagation delay time is obtained by summing the p
of MC 14532, MC 14539 (A input to output) and MC 14
output). The latter can be estimated as being equal to the ti
input because the number of gates is the same.

		5V		
		typ.	max.	typ.
14532	AL	250ns	375ns	120n
	CL	250	620	120
14539	AL	200	430	90
	CL	200	645	90
14518	AL	200	300	85
	CL	200	400	85

Table 5 PROPAGATION DELAYS

In the worst cases:

5 Volt CL series	$t_p = 620 + 645 + 400 = 1665 \text{ ns}$
5 Volt AL series	$t_p = 375 + 430 + 300 = 1105 \text{ ns}$
10 Volt CL series	$t_p = 300 + 285 + 175 = 760 \text{ ns}$
10 Volt AL series	$t_p = 180 + 190 + 135 = 505 \text{ ns}$
10 Volt AL series, typical	$t_p = 120 + 90 + 85 = 295 \text{ ns}$

3. DIGITAL EXPANDER USING CMOS

In order to recover the original sample value, the receive terminal must have a transfer characteristic which is the reciprocal of the transfer characteristic of the transmit terminal. One can obtain a similar characteristic in a relatively simple manner by using MC 14529 eight channel data selectors and a 12 bit D-A-C plus sign. In P.C.M. systems according to CCITT-recommendations the decoder needs one more bit than the coder. This can be explained by the fact that generally D-A-C's have their full scale equal to $(2^n - 1) \cdot \frac{V_R}{2^n}$, where n is the number of bits and V_R the reference value. Thus, if the output is commutated to obtain a bipolar output, there are not only two different digital inputs for the same analog output (plus and minus zero), but also two LSBs are lost (one for the positive side and one for the negative one). One can avoid this case by switching one $\frac{1}{2}$ LSB into each segment according to the linear code in Table 2. The MC 14529 is preferred for this application because it can act as a bi-directional 8 bit MUX or DEMUX and has a 3 state output (see Fig. 25). The MC 14529 presents the advantage that it can be used to replace the MC 14539 in the compressor since it has a similar truth table as seen below.

	STX	STY	B	A	Z	W
Dual 4-Channel Mode	1	1	0	0	X0	Y0
2 Outputs	1	1	0	1	X1	Y1
	1	1	1	0	X2	Y2
	1	1	1	1	X3	Y3
	1	0	0	0		X0
	1	0	0	1		X1
Single 8-Channel Mode	1	0	1	0		X2
1 Output	1	0	1	1		X3
(Z and W tied together)	0	1	0	0		Y0
	0	1	0	1		Y1
	0	1	1	0		Y2
	0	1	1	1		Y3
X = Don't Care	0	0	X	X		High Impedance

Table 6

digital expander, the MC 14529 is reversed and the input pins 9 and 10 connected together. Thus, it is possible to obtain information characterizing the steps within a segment into eight bits. The D-A-C according to the code given in Table 2. The bits A7, A6, A5 and A4 are directly addressed by A1, A2 and A3. The output Z responds to inputs A, B and ST of the device. The truth table is given on Table 7.

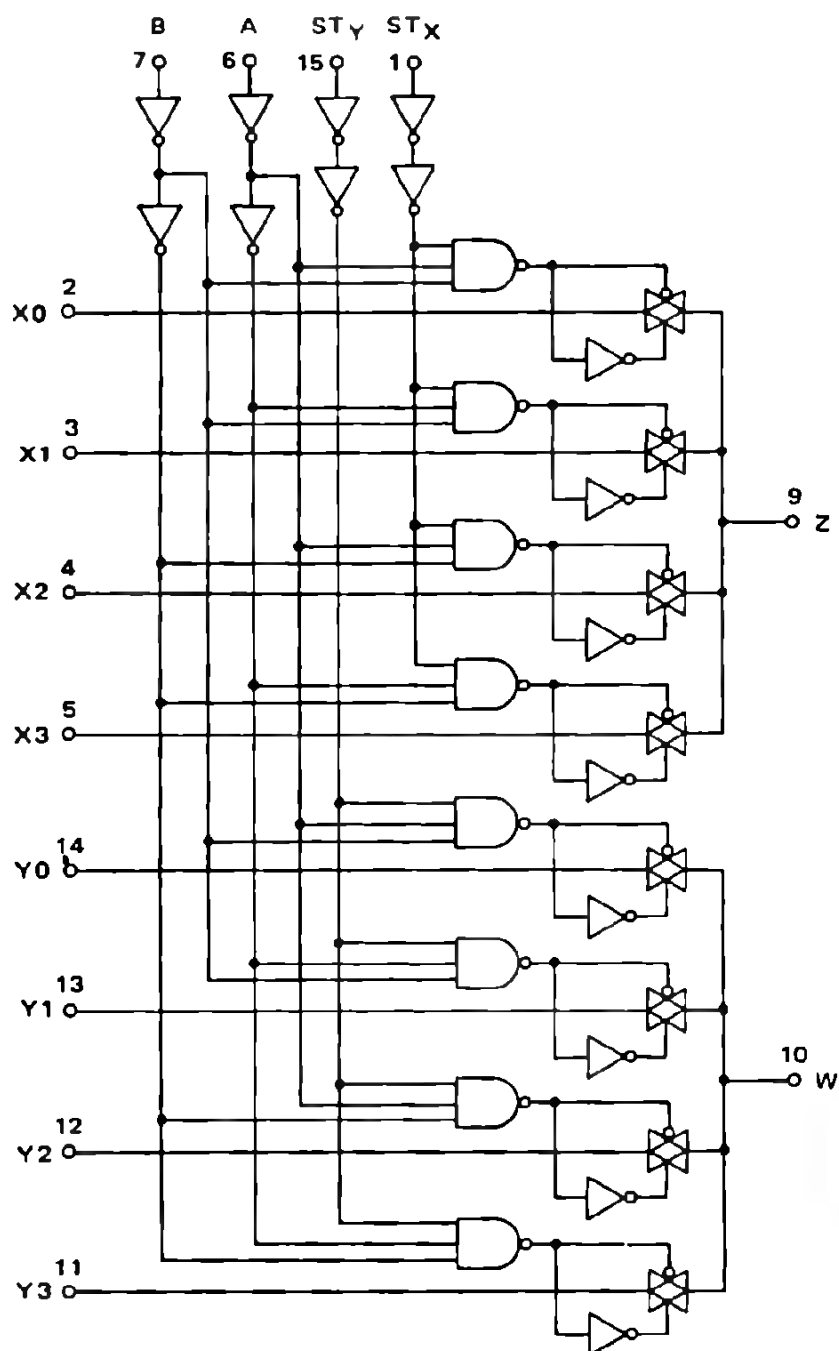


Fig. 25 LOGIC DIAGRAM OF MC14529

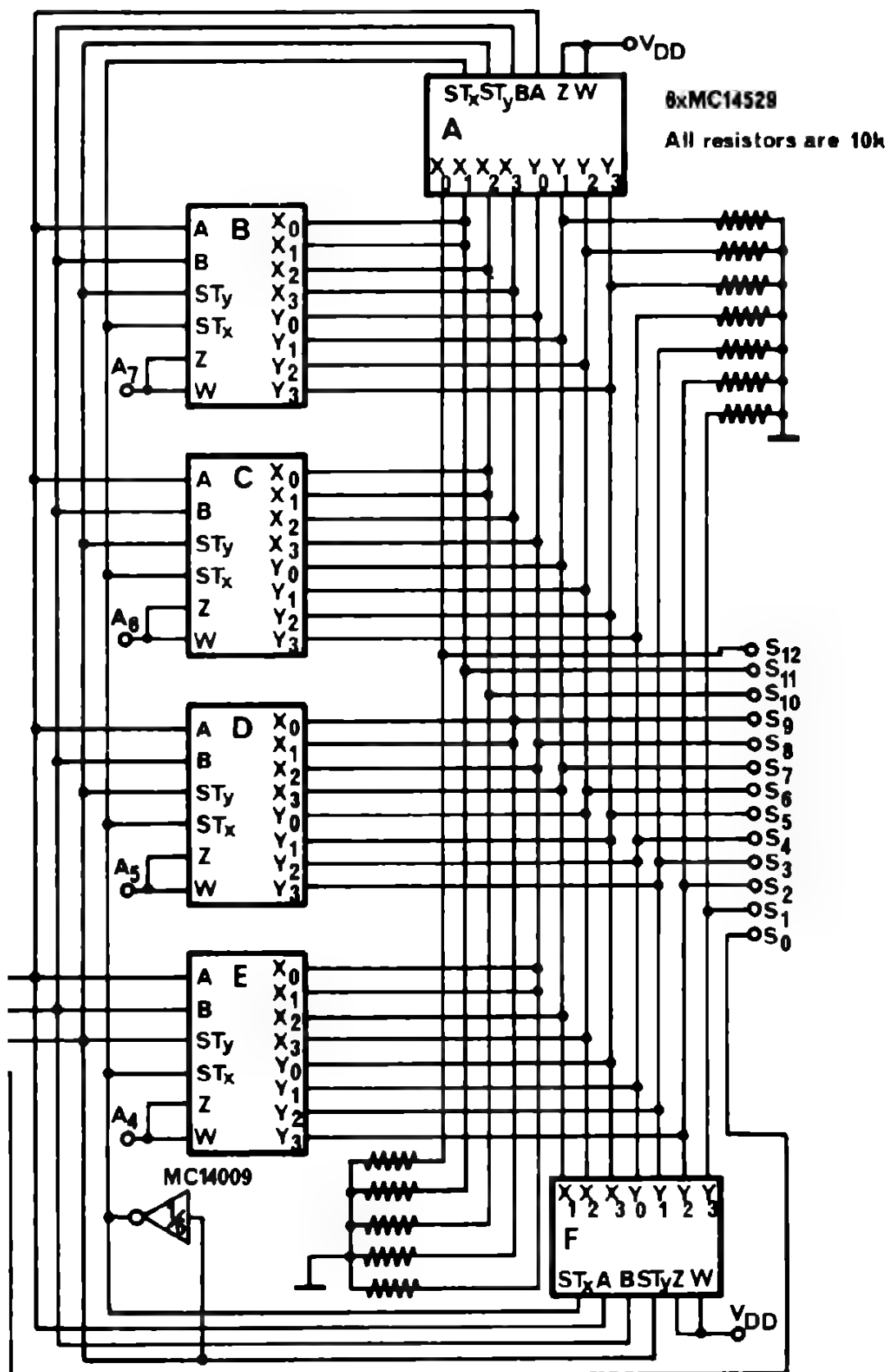
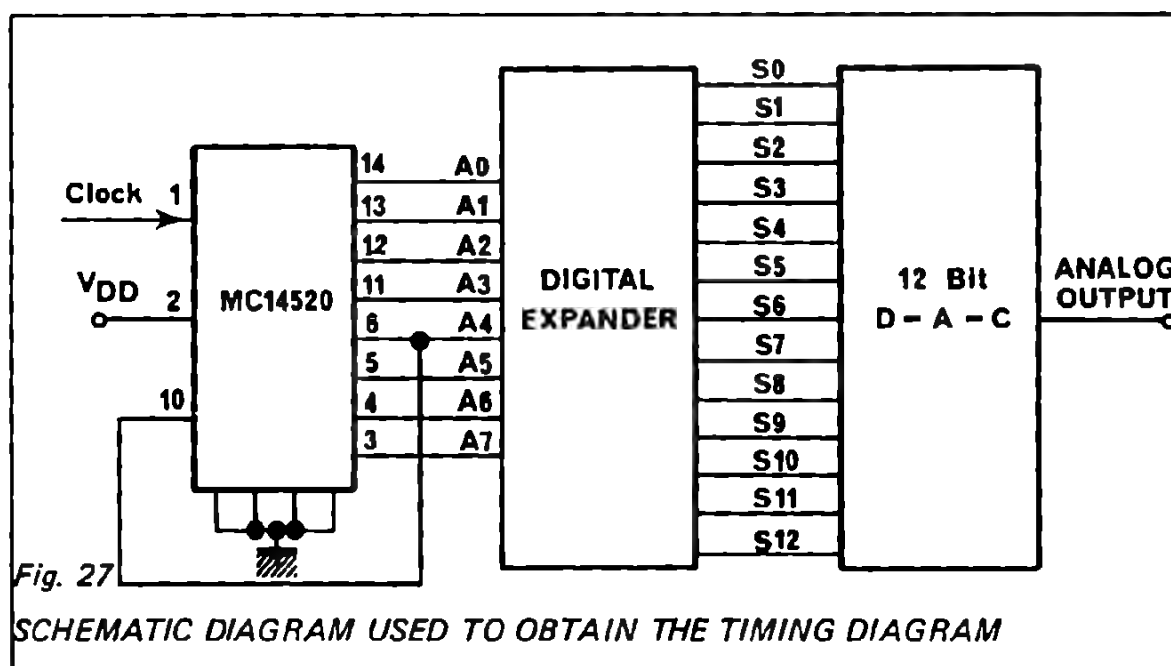


Fig. 26 DIGITAL EXPANDER USING C-MOS

STX	STY	B	A	Out A	Out B	Out C	Out D	Out E	Out F
A1	A1	A2	A3	1	A7	A6	A5	A4	1
1	0	0	0	S12	S11	S10	S9	S8	
1	0	0	1	S12	S11	S10	S9	S8	S7
1	0	1	0	S11	S10	S9	S8	S7	S6
1	0	1	1	S10	S9	S8	S7	S6	S5
0	1	0	0	S9	S8	S7	S6	S5	S4
0	1	0	1	S8	S7	S6	S5	S4	S3
0	1	1	0	S7	S6	S5	S4	S3	S2
0	1	1	1	S6	S5	S4	S3	S2	S1

Table 7 TRUTH TABLE OF THE EXPANDER

With this scheme the non-active outputs are kept at a high impedance since the transmission gates corresponding to these channels are switched off. Therefore, it is necessary to bias these outputs to zero by means of resistors. The value of $10k\Omega$ was selected to avoid long-time constants, and high current consumption.



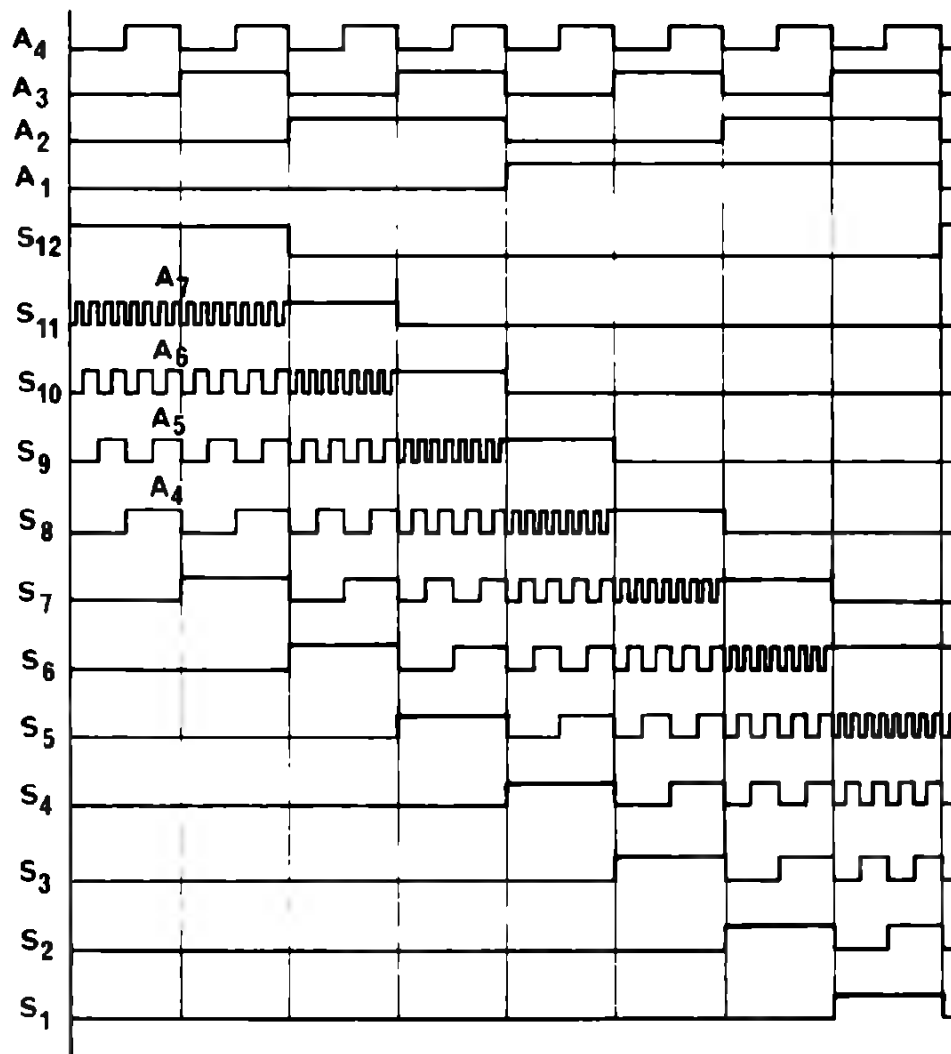


Fig. 28 TIMING DIAGRAM OBTAINED FROM THE SCHEMATIC DIAGRAM OF Fig. 18

The timing diagram of Figure 28 corresponds to the truth table of Table 2. The method using bilateral switches to implement a digital expander can be applied to all devices similar to MC 14529. For this application a low ON resistance is not required since the information transferred is digital.

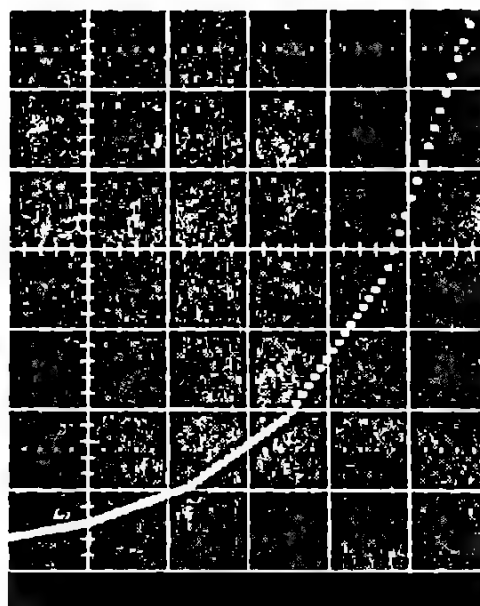


Fig. 30
**TRANSFER
CHARACTERISTIC**

SERIAL-TO-PARALLEL CONVERTER

As seen before, the P.C.M. transmission is made in serial mode. Therefore, to provide the D/A conversion it is necessary to convert the serial format into a parallel one. This operation can be easily performed by using the schematic diagram shown in the Figure 31a.

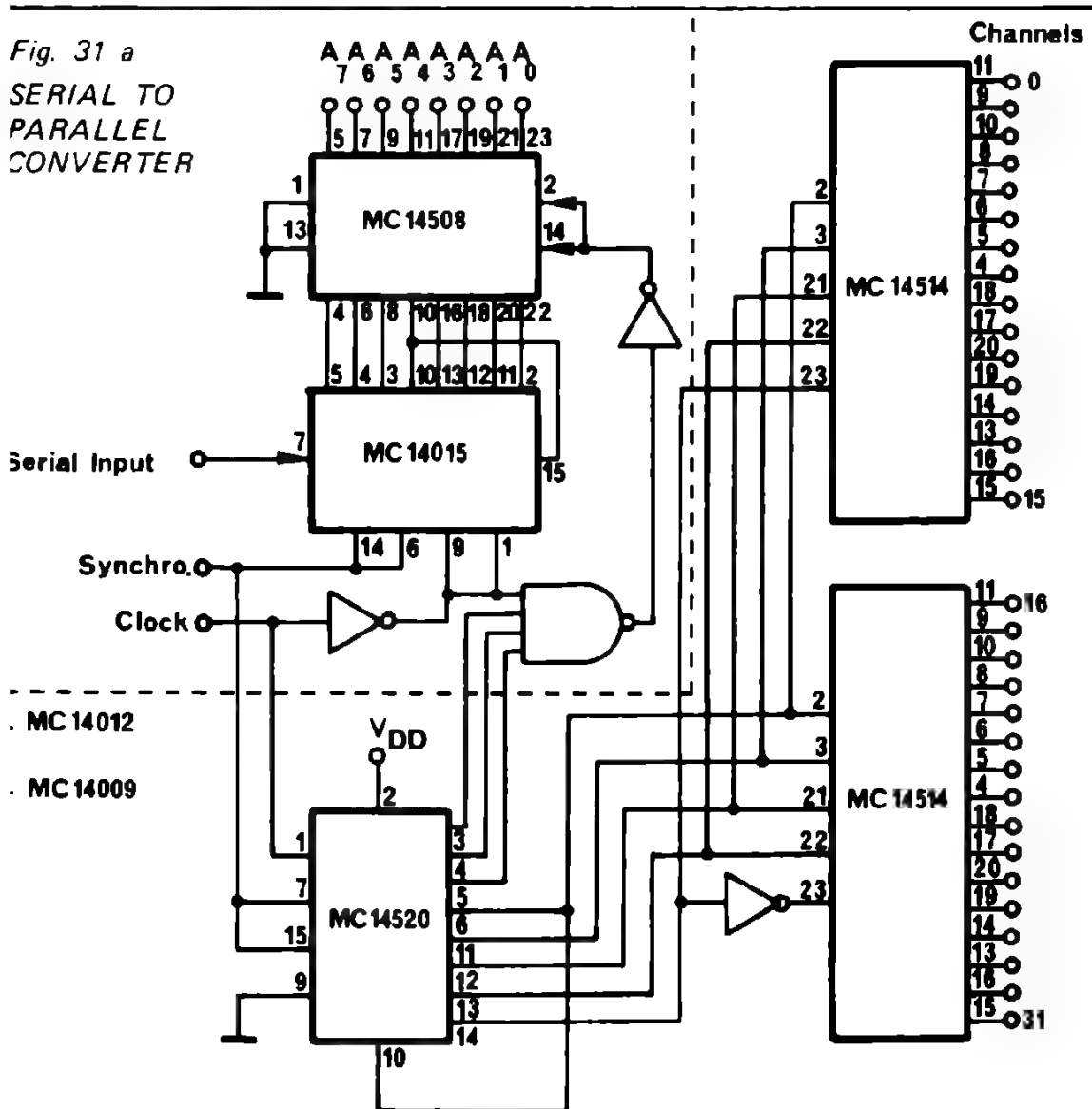


Fig. 31 b CHANNELS DISTRIBUTOR

The serial input comes from the transmission line after code conversion has been made (code conversion consists of translating the transmitting AMI or HDB3 code to a binary NRZ form).

The binary word characterizing each sample of the speech signal consists of 8 bits, each having a duration of 488 ns. This allows $3.91\mu\text{s}$ for the D/A conversion. The MC 14508 dual four-bit latch is used to store the digital information during this

TRUTH TABLE OF MC14508

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	1	1
0	1	0	0	1	0	0	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0
0	1	0	0	1	1	1	0	1	1	1
0	1	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	1	1	0	0	1
0	1	0	0	0	1	0	1	0	1	0
0	1	0	0	0	1	1	1	0	1	1
0	1	0	0	1	0	0	1	1	0	0
0	1	0	0	1	0	1	1	1	0	1
0	1	0	0	1	1	1	1	1	1	1
0	0	0	X	X	X	X	Latched			
1	X	0	0	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

Table 8

time. Outputs Q0A, Q1A, Q2A of the MC 14520 "anded" with the clock pulse, control the MC 14508 to transfer or latch its input information (see Fig. 32). The truth table above shows that the information is transferred when a "1" is applied to the strobe input and latched when the strobe is zero.

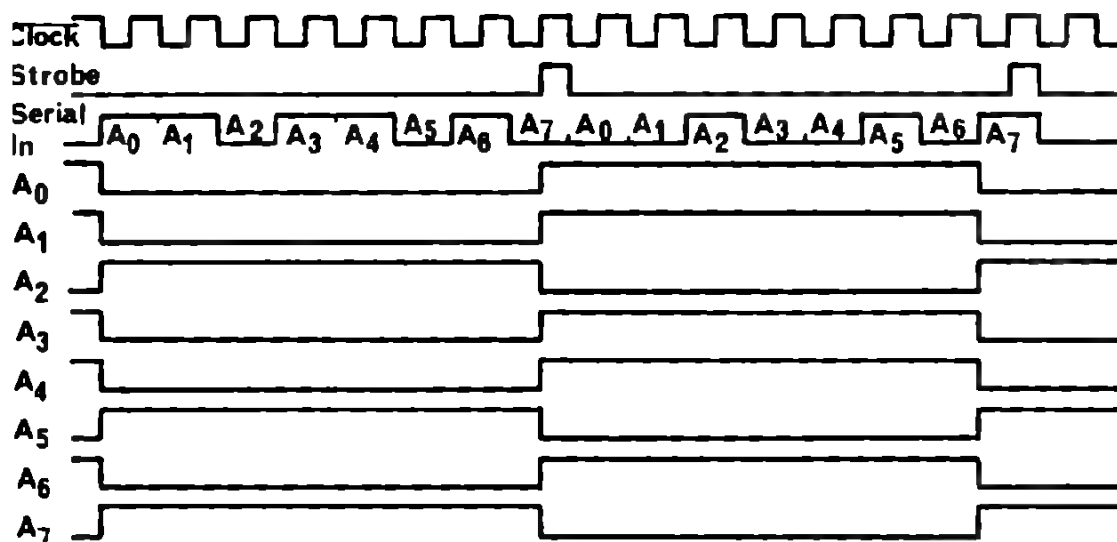


Fig. 32 TIMING DIAGRAM OF SERIAL TO PARALLEL CONVERTER

The timing diagram shows the operation of the serial-to-parallel converter when two complementary binary words are applied successively to its serial input. The part of the schematic diagram below the dashed separation line shows an example of an application of the MC 14514 4-bit latch/4 to 16 decoder as a driver for the multiplexer (see Fig. 31b).

5. CONCLUSIONS

These few examples show the wide field of the application of CMOS in P.C.M. systems because of the large variety of complex functions available. There are many applications in the field of signalling and also the multiplexing and de-multiplexing of analog or digital values.

One other advantage of using CMOS instead of TTL here for accurate D-A-C or A-D-C systems is that any transients on the ground or on the power supply line are not so large.

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C DATA TRANSMISSION

FREQUENCY GENERATOR FOR LOW-SPEED MODEMS USING CMOS COMPLEX FUNCTIONS (CCITT*-RECOMMENDATION V-21)

CMOS technology provides some interesting intrinsic characteristics, like high noise immunity and low power consumption, that definitely offer advantages for the realization of data transmission equipment.

Similarly, complex functions available in CMOS, like the data routing functions MC 14512/519, the BCD rate multiplier MC 14527 or the dual 4-channel data selector MC 14529, will help the circuit designer in finding attractive solutions with a reduced number of packages.

The example that will be handled here, represents part of a MODEM, whose general configuration is shown in Figure 33.

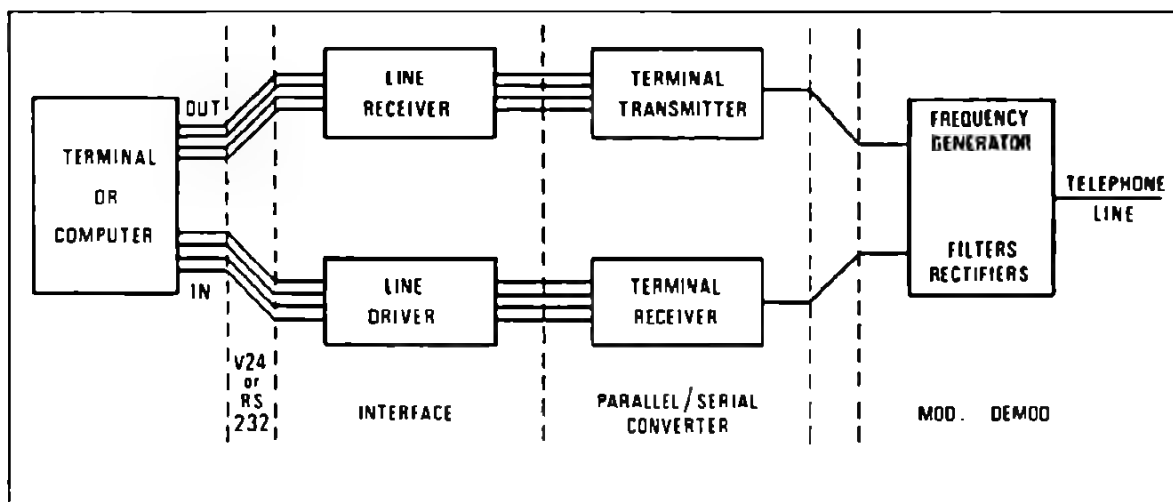


Fig. 33 MODEM

The type of MODEM considered corresponds to the CCITT-Recommendation V-21. This Recommendation applies to circuits operated at a maximum modulation rate of 200 bits/sec in a full duplex transmission mode.

The frequencies used for the forward channel are 980 Hz (mark sign or logic one) and 1180 Hz (space sign or logic zero). Those used for the backward channel are 1650 Hz (mark) and 1850 Hz (space).

* International Telegraph and Telephone Consultative Committee in Geneva.

The circuit described below is a generator delivering the four specified frequencies, synthesised from a 455 kHz ceramic filter oscillator. The reference frequency has been chosen below 1 MHz in order to keep the power dissipation as low as possible. However, the frequency stability versus temperature has not been verified for this case. If this should not be satisfactory, the circuit need be only slightly modified to be adapted to a reference frequency such as a crystal oscillator.

The digital generation of a sinewave requires the use of D-A-Converters and the harmonic content of such a wave depends on the number of amplitude steps chosen. The digital generation of a sinewave can be implemented either by regularly dividing its period and using variable amplitude steps, or using equal amplitude steps having variable duration. The first method, with a seven-step approximation, has been selected for this application.

Figure 34 shows the block diagram of the complete circuit which consists of

- 1) a variable divider, providing the four quotients;
- 2) the pattern generator, giving the digital value of the amplitude according to the proper position within the period;
- 3) the digital-to-analog converter and
- 4) a zero crossing detector, which allows the mark/space commutation only when the signal crosses the zero axis.

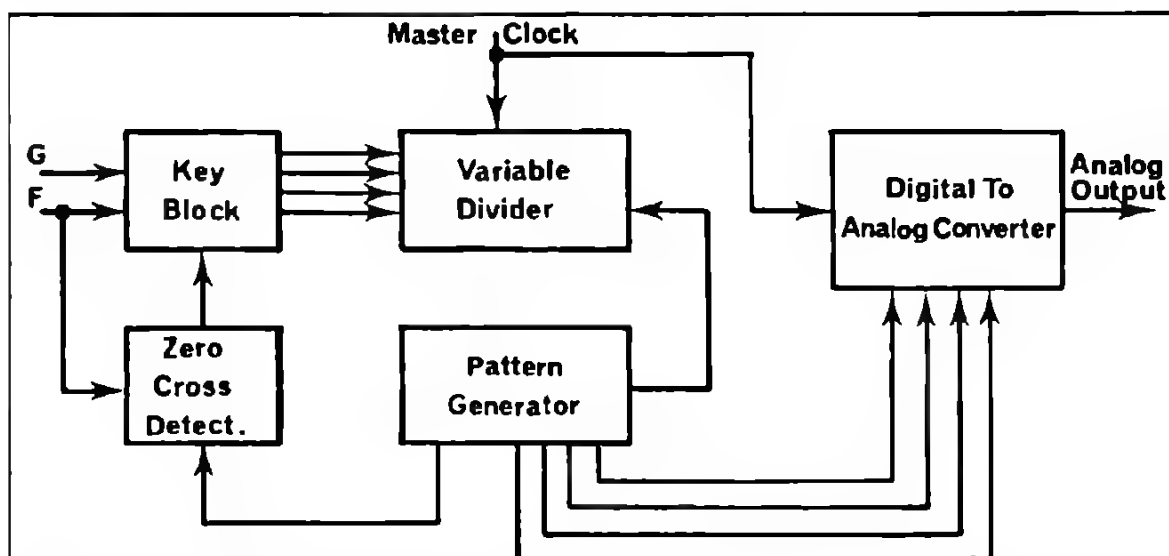


Fig. 34 BLOCK DIAGRAM OF THE FREQUENCY GENERATOR

F = Mark/Space

G = Channel selection

1. VARIABLE DIVIDER

This circuit provides the variable divide ratio, Q , required for the generation of each frequency. As it can be seen in Figure 35, the period of the original signal must be divided by 12 when using a seven-step approximation. This means:

$$f_{\text{out}} = \frac{455 \text{ kHz}}{12 \cdot Q}$$

In addition, it is not possible to reach the accuracy required ($\pm 6\text{Hz}$, according to CCITT-recommendation V-21) when dividing the reference frequency with Q integer. Therefore, a correction network will modify the cycle of the variable divider to obtain a fractional number. Indeed, if the divider required is 38,5, such a number can be implemented when dividing successively by 38 and 39. This operation is obtained by feeding the MC 14516 Q_1 output (pattern generator) back to the least significant digit of the programmable counter (variable divider) (Fig. 39). The variation in duration of the steps thus obtained has only a slight effect on the spectrum of the resulting waveform.

f required	f _{out}	Quotient	Absolute error	Relative error %	12 x f _{out}
910	972,2	39	9,8	0,493	11818,1
	984,8	38,5	4,8		
	998	38	18		
1180	1184,8	32	4,8	0,41	14218,8
1650	1648,6	23	1,4	0,088	19782,6
1850	1805,6	21	44,4	0,022	22195,1
	1849,6	20,5	0,4		
	1895,8	20	45,8		

Table 9

Two cascaded MC 14522 or 14526 (Fig. 39) are used to build the variable divider. Their input truth table is given below.

G	F	Frequency	Quotient	Dp4A	Dp3A	Dp2A	Dp1A	Dp4B	Dp3B	Dp2B	Dp1B
1	0	1180	32	0	0	1	1	0	0	1	0
1	1	980	38,5	0	0	1	1	1	0	0	1/0
0	0	1850	20,5	0	0	1	0	0	0	0	1/0
0	1	1650	23	0	0	1	0	0	0	1	1

F = Mark/space

G = Channel selection

Table 10 TRUTH TABLE OF THE VARIABLE DIVIDER

Note that, using this technique, it is possible, by programming the MC 14522 or the MC 14526 inputs, to divide the master clock by 1 to 99 or by 1 to 255 respectively with increments of 0.5.

2. PATTERN GENERATOR

As shown below a seven-step approximation implies that the signal period is divided by 12. Several methods, using shift registers and resistors or gates, allow one to implement a modulo 12 divider to synthesize a sinewave. Another solution, preferred here, which avoids resistors, uses the MC 14516 up/down counter (Fig. 39) having a cycle of 6.

Note that it is very easy to shift in phase the signal by initializing the MC 14516 on the PE input after having applied proper addresses to P_1 thru P_4 inputs.

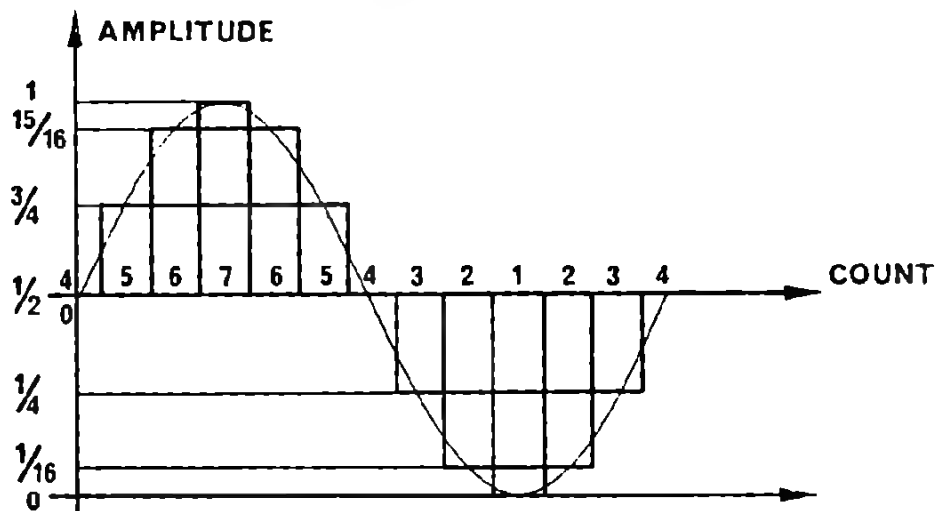


Fig. 35 SINEWAVE APPROXIMATION BY A 7-STEPS FUNCTION

The D-FF (1) (Fig. 39) is needed to provide the up/down count according to the timing diagram of Figure 36. It is necessary to delay the MC 14516 clock input because the up/down input must be pulsed before the incrementation of the count.

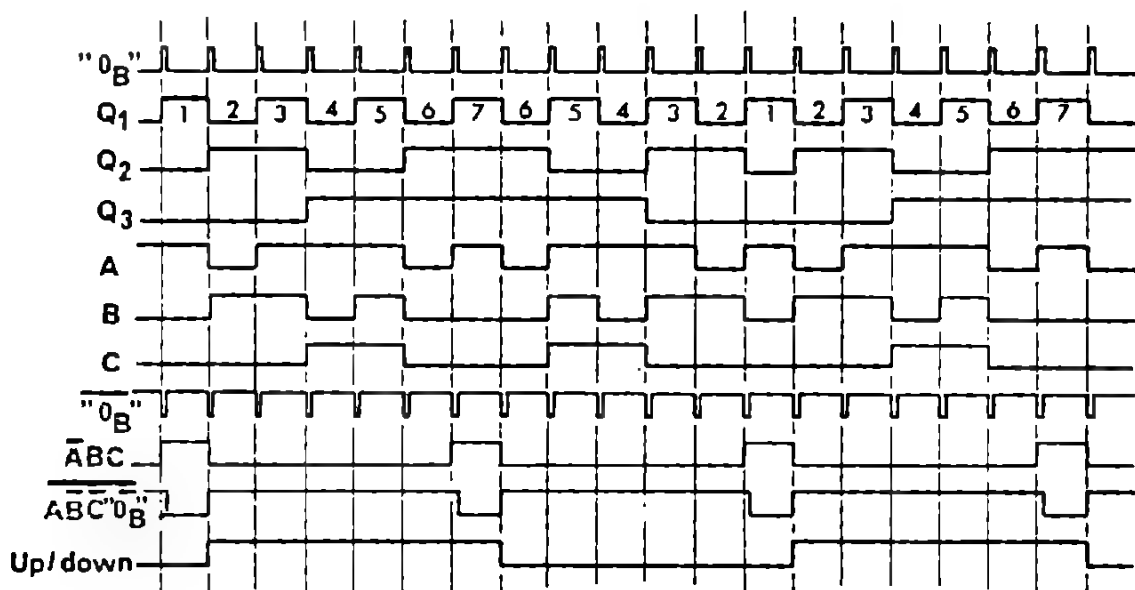


Fig. 36 TIMING DIAGRAM OF THE PATTERN GENERATOR

"O_B" : MC 14522 B output
 Q₁, Q₂, Q₃ : MC 14516 outputs
 A, B, C, D : MC 14527 BCD outputs
 ABC "O_B" : D-FF1 clock

In order to obtain the proper digital amplitude of the steps at the D-A converter input, it is necessary to make a code conversion of the MC 14516 Q_X outputs. This operation is performed by some NAND gates and inverters according to Table 11.

COUNT	SINE VALUES	BCD RATE MULTIPLIER					MC 14516			
		Output	D	C	B	A	Q ₃	Q ₂	Q ₁	up/down
1	0	1/10	0	0	0	1	0	0	1	1
2	1/16	2/10	0	0	1	0	0	1	0	1
3	1/4	3/10	0	0	1	1	0	1	1	1
4	1/2	5/10	0	1	0	1	1	0	0	1
5	3/4	7/10	0	1	1	1	1	0	1	1
6	15/16	8/10	1	0	0	0	1	1	0	1
7	1	9/10	1	0	0	1	1	1	1	1
6	15/16	8/10	1	0	0	0	1	1	0	0
5	3/4	7/10	0	1	1	1	1	0	1	0
4	1/2	5/10	0	1	0	1	1	0	0	0
3	1/4	3/10	0	0	1	1	0	1	1	0
2	1/16	2/10	0	0	1	0	0	1	0	0

Table 11 TRUTH TABLE OF THE SINEWAVE GENERATOR

3. D-A CONVERTER

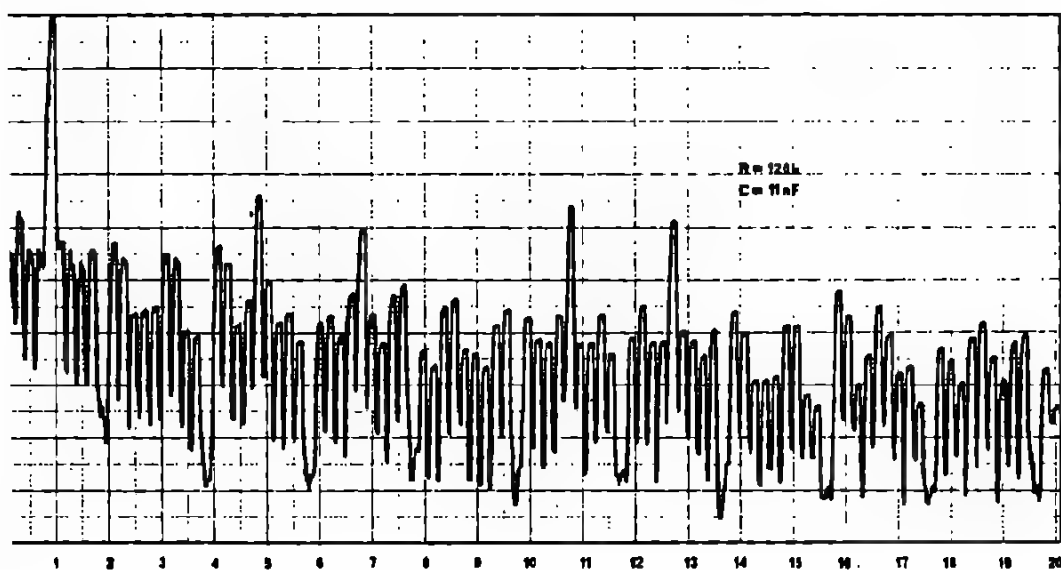
A simple way to achieve this conversion is to use an MC 14527, BCD rate multiplier. This integrated circuit will yield an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number there will be

output pulses for every 10 input pulses. Therefore, if the BCD inputs are jammed in such a way that each count of the up/down counter produces the closest sine value at the right time, the output of the BCD rate multiplier will be a sequence corresponding to this value. In the schematic diagram of Figure 39, the input clock pulse to the MC 14527 is the 455 kHz reference frequency while the number of pulse trains (given by ABCD inputs) is controlled by the MC 14516 pattern generator.

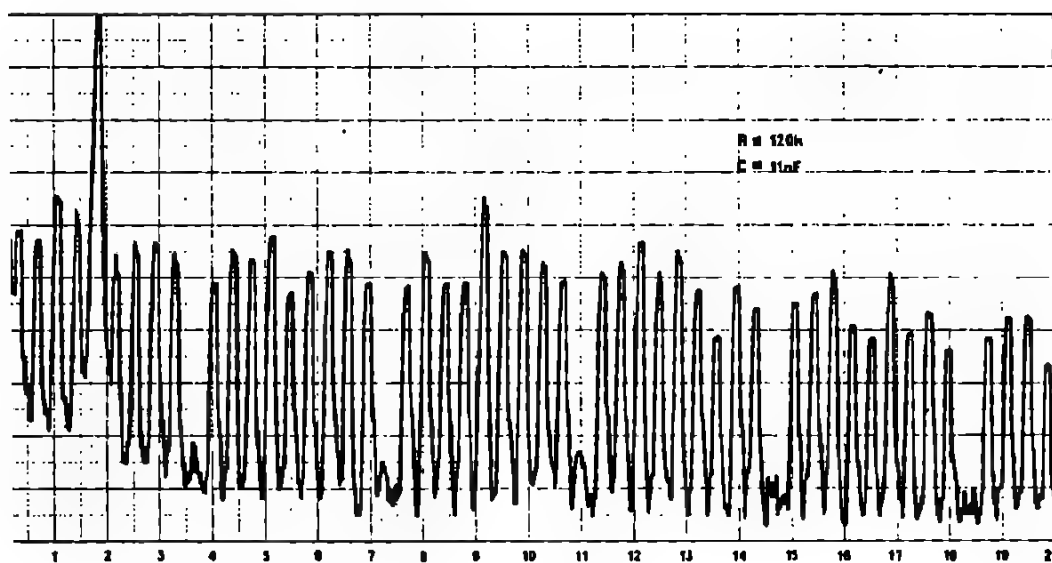
A seven-steps approximation to the sinewave can be seen by connecting an oscilloscope at the output of the MC 14527.

That, for other applications, it is possible to increase the accuracy of the conversion by cascading more MC 14527s.

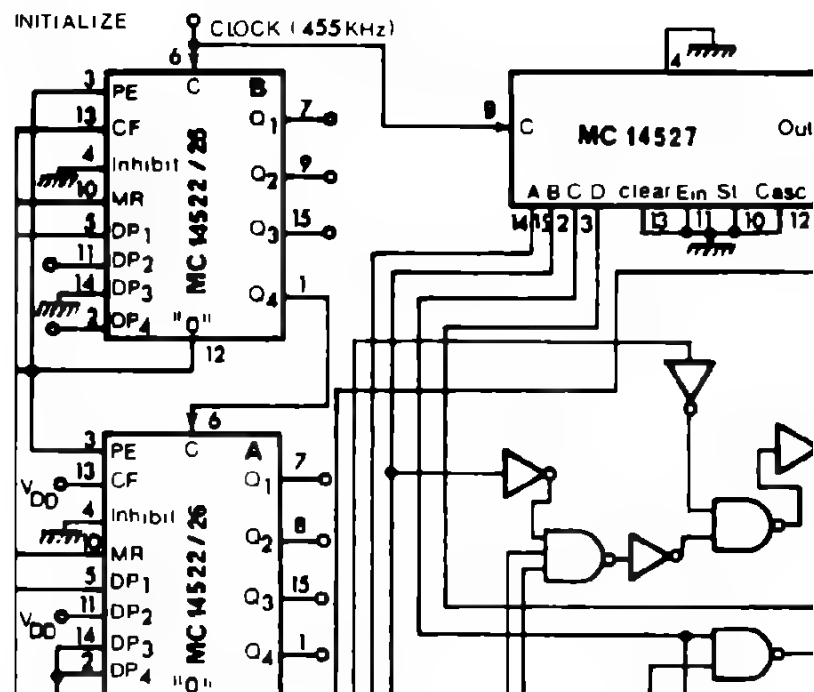
Figures 37 and 38 show the spectra obtained with the circuit of Figure 39 at the lowest (980Hz) and the highest (1850Hz) frequency.



37 SPECTRUM AT 980Hz



38 SPECTRUM AT 1850Hz



4. ZERO CROSSING DETECTOR

Since the waveform is generated digitally, it is very easy to obtain this function by decoding the corresponding digital output of the pattern generator. The information of MARK or SPACE is introduced on the D input of the D-FF (2) (Fig. 39) and it is clocked by the proper pattern generator output.

5. CONCLUSIONS

The described application of the frequency generator for MODEMs using CMOS complex functions can be developed to implement a very low speed waveform generator, having a wide range of frequencies and higher accuracy by cascading MC 14527 BCD rate multipliers.

The method using variable feedback divider should be used whenever it is not possible to reach the proper frequency by dividing a low clock frequency by an integer.

The field of application of CMOS complex functions is very large and, in many cases, it is possible to reduce the complexity of a circuit by using them.

Industrial Applications

1. LOW POWER D/A CONVERTERS
2. SUCCESSIVE APPROXIMATION
A/D CONVERTER
3. DUAL RAMP A/D CONVERTER

1. CMOS DECODER-DRIVERS
2. MULTIPLEXED DISPLAYS

1. INTRODUCTION
2. DISCUSSION OF DESIGN
PROCEDURE
3. A SPECIFIC APPLICATION
4. ACCURACY CONSIDERATIONS

1. INTRODUCTION
2. MAXIMAL LENGTH SEQUENCES
3. APPLICATIONS
4. CONCLUSIONS

1. A PERSONALIZED HEART RATE
MONITOR WITH DIGITAL
READOUT
2. A DIGITAL CLINICAL THERMO-
METER USING CMOS

A. INTRODUCTION

Other chapters of this book have described numerous characteristics of the MOTOROLA CMOS logic family in considerable detail. In this chapter those characteristics which are especially beneficial in industrial electronic applications will be singled out. To illustrate the various features of CMOS, a few representative circuits will be presented. A significant feature of CMOS is the high noise immunity, especially at a power supply level of 15-18 volts. Since the industrial environment is known to be often very noisy, CMOS is ideally suited for use in industrial electronic equipment. In addition to this high noise immunity, the tolerance to power supply voltage variations and power supply line impedance is very large. The consequences are that less system design time is usually needed and that the total system costs are decreased.

Another major characteristic of CMOS is its extremely low power consumption. Therefore, the CMOS family offers excellent opportunities for the design of self-contained, battery powered equipment. These equipments are becoming more and more widespread in use because of their independency of the line supply, which not only reduces the systems cost but also the risk of electrical hazard. This is extremely important in medical electronic equipment, where even a very small current may present a hazard to the patient.

The very high input impedance of CMOS combined with a fairly low output impedance offers an almost unlimited fanout. This feature can in turn reduce the number of parts used for a system as well as its complexity, contributing to higher system reliability and reduced cost.

The tri-state output of CMOS devices can be looked on as an equivalent of the open-collector feature of bipolar logic circuits but offering many more possibilities. The tri-state output not only provides a very high output impedance state, but also a low output impedance, in either the high or low logic state, depending on whether the output transmission gate is open or closed.

This feature offers the design engineer a very real additional degree of freedom.

In addition to the electrical properties of complementary MOS, the MOTOROLA family features an extremely well coordinated set of parts, thoroughly compatible with each other, with many special LSI functions.

Examples occur not only in the various arithmetic functions but also in circuits such as the A/D converter parts described later.

B D/A AND A/D CONVERTERS

1. D/A CONVERTERS FEATURING LOW POWER CONSUMPTION

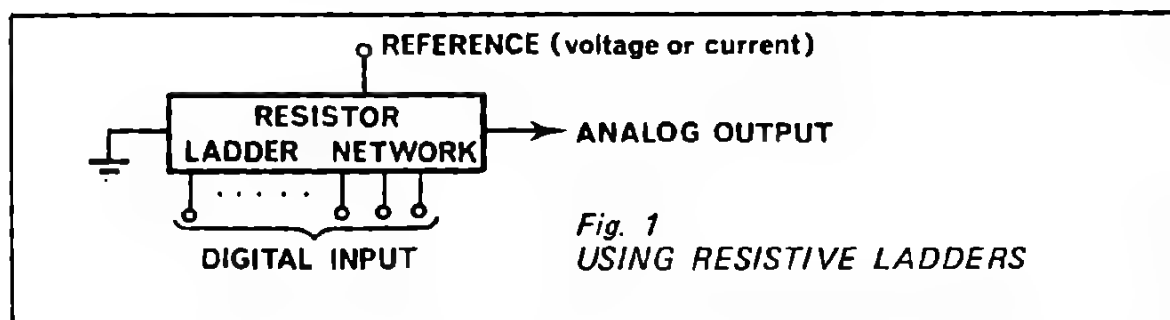
1. 1. INTRODUCTION

As the interest in small battery powered instruments continues, slowly the battle for lower power consumption (and hence improved battery lifetime) is being won.

Logic circuits may be implemented in CMOS (e.g. MC 14xxx series), analog circuits may be designed using micropower operational amplifiers (e.g. MC 1776) as the active elements and shortly, liquid crystals will be available to take over the function of visual displays. A typical instrument may require only microwatts for each section; however, in practice, the interfaces between any digital circuit and an analog one may consume a lot of current; of the order of milliwatts. It seems timely then to examine the D/A converter from the viewpoint of power consumption.

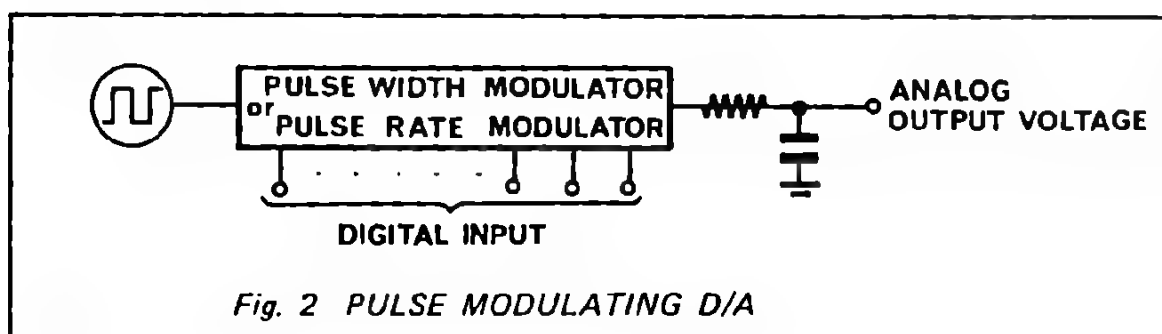
1. 2. BASIC TECHNIQUES OF D/A CONVERSION

The D/A converters to be considered here all fall into one of two major groups. The first and most widely employed group, illustrated by Figure 1, uses the digital input levels to activate switches, thereby altering the connections to a resistor ladder network and producing a voltage or current at the network output terminals corresponding to the digital input word.



The second group of D/As, seen in Figure 2, use digital circuitry to generate a train of equal amplitude pulses of constant frequency, whose duty cycle is proportional to the digital number or, alternatively, a train of equal pulses whose time density has the desired analog relationship to the digital input. Either of these methods, using variable width pulses or variable density pulses will, after suitable smoothing, produce the desired d.c. analog output corresponding to the digital input word. As a class, these converters tend to be slow because the counters can accept only limited frequencies and several cycles of a wave-shape made up of many clock pulses must be integrated to provide a smooth analog voltage.

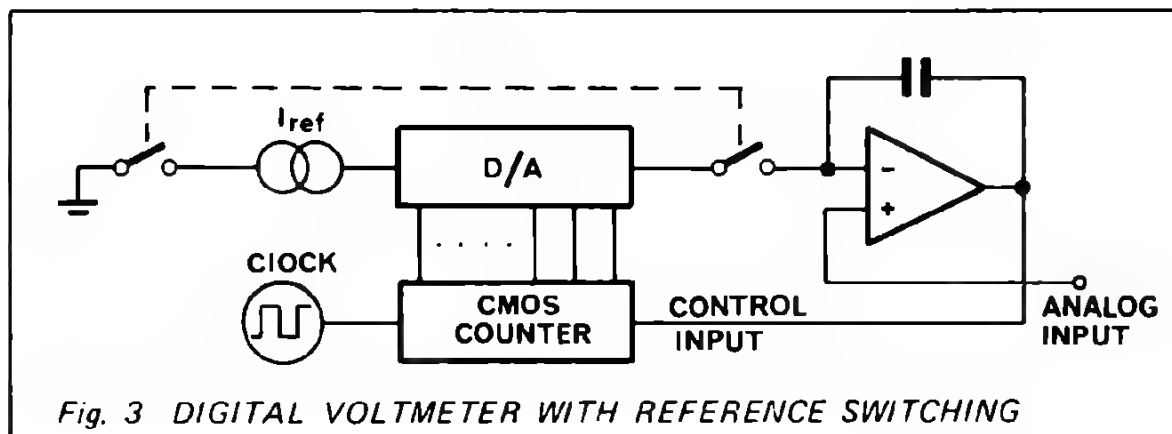
These systems will now be considered in more detail, especially regarding the power consumption.



Current switching resistive ladder network:

This is probably the most popular form of D/A, using the resistor network to sum currents; it has a fast response time and, owing to the low values of resistance required in the ladder, is suitable for implementation in microcircuit form with thin film resistors. A typical example of a complete monolithic D/A is the MC 1508. This device may be driven by CMOS logic elements and the analog output current follows within 500 ns of a logic input change. The reference current to be switched must, of course, come from the power supplies and hence constitutes an additional power drain. While this can often be as little as 100 microamps per decade, the MC 1508 integrated circuit specification is not guaranteed with less than 500 microamps reference current. If this amount of current is objectionable, it is possible to switch the reference current off and subsequently on again, re-establishing the analog voltage output within 500 ns.

Thus, careful circuit design, where the D/A is switched on only when required, can result in appreciable power savings. For example, the digital voltmeter of Figure 3, in which the display needs to be up-dated only at the speed of response of the eye, could use a D/A which is switched off for the majority of the time. This could bring the average power consumption of the D/A down below that of the other digital and analog circuits.



Voltage switching resistive ladder network:

This technique, illustrated in Figure 4, switches a precise voltage source on to various nodes of a resistive ladder divider as directed by the digital input. Apart from the different voltage reference that is needed, the major difference between this and the current switching system is in the resistors used. Here, high resistance values are required to reduce the power consumption, and this immediately causes problems of decreased switching speed and increased cost of the resistive network. For example, switching may take typically several microseconds, whilst the ladder network has to be constructed using thick film technology or even with discrete resistors, involving further difficulties owing to temperature drift of the resistors. Nevertheless, this D/A technique is attractive owing to its simplicity, since it does not require switching off the reference signal in order to have minimum power consumption. Also both its high impedance levels and slower speeds make it an ideal candidate for CMOS logic.

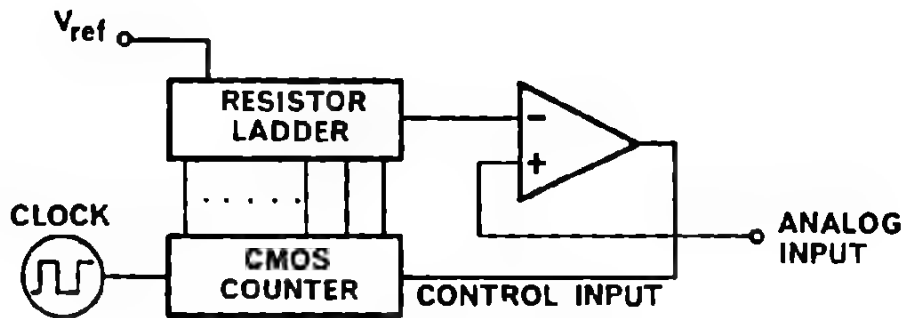


Fig. 4 A/D WITH VOLTAGE REFERENCE

Variable mark/space ratio rectangular wave:

The circuit of Figure 5 is the first converter of the second group mentioned above which we are considering. It produces a rectangular waveshape whose duty cycle is proportional to the digital number input. This rectangular wave is generated digitally by using two equal length counters to set and reset a flip-flop.

The duty cycle of the flip-flop is altered by adding extra counts into one or the other counter, or "phase shifting" the counters. The resolution in changing the duty cycle depends on the length of the counters themselves, whilst the period of the rectangular wave is fixed by the clock rate and counter length. To obtain the analog output voltage, an integrator is connected to the flip-flop output. This circuit becomes quite complex if provision is made to adjust the 'phase difference' between counters without having to wait until one or the other has reset itself. The power consumption of this circuit will probably be very low, resulting mostly from the CMOS elements. The only other power consuming device is the integrator, which can be made with a micropower op-amp if additional gain is necessary. Current drain of the CMOS can be kept low by running it at the minimum speed necessary for the application, since it draws current primarily during transitions.

Variable mark/space ratio using up/down counters:

Figure 6 shows this converter to be very similar to the previous one except that a single up/down counter is used instead of two up-counters. The counter is preset to the desired digital input number and alternately counts up or down from this number to the counter zero state. A high output is obtained while the counter is counting down, a low while it is counting up; so preset, upcount, reset and downcount produces one complete rectangular waveshape cycle. The

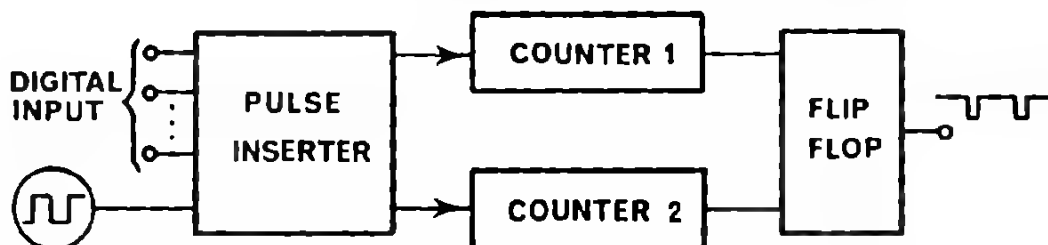
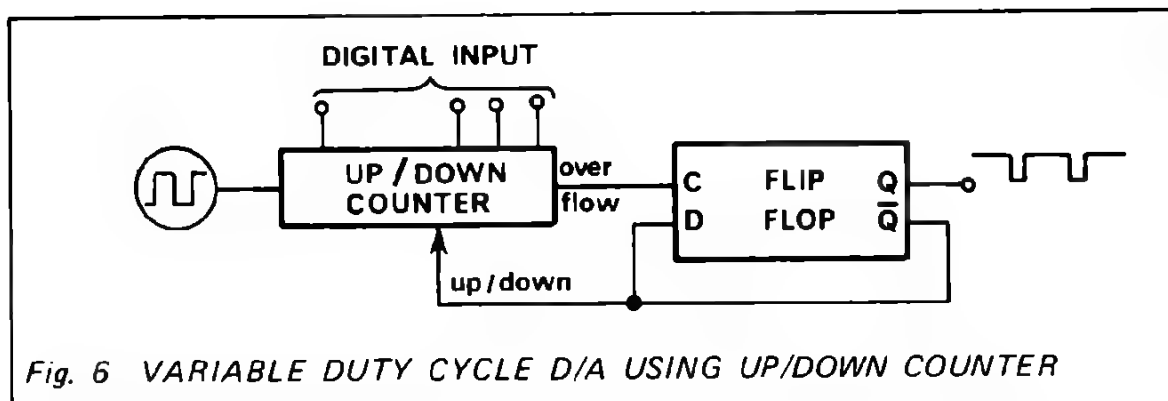


Fig. 5 VARIABLE DUTY CYCLE D/A USING TWO COUNTERS

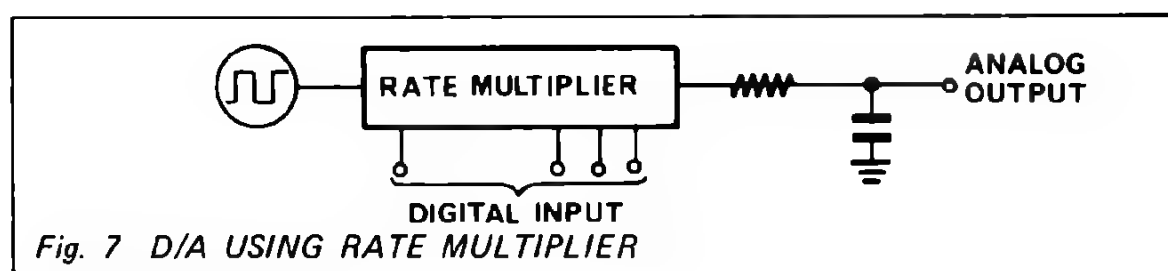


high-low output is the required duty cycle modulated a.c. signal. It is subsequently integrated, as before, to supply the analog output voltage.

This converter, like the previous one, uses CMOS entirely except for the integrator, so the power consumption considerations are similar. It is intermediate in complexity between the previously and subsequently described digital techniques.

Variable pulse rate converter:

The converter of Figure 7 is somewhat similar to the previous two except it operates by removing some of the pulses of a continuous stream to provide numbers less than full scale. A rate multiplier circuit such as the MC 14527 generates the modulated pulse stream and an integrator converts it to an analog level. Since the counter in the rate multiplier runs continuously, there is no problem of resetting, as in the case of the dual counter system described previously. Of the low power D/A converter techniques considered here, this is the simplest and easiest to make work and, as with the previous two, its accuracy is dependent primarily on the analog integrator. Since the rate multiplier is a CMOS part, its power consumption is also dependent on operating speed and, in addition, the integrator may require slightly more current with higher operating speeds.



1. 3. CONCLUSIONS

Of the low power D/A conversion techniques examined here, two appear to have the most promise: the current switch exemplified by the MC 1508 with CMOS driving circuits, and the rate multiplier exemplified by the MC 14527. The first is more commonly used, probably because it is better known, but the latter, although slower, has the potential of being considerably less power consuming.

2. SUCCESSIVE APPROXIMATION TYPE DIGITAL-TO-ANALOG CONVERTER

2. 1. PRINCIPLE OF OPERATION

In analog to digital conversion by the method of successive approximation, the analog voltage is compared with the output of a digital-to-analog converter (DAC), connected in a feedback loop as shown in Figure 8. The digital input word presented to the DAC is identical to the digital output word of the analog-to-digital converter (ADC).

The operating sequence of the converter is the following: the most significant bit of the DAC is first presented to the comparator. If the comparator output remains high, the bit is memorized, if it goes low, the bit is erased. This same operation is repeated for each bit and the conversion cycle thus ends with the least significant bit.

The whole converter circuit consists of a DAC, an operational amplifier, a voltage comparator and the digital circuitry that controls the above described conversion cycle. These logic circuits, called the successive approximation register (SAR) have been realised on one single CMOS chip which will now be considered in more detail.

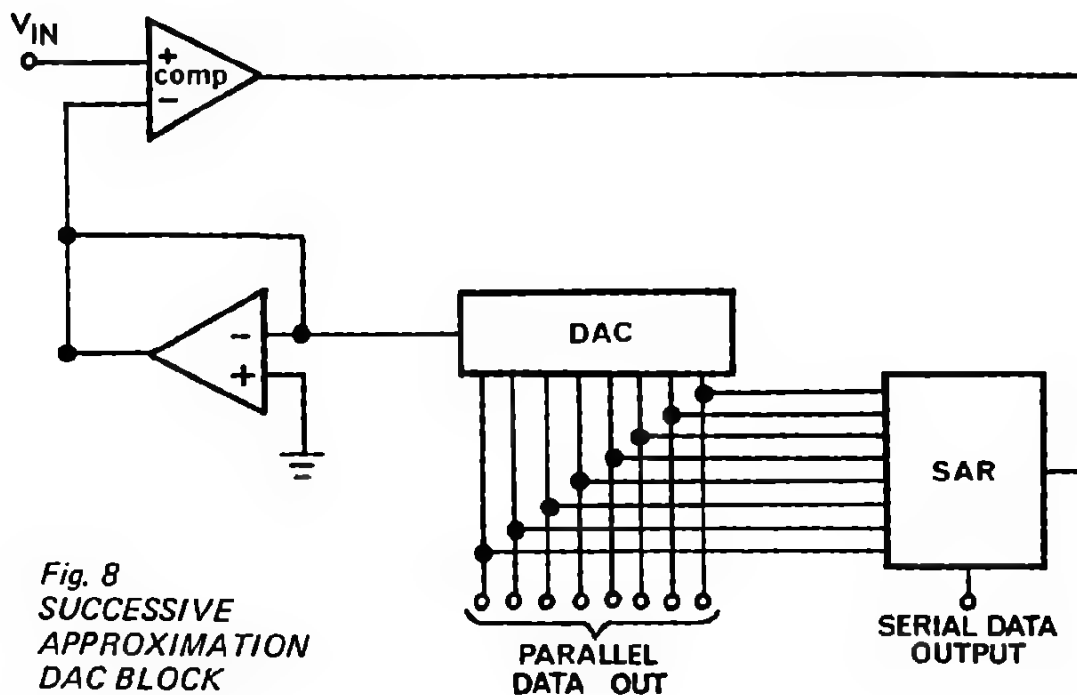


Fig. 8
SUCCESSIVE
APPROXIMATION
DAC BLOCK
DIAGRAM

2. 2. RESETTABLE SAR MC 14559

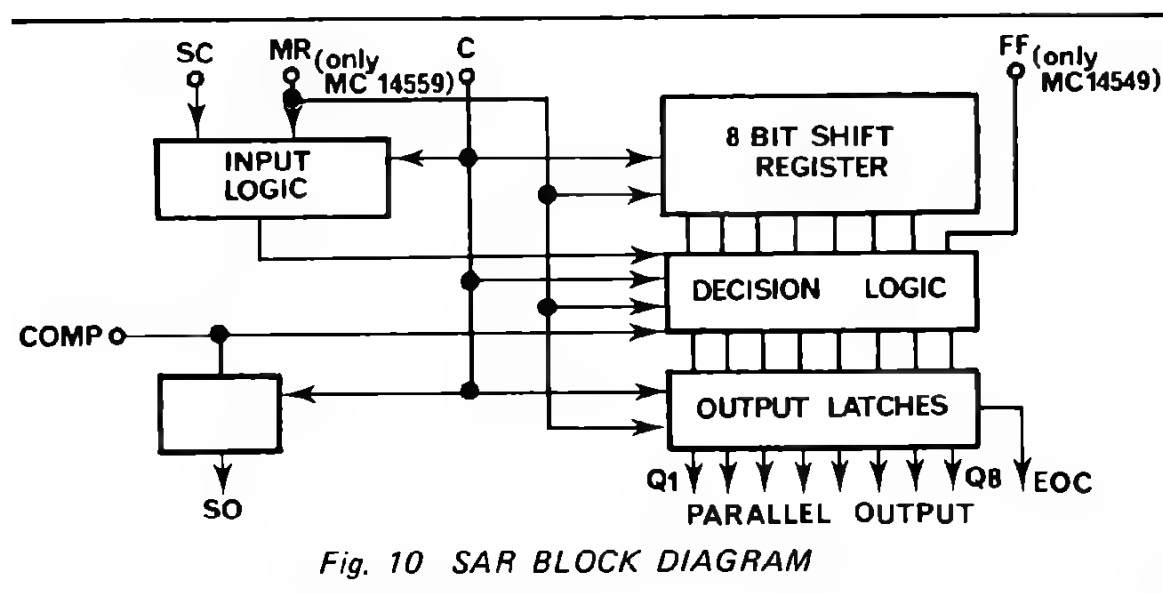
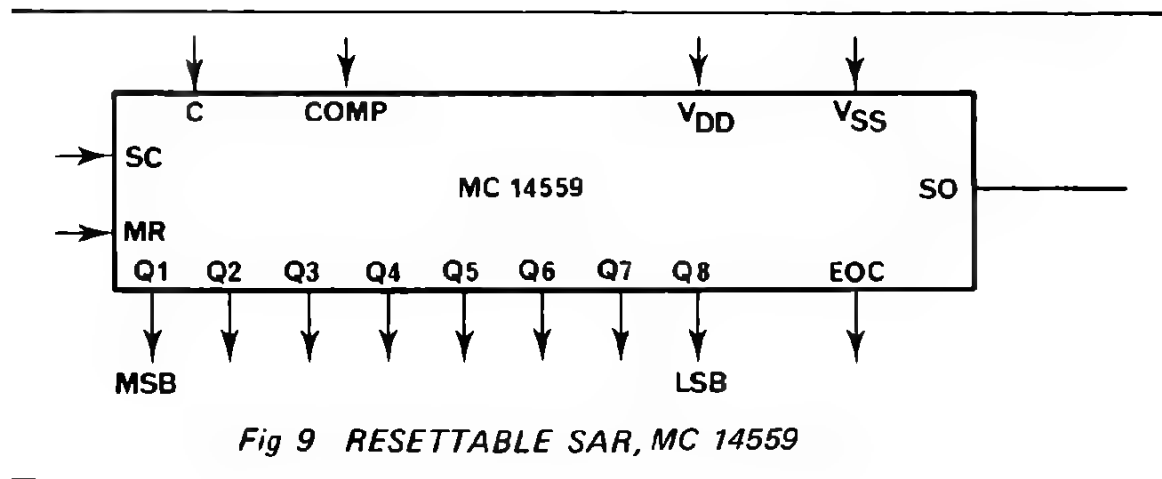
The resettable SAR shown in Figure 9 features a start conversion (SC), a master reset (MR), a clock (C), and a comparator (COMP) input, eight parallel data outputs Q_1 to Q_8 as well as an end of conversion (EOC) indicator output. In addition to the parallel data output a serial data output (SO) is available.

The circuit (shown in Figure 10) operates as follows:

Before starting the conversion cycle, the register is cleared by applying a logic 1 to the MR input. The conversion cycle starts when the MR input has been removed and a logic 1 is applied to SC. In synchronism with the clock, the operating sequence is as follows: The first output latch is set. Then the second output latch is set and the comparator output (a one or a zero depending on the value of the input) is simultaneously strobed into the first output latch where it remains permanently. This step is repeated for each bit, until the last output latch, corresponding to the least significant bit, is permanently set. At the following clock pulse, the EOC output goes high and simultaneously the whole conversion cycle is stopped. The output latches and the EOC output remains in that state until a new clear signal is applied to the MR input.

The sequential addressing of the output latches is done by an eight bit shift register, that is initially empty and is filled one stage at a time by logic ones.

The Master Reset clears this shift register as well as the output latches and prepares the total circuit for the next conversion cycle.



1. 3. NON-RESETTABLE SAR MC 14549

This SAR, shown in Figure 11, is a metal option of the MC 14559 and differs from this one by having no MR but instead a feed forward (FF) input. The circuit is cleared internally before starting the conversion cycle, as soon as a start signal is applied to the SC input.

If the SC input is held high, the conversion is continuously taking place, i.e. after each completed conversion a new cycle will start.

The feed-forward (FF) input allows the conversion to be stopped before a complete 8 bit cycle is terminated. If, for example, only five bits of the register are to be used, the 6th output has to be fed into the FF input, anticipating the end of the cycle right after the 5th conversion, generating an EOC signal and topping the cycle. The difference between these two registers will become clearer in the next section, where some of the most common applications are treated.

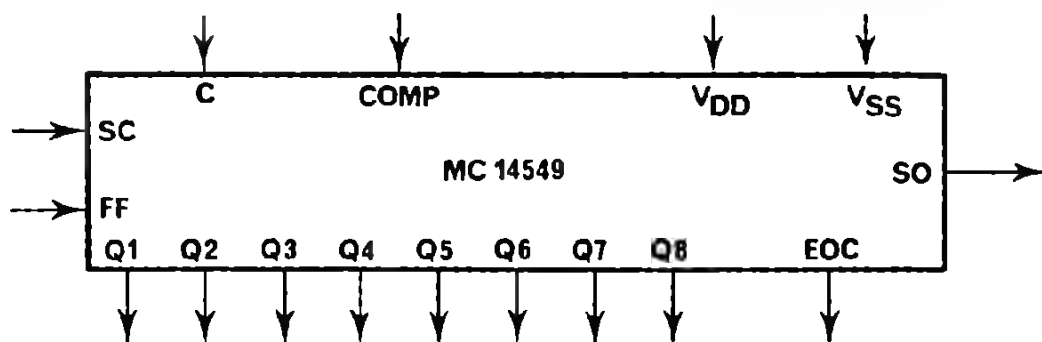


Fig. 11 NON-RESETTABLE SAR MC 14549

2. 4. APPLICATIONS

Externally controlled 6 bit ADC (Figure 12):

Several features are shown in this application:

Shortening of the register to 6 bits by feeding the seventh output bit into the FF input.

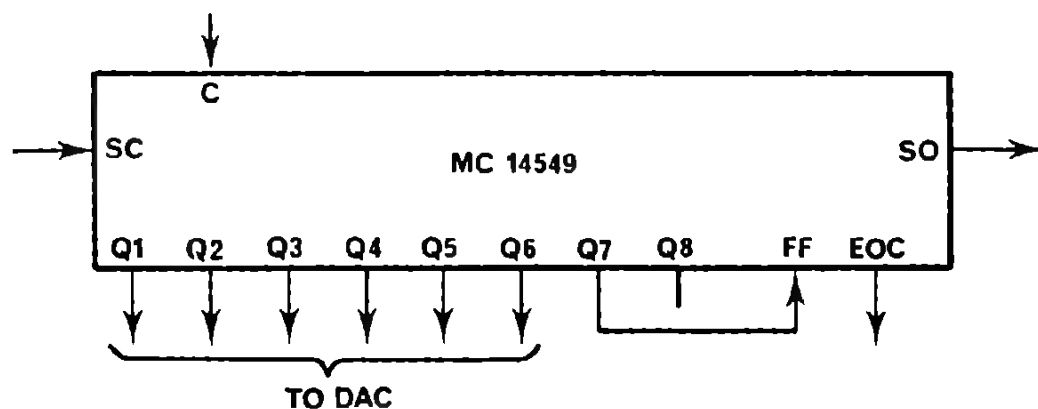


Fig. 12 EXTERNALLY CONTROLLED 6 BIT ADC

Continuous conversion, if a continuous signal is applied to SC.
 Externally controlled updating (The start pulse must be shorter than the conversion cycle).
 The EOC output indicates that the parallel data are valid and that the serial outputs complete.

Continuously cycling 8 bit ADC (Figure 13):

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously cycling 12 bit ADC (Figure 14):

Because each SAR has a capability of handling only an eight-bit word, two must be cascaded to make an ADC with more than eight bits.

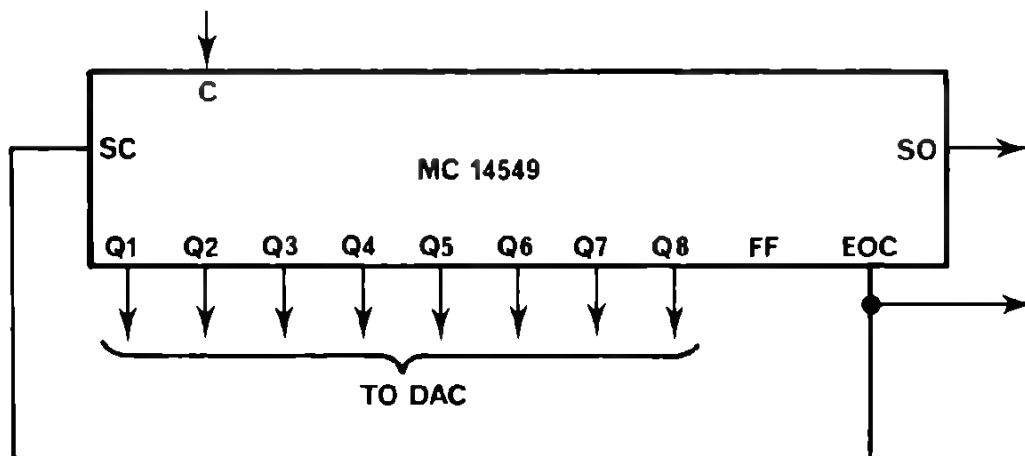


Fig. 13 CONTINUOUSLY CYCLING 8 BIT ADC

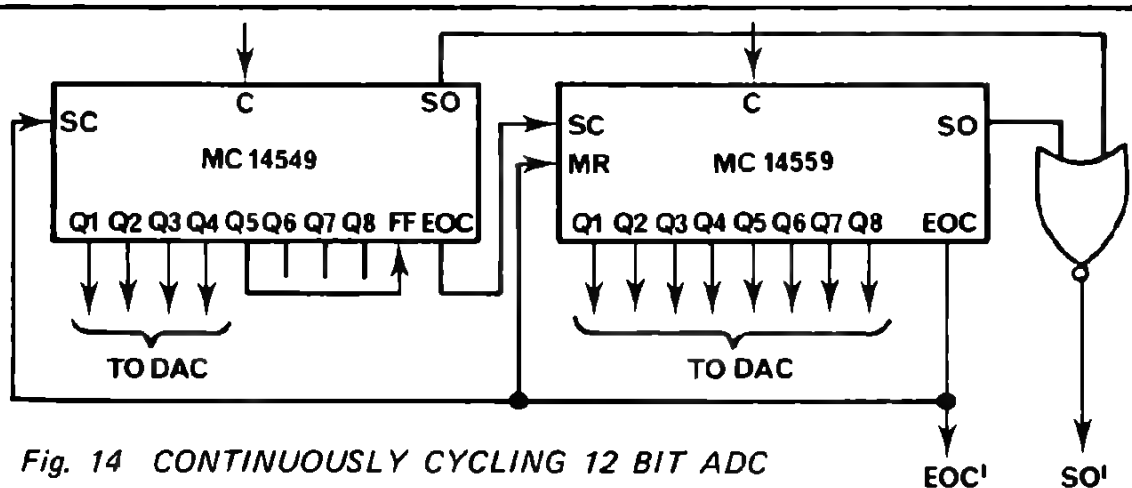


Fig. 14 CONTINUOUSLY CYCLING 12 BIT ADC

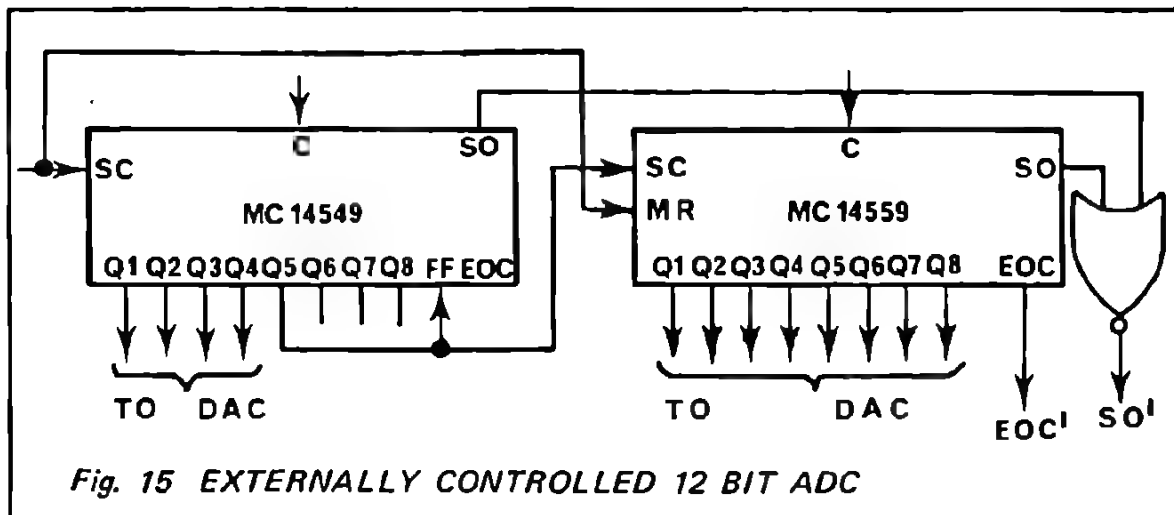
When it is desired to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling. The reason for this can easily be illustrated with reference to Figure 14. If during switch-on or due to outside influences the first stage has entered a reset state, the entire ADC would remain in a stable non functional condition.

This 12 bit ADC is continuously recycling. The serial as well as the parallel output are updated every thirteenth clock pulse. The EOC' pulse indicates the completion

of the 12 bit conversion cycle, the end of the serial output word and the validity of the parallel data output.

Externally controlled 12 bit ADC:

Referring to Figure 15, the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q_5 of the first SAR goes high, the second SAR starts conversion, whereas the first one stops conversion. EOC' indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.



2. 5. ADDITIONAL MOTOROLA PARTS FOR SUCCESSIVE APPROXIMATION ADC

In addition to the CMOS SARs, MOTOROLA manufactures other parts suited for use in SA-ADCs:

Monolithic digital-to-analog converters:

The MC 1408/1508 converter has eight bit resolution and is available with 6, 7 and 8 bit accuracy.

The amplifier-comparator block:

MC 1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADC's with an accuracy of up to eight bits, using as the register one MC 14549 or one MC 14559.

An additional CMOS block would be necessary to generate the clock frequency.

3. DUAL RAMP TYPE ANALOG TO DIGITAL CONVERTER

3. 1. PRINCIPLE OF OPERATION

The analog voltage (V_i) is applied to the input of a linear integrator during a fixed period of time t_1 (t_1 is defined by counting a fixed number n_1 of pulses at a clock frequency f_0 .) After the time t_1 has been completed the integrator input is switched to a reference voltage (V_r) of opposite sign, which causes the output voltage of the integrator, which has been increasing during t_1 , to decrease.

After another time interval t_2 , during which n_2 pulses may have been counted, t again reaches zero. This process generates the two ramp voltages from which the system derives its name.

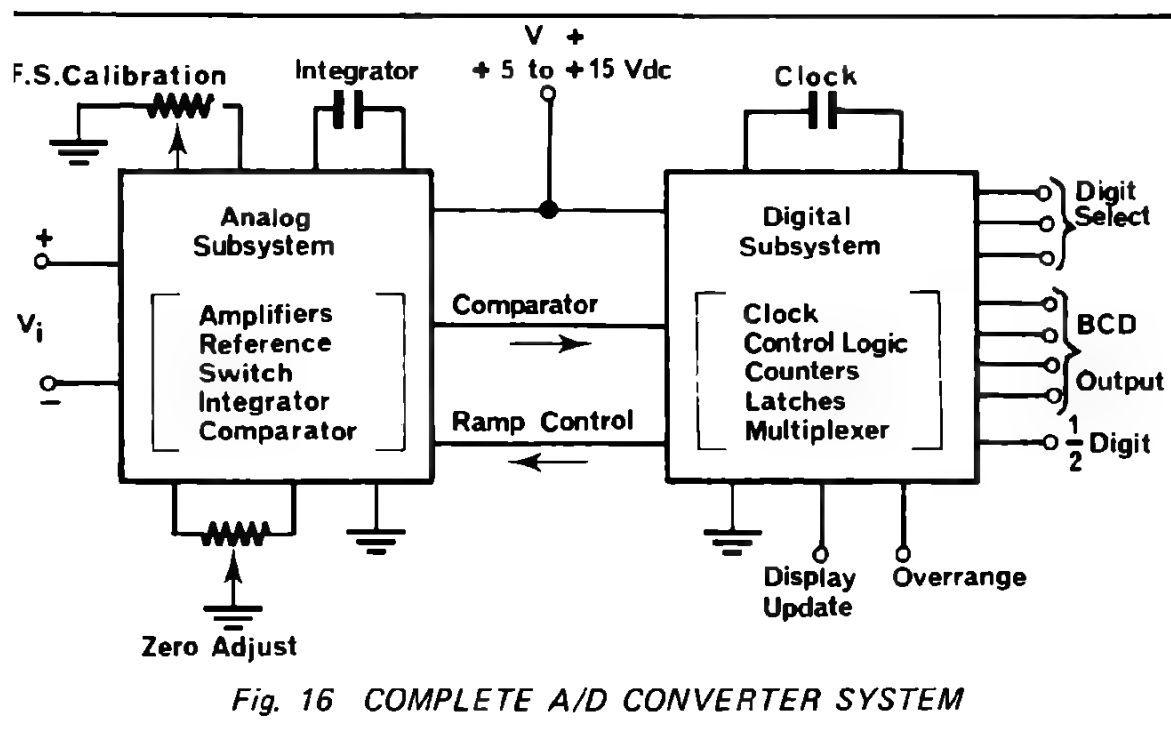
Because $V_i \cdot t_r = V_r \cdot t_2$ and $t = \frac{n}{f_0}$,

the input voltage can be expressed in terms of the counted pulses:

$$V_i = V_r \frac{t_2}{t_1} = V_r \frac{n_2}{n_1}$$

Notice that this expression does not depend on the clock frequency f_0 , provided that f_0 does not change during the conversion cycle. This means that the dual ramp system is fairly insensitive to the long term drifts of the clock frequency and of the other component values and thresholds.

The dual ramp system needs some linear parts for operation, i.e. an integrator, a voltage comparator and analog switches. The associated digital circuits contain the counters, the control logic and the output latches. This paragraph will discuss the whole MOTOROLA system and not just the digital CMOS control logic, because the whole ADC set should be considered as an entity. This is justified because the complete linear circuit is contained on one single linear chip and all the logic circuitry on a single CMOS chip. Both chips are encapsulated in the familiar 16 pin dual-in-line package. Figure 16 shows their interconnections.



1. 2. ANALOG SUBSYSTEM MC 1505

The analog subsystem shown in figure 17, contains all the analog functions needed for A/D conversion using the dual-ramp method.

As may be seen from the schematic of Figure 17, the input voltage is converted into a current which is switched either to the input of the integrator or to

he positive power supply line, depending on the state of the ramp control circuit. Similarly to the input current, the reference current is also switched either to the input of the integrator or to the ground line, again depending on the state of the ramp control circuit.

n addition to the input current, another fixed current, called the offset current, I_o , is connected to the integrator input when the ramp control input is low. This offset current causes the output voltage of the integrator to increase by a fixed amount during the first, fixed, integration period, even when no analog input voltage is applied to the voltage input terminals. This output voltage increase must be compensated during the second integration period, when the reference current is applied to the integrator input, by counting an additional fixed

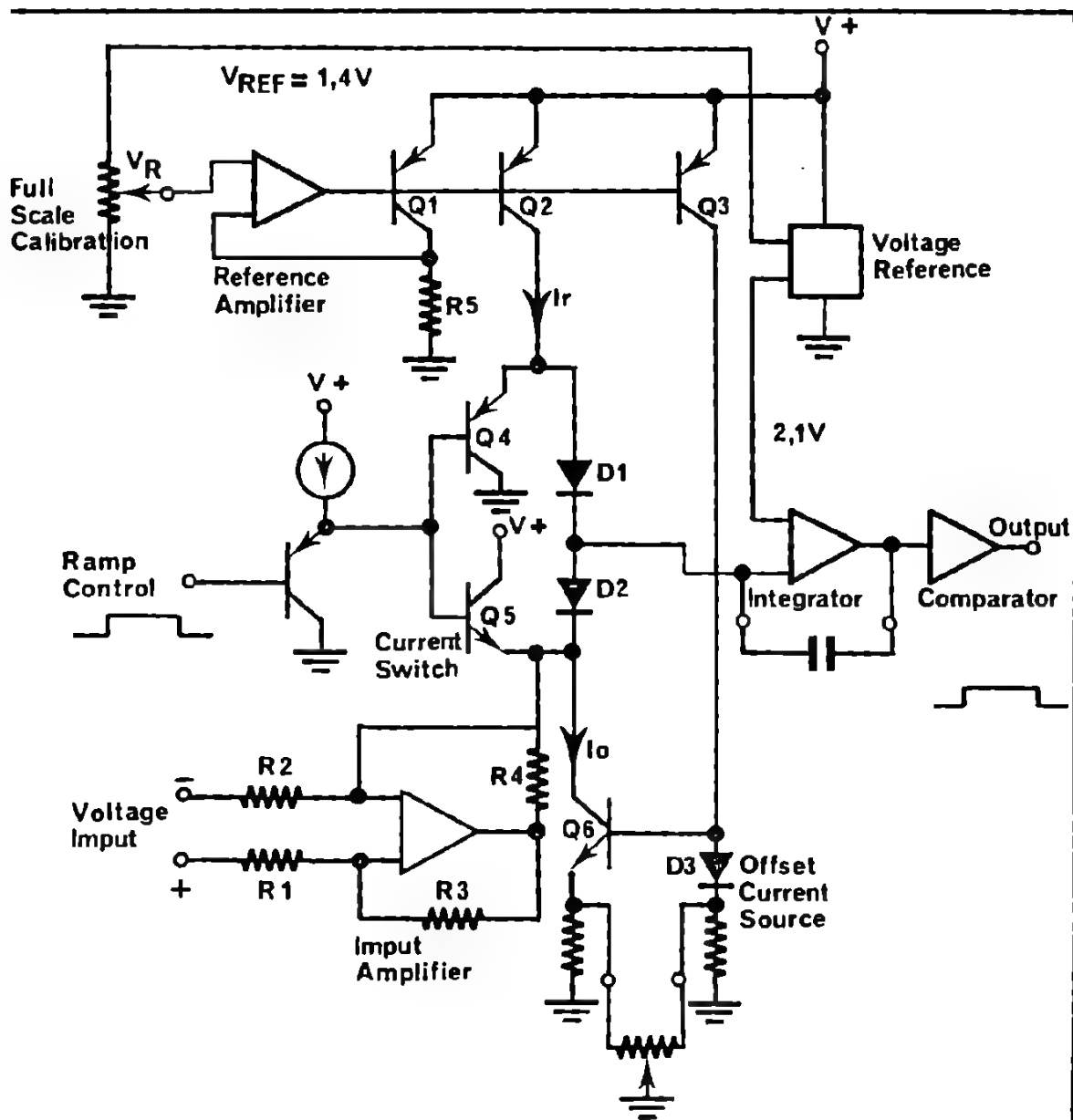


Fig. 17 SIMPLIFIED SCHEMATIC OF THE ANALOG SUBSYSTEM

number of clock pulses, say n_0 . Mathematically speaking, referring to the terminology employed previously, this means:

$$I_0 \cdot \frac{n_1}{f_0} = I_R \cdot \frac{n_0}{f_0}$$

The fixed number of counts, n_0 will be considered further in the next section where the digital subsystem is treated.

The output of the integrator is connected to the comparator that detects when the integrator output voltage crosses the reference level. The output of this comparator has to be connected to the digital control system.

3. 3. DIGITAL SUBSYSTEM MC 14435

As shown on the block diagram of Figure 18, an internal clock generator, needing just one external capacitor, synchronizes the whole ADC system. The system operates as follows:

The ramp, produced by the sum of input current and offset current, starts when the ramp control output is low. At the moment the ramp crosses the reference level of the comparator, its output goes high, beginning the counting in the 3 1/2 digit counter. The counter counts to 1999, then the ramp control output goes high, whilst the counter goes to zero. From now on the ramp voltage

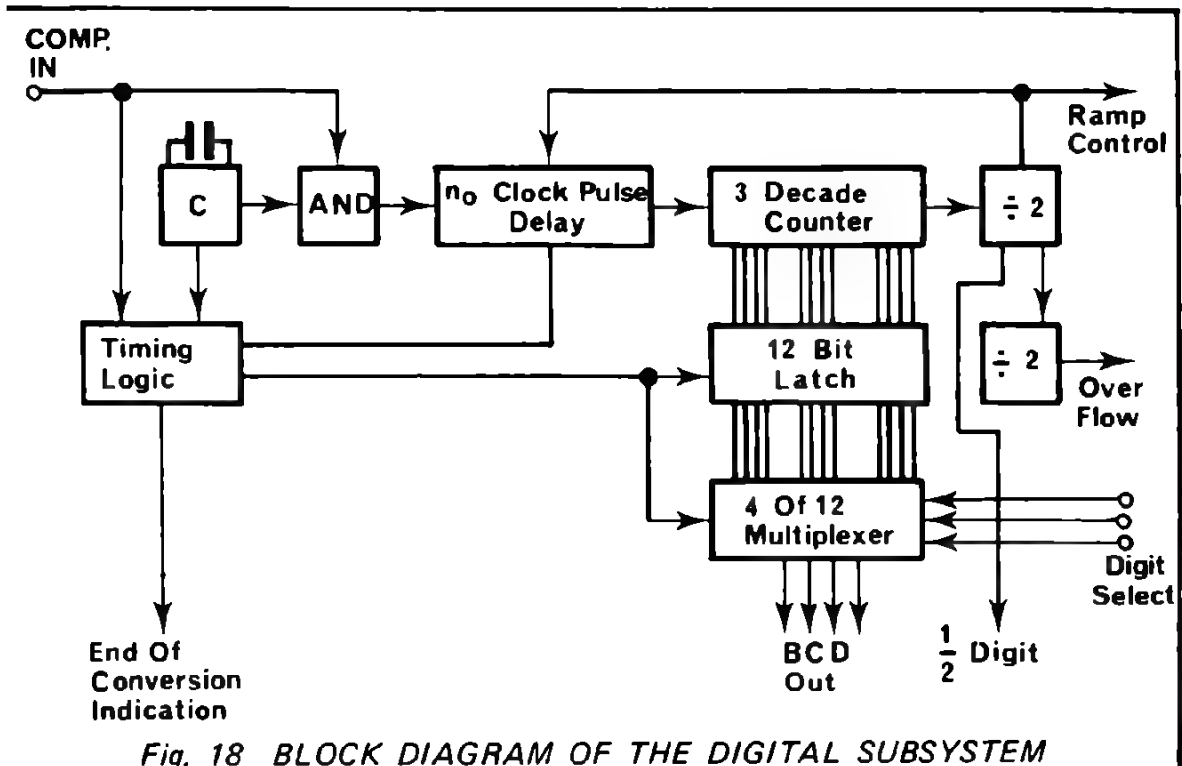


Fig. 18 BLOCK DIAGRAM OF THE DIGITAL SUBSYSTEM

decreases because the reference current is of opposite sign. After a delay of n_0 clock pulses, the 3 1/2 digit counter is refilled until the ramp again crosses the reference level of the comparator. The comparator then goes low and stops the counting.

The delay of n_0 clock pulses serves to compensate for the effect of the offset current mentioned above. This method has been chosen to avoid the transients caused by the current switching in the analog subsystem; for even at zero input voltage, the ramp voltage is above zero when the current switches are actuated, due to the integration of the offset current. At the same time this method guarantees a definite conversion time even at zero input voltage.

When counting is stopped by the comparator, the contents of the counters are strobed into the 12 bit latch from whence they can be displayed on the four BCD output lines via the multiplexing circuit provided, for this purpose.

3. 4. RESUME OF THE SYSTEM'S PERFORMANCE

The system offers several interesting features that are worth a short review; 3 1/2 digit resolution, typical accuracy of 0.02% of full scale.

All circuitry is contained in two 16 pin dual-in-line packages; only two external capacitors and two potentiometers are needed.

The system operates from a single power supply voltage between +5 and -15 volts.

The typical power consumption is 50 mW at +5 volt power supply voltage.

The conversion speed is faster than 5 ms.

C. DISPLAY SYSTEMS

1. CMOS DECODER-DRIVERS

There are various CMOS parts which can be used to drive display readout elements. For relatively high power consuming elements such as LEDs, incandescent lamps or mechanical readouts, several output buffers MC 14009, 14010, 14502, 14049, 14050, are available which are well suited for use as output drivers. Low power readouts, such as liquid crystals can even be driven directly from the output of standard CMOS gates and flip-flops.

However, some more complex CMOS circuits exist that are able to convert a BCD coded input word into an output word corresponding to the familiar seven segment numerical readout. These blocks are the MC 14511 and the MC 14543.

The MC 14511 is a BCD to seven segment latch-decoder-driver featuring a 25 mA output current sourcing capability. Its operation is best illustrated by having a look at the logic diagram represented in Figure 19.

The latch-enable (LE) input gates the BCD coded input data into the decoding network and also strobes the data into the input latches; If LE is low, the input data are fed through the input latch to the decoder, if LE is high, the input remains open and is isolated from the latches. However, if during the time the input data are present, the LE goes first low and then high, the input data are strobed into the input latches and remain stored there.

In addition a lamp-test (LT) input is provided to display the number 8 (all segments "on") at the readout, independent of the state of all other inputs, if a logic zero is applied to \overline{LT} . The \overline{LT} input must therefore be high for all other operations of the circuit.

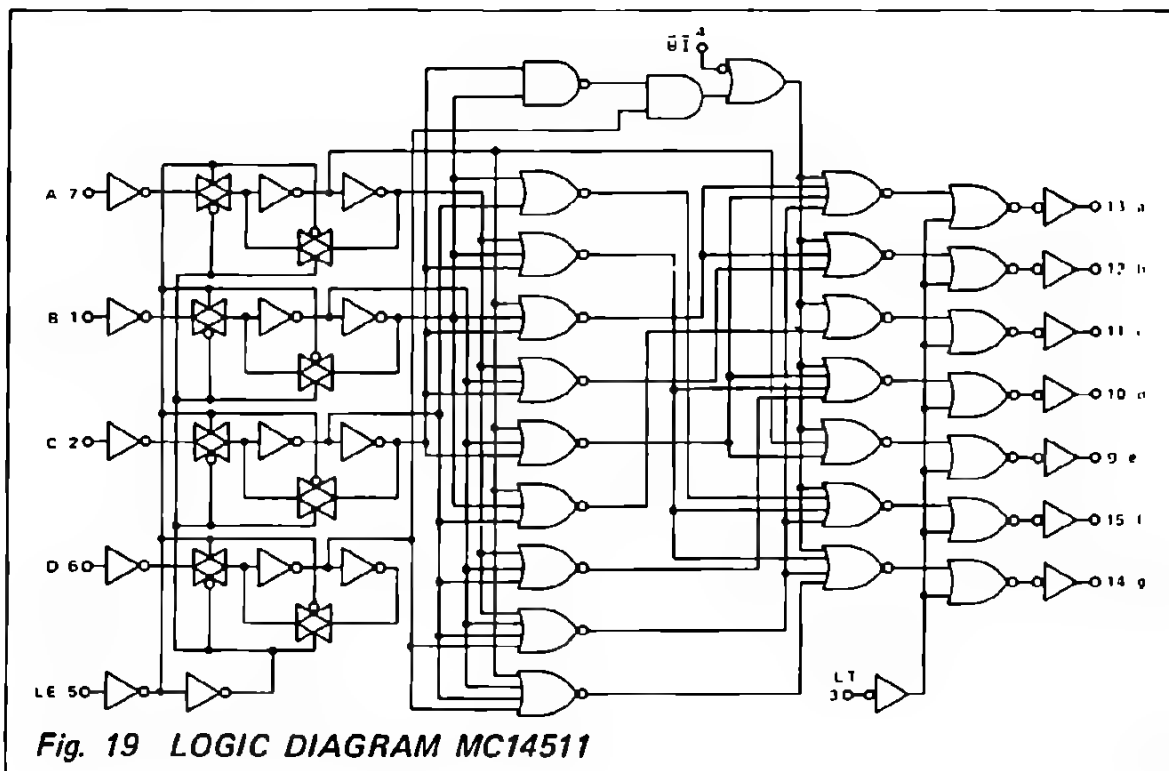


Fig. 19 LOGIC DIAGRAM MC14511

The BI input blanks the display if a logic zero is applied.

The output boosters are equipped with a (bipolar) emitter follower, allowing a current of 25 mA to be sourced to the load. Therefore the circuit is able to drive common cathode LED and incandescent readouts directly (Figure 20 and 21).

For other readouts, namely, common anode LEDs, gas discharge tubes, etc. external driver transistors or IC's are needed.

Liquid crystals need to be driven by a.c., if their life expectancy is not to be degraded. The MC 14511 is therefore used in these applications together with a phase inverter circuit as is shown in the next circuit diagram (Figure 22)

However, to drive liquid crystals, another decoder-driver is available which needs no additional circuitry to provide the a.c. drive to these readouts: The MC 14543.

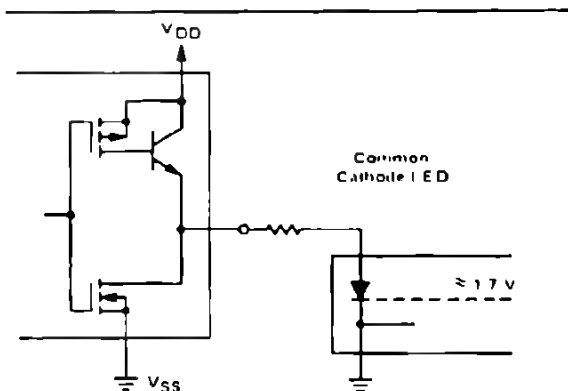


Fig. 20 MC14511 DRIVING COMMON CATHODE LEDs

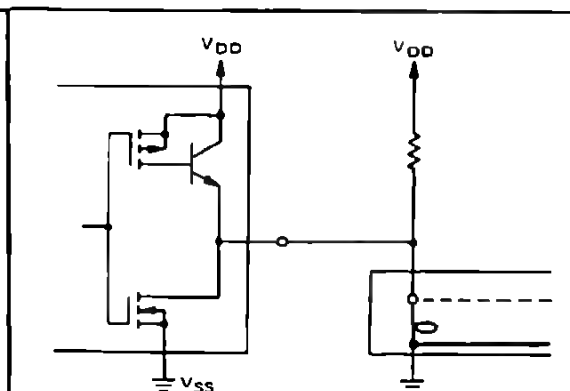


Fig. 21 MC14511 DRIVING INCANDESCENT LAMPS

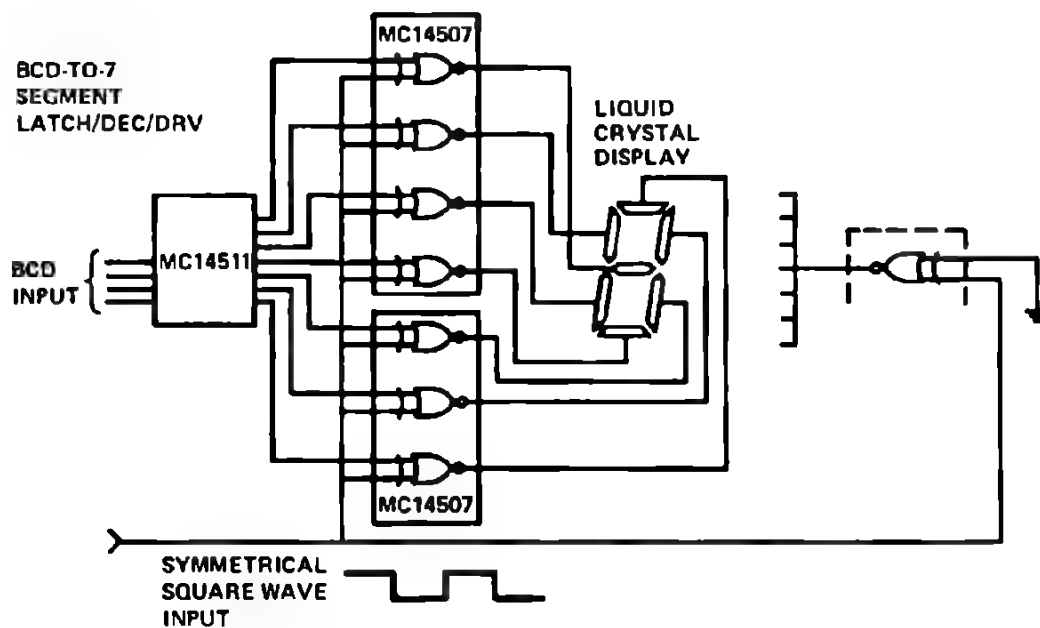


Fig. 22 DRIVER CIRCUIT FOR LIQUID CRYSTAL DISPLAY

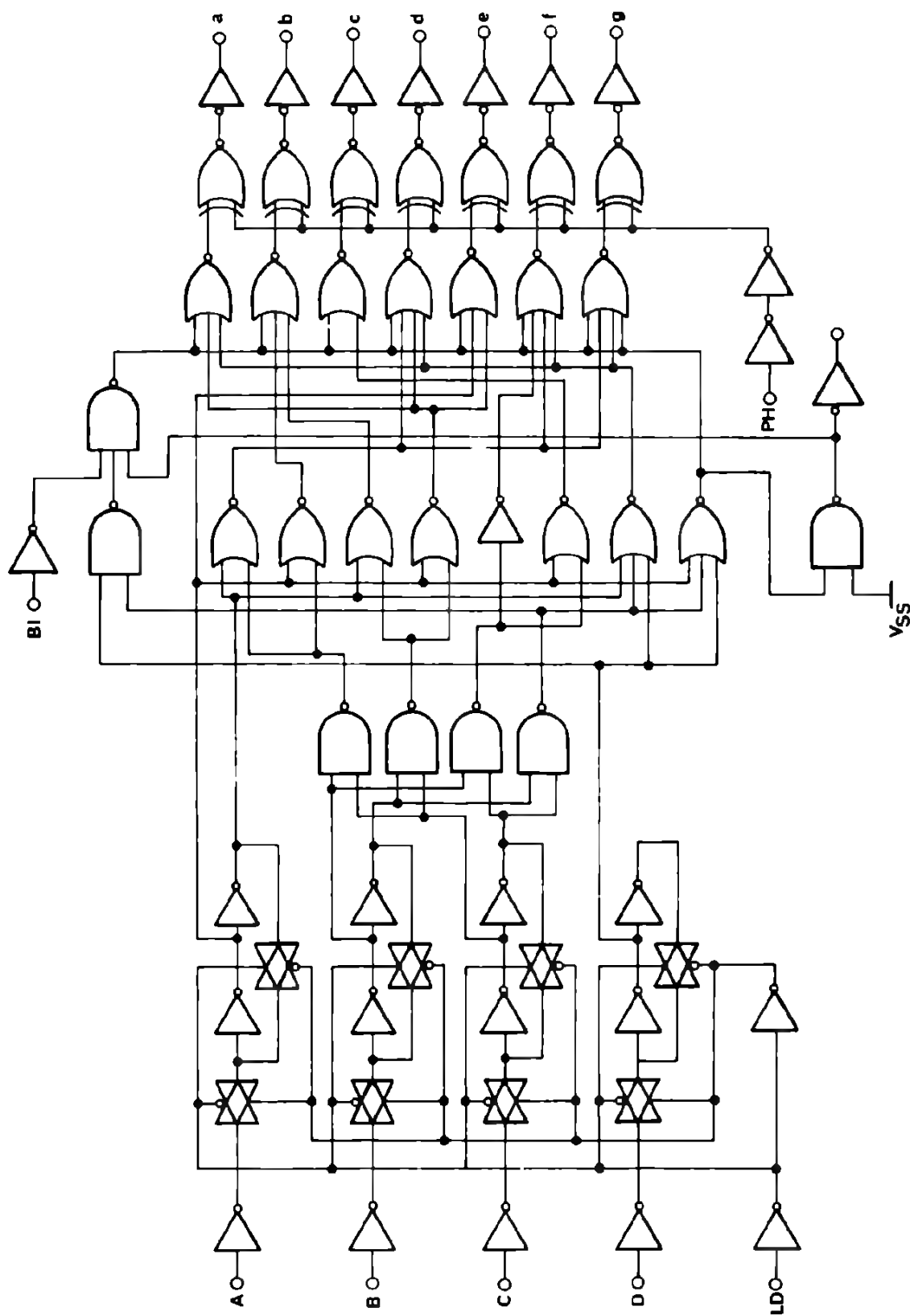


Fig. 23 LOGIC DIAGRAM MC 14543

The logic diagram in Figure 23 shows how this circuit differs from the MC 14511. The input latches are similar to those of the MC 14511 but they need an opposite command signal ($LD = \overline{LE}$). Also the blank input (BI) needs a logic one to blank the display. A very important feature is the phase-input (PH). This input allows the designer to invert the whole input-output truth table by applying a logic one to it.

When driving liquid crystals, this input is connected to a square wave as well as to the common plane of the liquid crystal. Thus for each activated segment the signal applied to the front electrode is 180° out of phase relative to the black plane, whereas for unselected segments both electrodes are in phase, resulting in a net zero voltage between them. But the phase-input provides another advantage:

Because the output buffers of the MC 14543 are able to source and to sink about 10 mA of output current, they are able to drive single LED seven segment readouts. The PH input permits driving both kinds of LED readouts without additional external circuitry: If a common cathode readout has to be driven the PH input must be low, whereas for common anode devices PH must be high.

2. MULTIPLEXED DISPLAYS

In a multiplexed display system all individual numerical readout elements share one common decoder-driver.

For example if such a system has n digits, each digit is activated only during a time $\frac{T}{n}$ and remains unactivated during a time $\frac{n-1}{n}T$, T being the time necessary to scan all the n digits (display cycle period). Also the data to be displayed on the selected digit are only presented to it during the time it remains activated. The display cycle period T is chosen so that the eye does not perceive the flicker of the readout.

There are different reasons for using multiplexed display systems, such as saving power and saving the costs of individual decoder drivers for each readout element. On the other hand, some more recent multidigit readout elements, LED and gas-discharge types, need to be operated in a multiplexed mode, because there are not a sufficient number of outside connections to allow continuous mode operation. It is therefore worth discussing these types of displays especially because CMOS elements are very well suited to this kind of application.

Here, a four digit multiplexed seven segment gas discharge display will now be considered (Figure 24).

The content of the MC 14518 BCD counters is strobed into the MC 14508 latches by applying a positive pulse to the strobe input. The outputs Q_0 to Q_3 of these four latches are connected to a common four bit data bus, leading to the decoder-driver.

It is possible to use this common data bus because of the unique tri-state feature of the MC 14508: if the disable (DIS) input is high, the outputs of the MC 14508 are isolated from the latch by an open transmission gate. In this state, the latch exhibits a very high output impedance, hence presenting virtually no load at all to the data bus. The operation sequence of the circuit is the following:

One digit is selected and at the same time, the output of the corresponding latch is enabled. Its data output pattern is then fed through the data bus to the

he decoder driver, During this period all other latch outputs are disabled. Before the operation is repeated at the next digit the first digit and latch is disabled. After four operations all digits have been scanned and the cycle starts again. The scanning speed is given by an external oscillator (SR). Notice that the only bipolar circuit elements used in this circuit are the segment and the digit drivers. All other circuits are in CMOS.

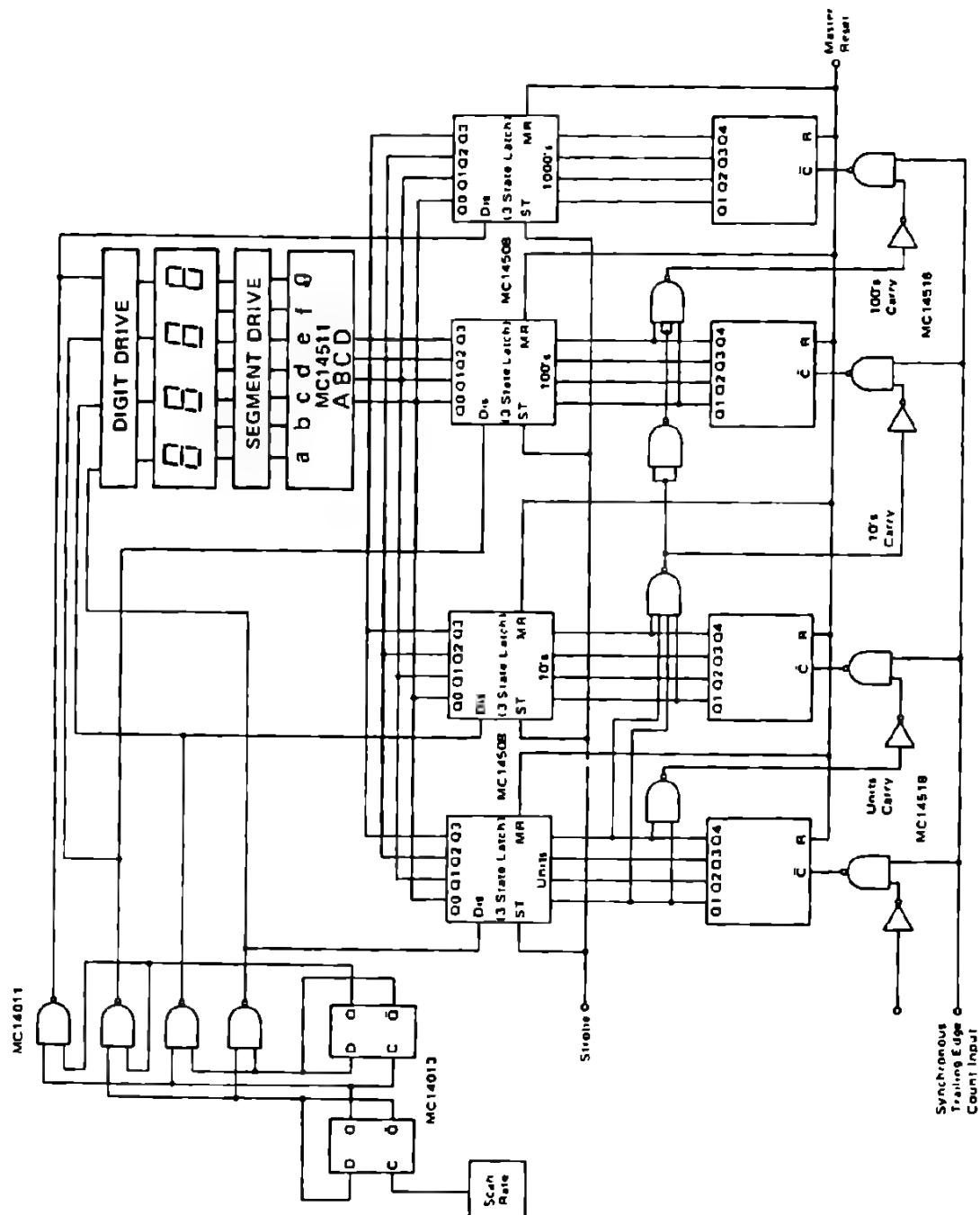


Fig. 24 FOUR DIGIT MULTIPLEXED NIXIE GAS DISCHARGE DISPLAY

D. DIGITAL TIMERS

INTRODUCTION

The basic principle of digital timing is simple and well known. A clock of known frequency is started at the beginning of the interval to be timed. It is run into a counter and when the required number of pulses have been counted, the time has elapsed. Figure 25 shows a typical example. The advantages of a digital timer are accuracy, assuming the clock is accurate, and fine resolution on longer times, if a fast clock is used.

However, in many applications the latter of these attributes is not an advantage but rather the opposite. Since every possible multiple of the clock is available, the decoding of a specific time may take as many inputs as there are counting stages. For example, if the four intervals of 1 second, 1 minute, 10 minutes and 3 hours are desired, each interval may require the decoding of 14 signals since it takes 14 bits to give 1 second resolution in 3 hours. This is contrasted to an R-C timer, such as that of Figure 26 which could provide the same intervals with a 4-position switch. The accuracy of the analog timer would probably not be as good, but in many cases this is not a serious disadvantage.

In the controls industry, a stratum of complexity exists which is beyond the simple R-C timer in that it uses digital techniques, but has not yet reached the complexity of the minicomputer. For this use, it is possible to design digital timers which provide the simple address of the analog circuit while retaining the high accuracy of the digital circuit. This is accomplished by providing geometrically expanding timed periods, each being longer in duration than the previous by an increasing increment. Then one can obtain whatever time one wishes, up

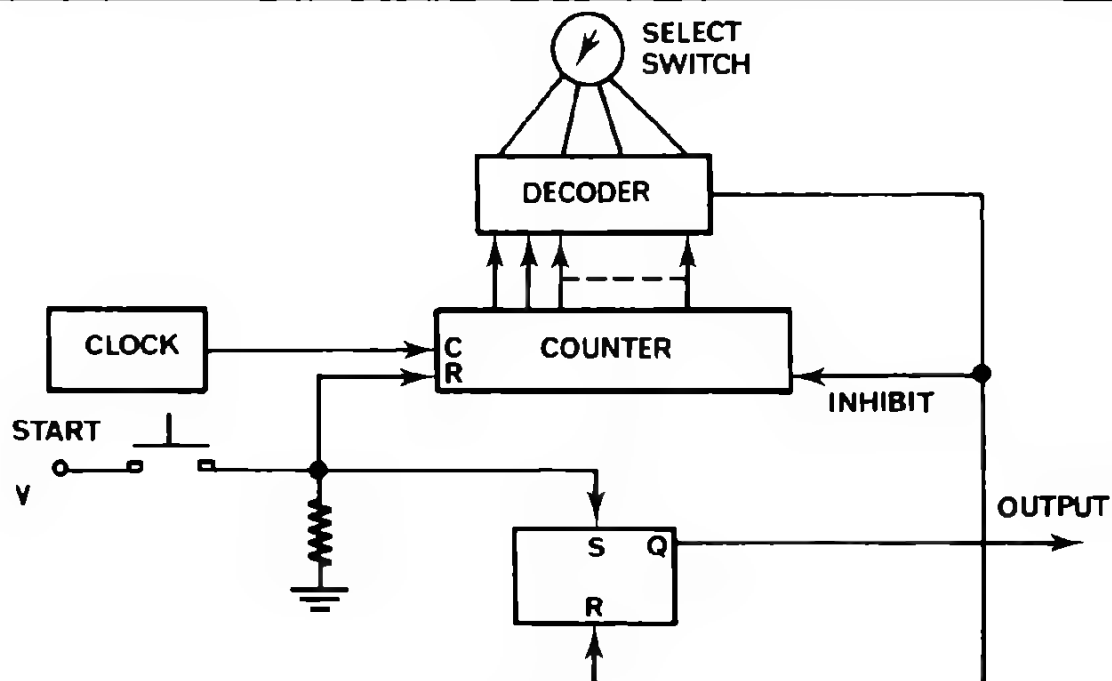


Fig. 25 TYPICAL DIGITAL TIMER

o the total timer duration, even more simply than with the analog system and within an accuracy of approximately plus-or-minus half the increment ratio. The total dynamic range which can be covered with only a modest number of steps is surprisingly large. For example, if each step is 50% longer than the previous, and the first is one second, then in 16 steps we have already reached a total duration of almost 440 seconds. In this section we shall discuss one way to design variable interval timers, proceeding from the initial examination of the problem through two intermediate configurations and ending up with a specific application.

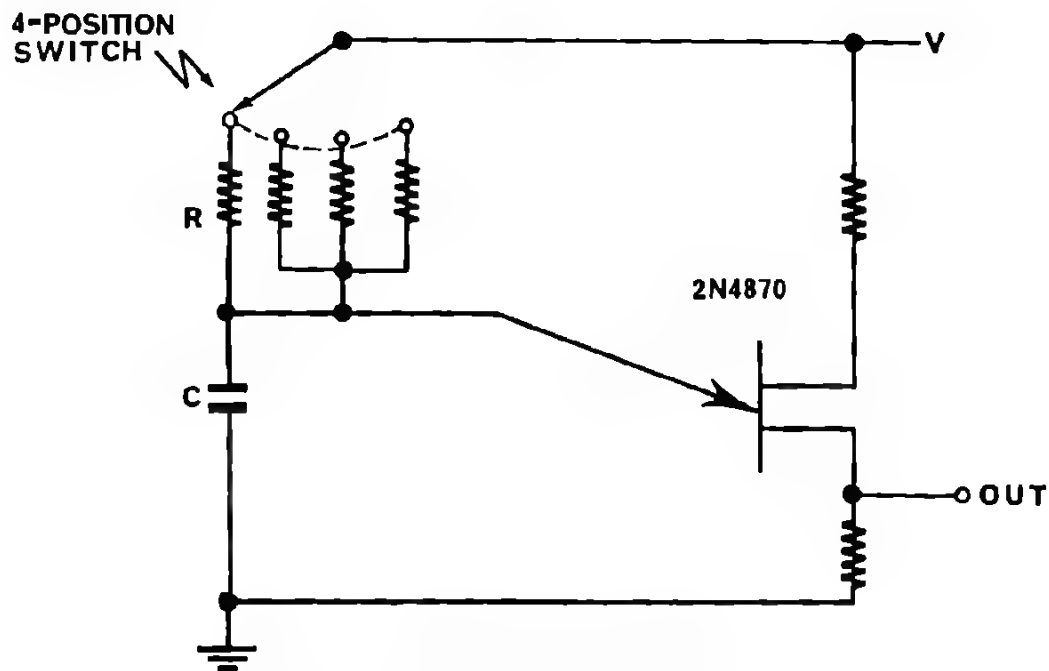


Fig. 26 UNIJUNCTION TIMER

2. DISCUSSION OF DESIGN PROCEDURE

Design of the digital circuitry to accomplish the timing function starts with an examination of the desired sequence of times, especially the increments. These will normally fall into a simple repeating pattern. For example, the timer which has each period duration 1.5 times the previous, also has increments which increase by a ratio of 1: 1.5. This can be implemented, at least for pairs of values, by a modulo-2/modulo-3 counter. We use two "count-throughs" of a counter for the first interval and three "count-throughs" for the second giving the desired ratio of 1: 1.5. However, a problem arises when we try to make a third increment which has a duration 1.5 times that of the second, in that the required number of counters expands rapidly as the number of steps increases. If a compromise is acceptable, however, a simple solution is possible. After each properly ratioed pair, we divide by two and repeat for the next pair. This gives ratios of 1: 1.5 between the first and second interval, 1: 1.33 between the second and third interval, 1: 1.5 again between the third and fourth interval, etc. This results in a useful sequence of times. Figure 27 is a block diagram of the scheme.

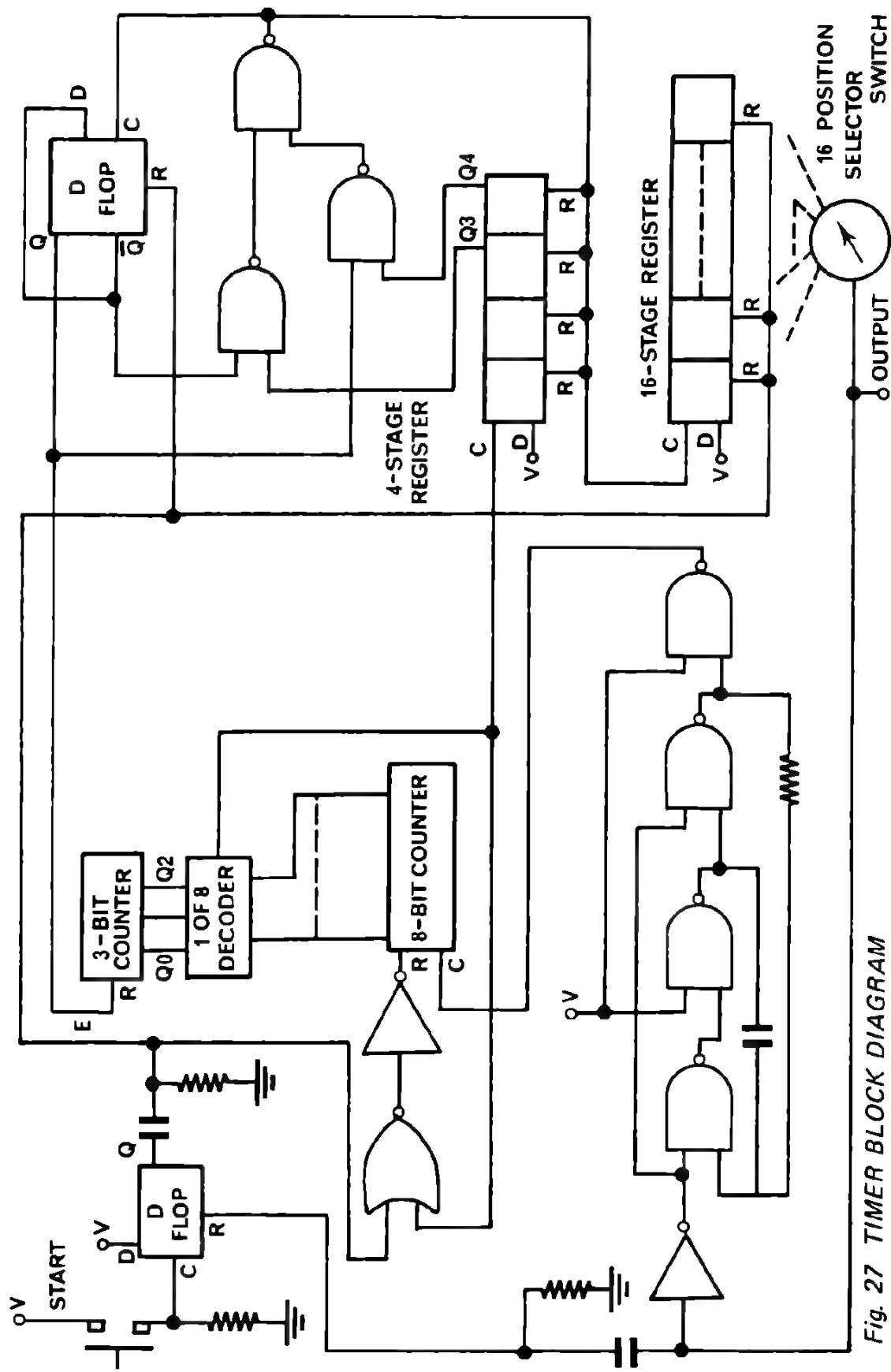


Fig. 27 TIMER BLOCK DIAGRAM

3. A SPECIFIC APPLICATION

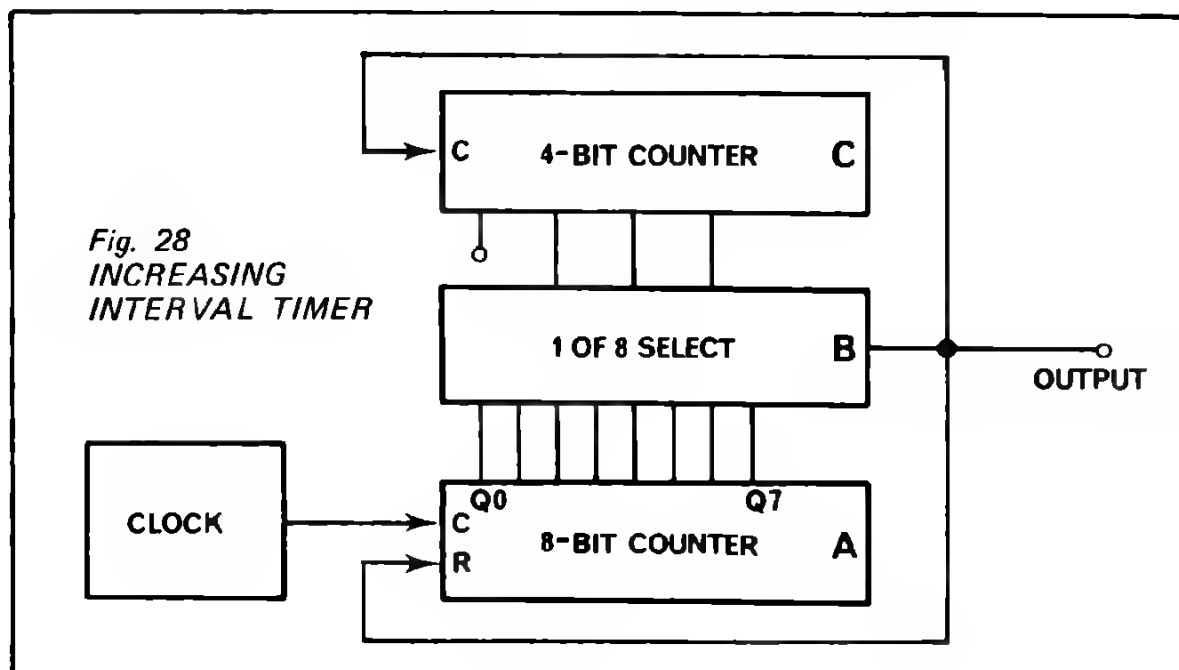
In photography, exposure is usually varied in 1 : 2 increments by changing the lens opening by one "f-stop". The finest resolution normally required is "half an f-stop" or an increase of $\sqrt{2} : 1$ for each setting over the previous one. Since, over a wide range of values, the photographic exposure is the product of light intensity (f-stop) and time, considerable convenience would be provided by a timer whose intervals varied in the same ratios as the lens settings.

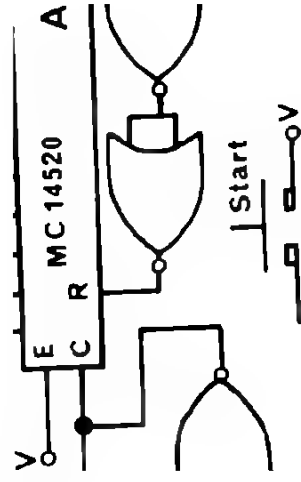
To make a timer which would produce total light duration periods in exactly the optical sequence would be difficult. However, if the sequence is changed only slightly, the problem becomes much easier. The simplified sequence is as follows:

Timed duration:	0	1	1.5	2	3	4	6	8	12	16
Increment:		1	0.5	0.5	1	1	2	2	4	4

The increments consist of identical pairs (except for the first) with each pair equal to twice the previous pair. Using the terminology of the previous discussion, the sequence can be generated by two "count-throughs" of an n-bit counter, two "count-throughs" of an (n+1) - bit-counter, etc., up to the number of increments necessary to provide the desired total time duration.

Figure 28 shows such a system. The 8-bit counter "A" is lengthened by looking at successive Q outputs with the 1 to 8 selector "B". In this scheme the 3-bit counter "C" is incremented only on alternate output pulses, so the last three stages of a 4-bit counter can be used to provide command signals to the 1-of-8 selector. Two additional functions, not shown in Figure 28 are necessary to produce a complete timer: the output pulses must be accumulated to a preset number by a shift register and selector switch, and all registers, flip-flops and counters must be reset by the start pulse as shown in the previous system.





Examination of the system waveshapes reveals that a 1-second clock gives times of 0,1,3,5,9,13,21,29... seconds. These have little resemblance to the simplified sequence which was desired. The principal problem is the start-up sequence: there is only one short increment instead of two and the initial long one is missing entirely. This situation can be alleviated by inhibiting the 4-bit counter until a sufficient number of initial short increments have been produced. In fact, if we allow four initial short periods, the timed interval durations can be: 0 0.5 1 1.5 2 3 4 6 8 12 16 24, differing from the desired sequence only by the addition of the first 0.5. Figure 29 shows an implementation of a complete timer which produces this sequence. The only additional parts over those of the previous timer which are needed to provide this change are 4-bit counter "E" and a gate package to make the S-R flip-flop "D". This is not a great sacrifice since the 4-bit counter is free - it was an unused half-package in the previous design. Operation is made clear by reference to Figure 30 the circuit waveshapes. The parts used in construction of this system included two MC 14001 and one MC 14011 gate packages, one MC 14512 data selector, two MC 14015 shift registers and MC 14520 counters. CMOS parts were selected to take advantage of the complex functions available, to allow use of a poorly regulated low current power supply and to avoid the transients inherent in many other logic families.

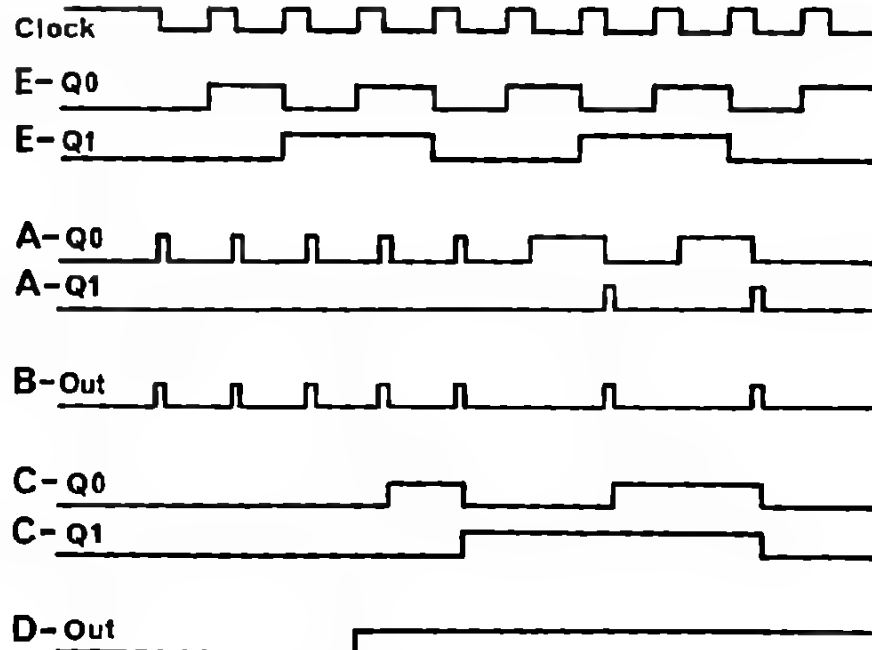


Fig. 30 TIMER WAVESHAPES

4. ACCURACY CONSIDERATIONS

There are two accuracy considerations which deserve comment. Since the intervals increase by a given percentage, clock accuracy need be only a corresponding percentage. For example, with each increment increasing by 50%, there is no sense holding clock accuracy to better than 5 or 10%. However, there is a way of using this circuit to provide long intervals which are also very accurate. For example, if 131 seconds is required, the timer can time out to 128 seconds, be reset, and then count out 3 seconds. In this case, we are assuming an accuracy of about one second out of 130, so clock accuracy must be within $\pm 0,5\%$. In industrial applications this type of accuracy can be easily attained by synchronizing from the power line.

E GENERATION AND USES OF PSEUDO RANDOM BINARY SEQUENCES

1. INTRODUCTION

Certain cyclic sequences of binary levels (0s and 1s) can be shown to possess the statistical properties associated with "randomness". However, these sequences, since they are cyclic, do have a defined periodicity. The name given to such series is pseudo-random binary sequence (p.r.b.s.), for obvious reasons.

The use of these p.r.b.s. is becoming more widespread in the fields of telecommunications, radar, signal coding, control systems, digital counting, bio-medicine, digital to analog conversion, flow measurement, etc.. In this discussion, digital techniques for generating some sequences will be discussed and several applications described in detail, making use of the complex functions available in CMOS.

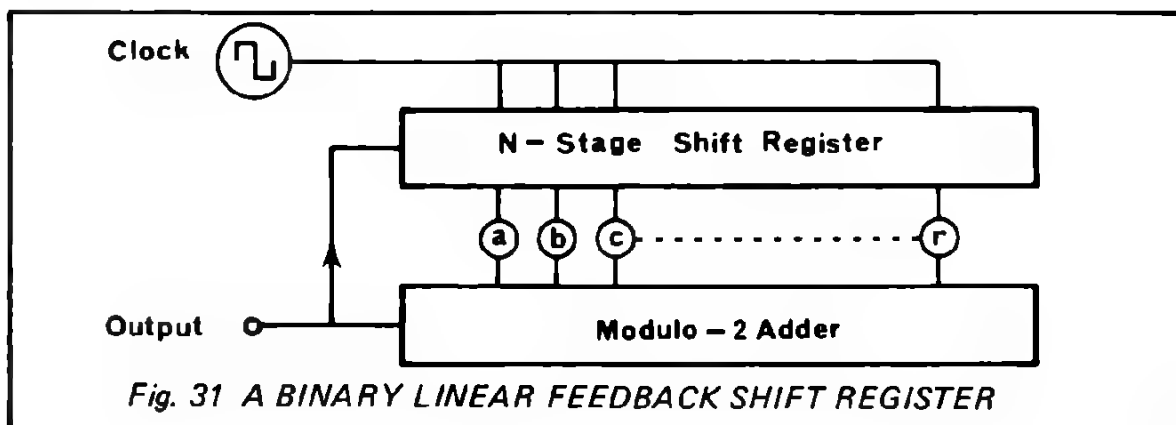
2. MAXIMAL LENGTH SEQUENCES

Many different p.r.b.s. have been described in various mathematical treatise; however, the series which are of most practical interest are those which can easily be generated with a small amount of electronic hardware.

The discussion here will be limited to the particular series known as maximal length sequences (or m-sequences) and derivatives thereof. In order to describe these m-sequences and their properties, it is easiest to show first how they may be generated.

2. 1. MATHEMATICAL DESCRIPTION

An m-sequence is the serially clocked output obtained from a binary linear feedback shift register when certain specific feedback connections are made by a modulo-2 adder. The diagram (Fig. 31) shows the connections which may be made.



In the general case, the coefficients a, b, c, \dots, r are binary multipliers or "presence coefficients". If for example, $a = 1$, this signifies a connection is made from the first stage output (Q_1) of the shift register, to the modulo-2 adder. Modulo-2 adding (identical to subtracting) involves logically adding all input levels, but ignoring carry over into higher significant bits. In effect, this means that if there is an odd number of high logic levels (1s) on the input lines, then the output is high (1). An even number of high inputs (1s) produces a low (0) level output.

If each cell of the shift register is represented as initially containing a binary value Y , and after a clock pulse this becomes Y' , then the following relations must hold.

$$Y_1' = aY_1 + bY_2 + cY_3 + \dots + rY_n$$

$$Y_2' = Y_1$$

$$Y_3' = Y_2$$

.

.

etc.

where the addition is modulo-2.

These equations can be written conveniently in matrix form as

$$Y' = T.Y$$

where T is defined as the transition matrix.

Example for $n = 4$:

$$\begin{bmatrix} Y_1' \\ Y_2' \\ Y_3' \\ Y_4' \end{bmatrix} = \begin{bmatrix} a & b & c & d \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \\ Y_4 \end{bmatrix}$$

If the vector Y is a given state of the shift register, then TY, T^2Y, T^3Y, \dots are the following states. If T^{-1} exists (regular matrix), $T^{-1}Y$ is the preceding state. For an arbitrary variable x , the polynomial, $\Phi(x) = \det(T - xI)$, is said to be the characteristic polynomial of T . Using modulo-2 arithmetic, this is equivalent to:

$$\Phi(x) = \det(T + xI), \text{ where } I = \text{unity matrix}$$

The characteristic polynomial for linear feedback shift registers

$$\text{with } n = 2 \text{ is } \Phi_2 = \det \left(\begin{bmatrix} a & b \\ 1 & 0 \end{bmatrix} + \begin{bmatrix} x & 0 \\ 0 & x \end{bmatrix} \right) = \begin{vmatrix} a+x & b \\ 1 & x \end{vmatrix}$$

$$\Phi_2 = (a+x)x + b = x^2 + ax + b.$$

$$\text{and for } n = 3 \quad \Phi_3 = \begin{vmatrix} a+x & b & c \\ 1 & x & 0 \\ 0 & 1 & x \end{vmatrix}$$

$$\Phi_3 = x \cdot \begin{vmatrix} a+x & b \\ 1 & x \end{vmatrix} + \begin{vmatrix} a+x & c \\ 1 & 0 \end{vmatrix} = x \Phi_2 + c$$

$$\Phi_3 = x^3 + ax^2 + xb + c$$

Evidently, this structure is general:

$$\Phi_n = x^n + ax^{n-1} + \dots + r$$

Assuming a regular transition matrix (i.e. T^{-1} exists), the flow graph of the shift register is composed of state cycles only. If k is the smallest integer such that $T^k = I$, then the cycles of the flow graph have lengths k , or multiples of k ($T^k Y = Y$).

The maximum cycle length obtainable with the circuit shown in figure 31 is $k = (2^n - 1)$ with the all-zero state eliminated (since this state is a self-sustaining singleton). If every possible (n -tuple) state of the $(2^n - 1)$ states of the shift register is obtained sequentially once and only once in the cycle, the binary output sequence from any stage of the shift register is defined as a maximal length sequence. In order to obtain this condition, the feedback coefficients must be chosen such that the characteristic polynomial $\Phi(x)$ is :

- (a) irreducible i.e. $\Phi(x)$ must contain no factors with binary coefficients
- (b) primitive i.e. $\Phi(x)$ must not be a factor of $(x^k - 1)$ for k smaller than $(2^n - 1)$.

A table of irreducible primitive polynomials up to degree 34 has been compiled by Peterson and Weldon (Error-correcting Codes, M.I.T. Press, 1972). This table permits the determination of the necessary feedback connections to the appropriate stages of the shift register (up to 34 stages) to give the respective m -sequences.

2. 2. CIRCUIT REALISATION USING CMOS ELEMENTS

Only two components are needed (apart from the clock) to generate a maximal length sequence. These are a modulo-2 adder and a shift register, for which access is available to several stages. The connections between the shift register stages and the input to the modulo-2 adder are determined by the mathematical relationship defined in the previous section.

Modulo-2 addition circuits:

The description of modulo-2 addition (or subtraction) given earlier shows that it is equivalent to the logical EXCLUSIVE OR function.

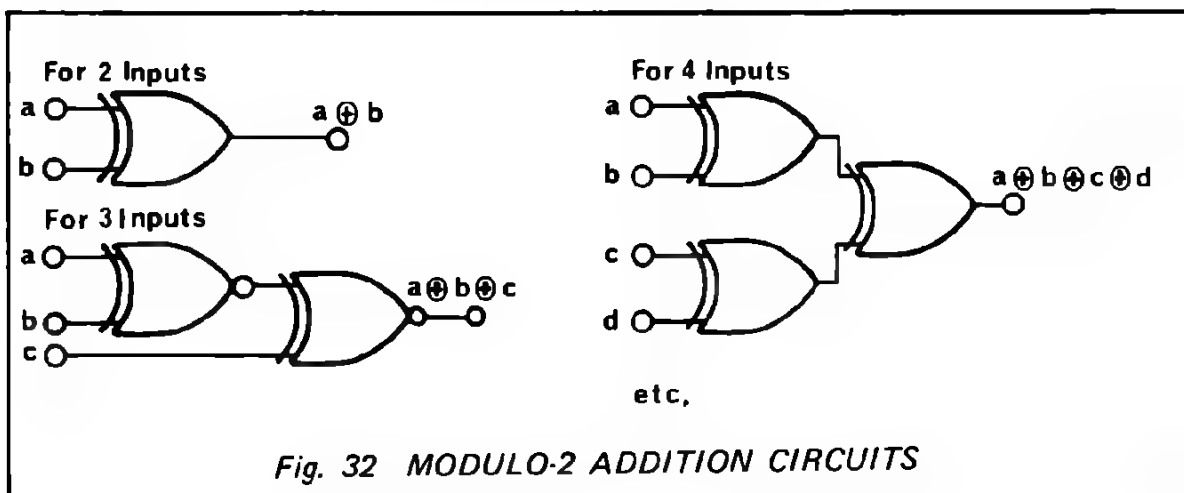


Fig. 32 MODULO-2 ADDITION CIRCUITS

For an even number of input lines, EXCLUSIVE OR is obtained by combining 2-input EXCLUSIVE OR circuits (MC 14507). For an odd number of input lines, the EXCLUSIVE NOR 2-input circuits (MC14519) should be used, as is shown in Figure 32. To reduce the parts count, the more complex 12-input EXCLUSIVE OR (MC 14531) may also be used if more than five inputs are needed: The basic element of a shift register is the D-type flip-flop (1/2 MC 14013). Any number of these may be used to build up the required shift register length. A variety of CMOS integrated circuit shift registers are available, details of these are given below.

Part No	No of stages	Access to Q outputs
MC 14006	18	4, 8, 9, 13, 17, 18,
MC 14015	2 x 4	ALL
MC 14021	8	6, 7, 8
MC 14034	8	ALL
MC 14517	2 x 64	16, 32, 48, 64 (of each)

Feedback connections:

It may be shown that to generate an m-sequence, an even number of feedback connections are required as inputs to the modulo-2 adder. Furthermore, an examination of the table of irreducible polynomials shows that, at least up to degree 34, it is not necessary to use more than four feedback connections to enable the required length m-sequence to be generated (in many instances, only two connections are needed). A partial listing of these simple feedback connections is shown in the table following.

Starting and synchronization:

One problem that is encountered in using an m-sequence generator in a system, is that of setting the shift register starting state. This is particularly important where two identical sequences are to be generated with a controlled delay between them.

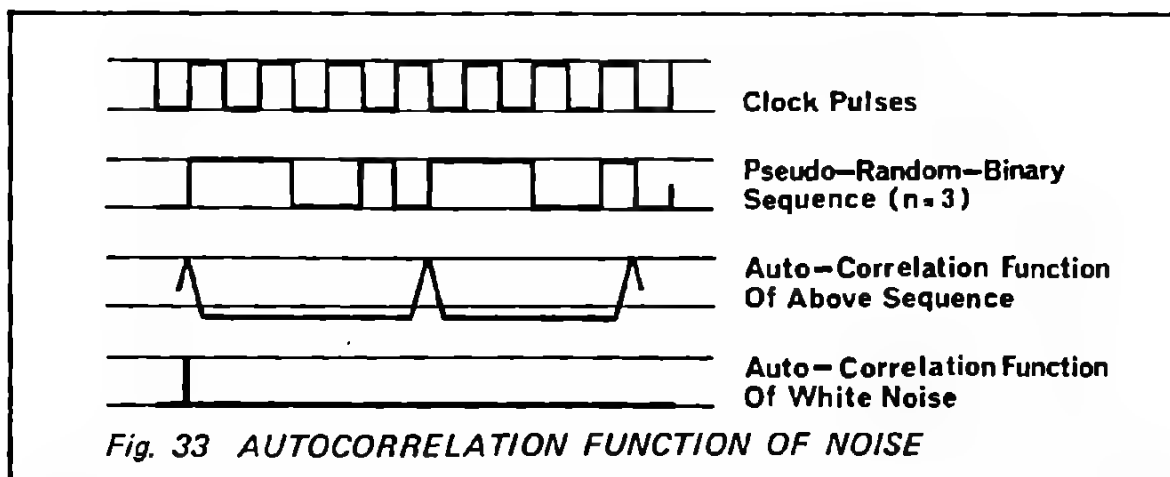
When the shift register consists of D-type flip-flops (MC 14013), starting is a trivial problem since any desired state can be set into the shift-register via each R-, S- or D-input. Similarly, the 8-stage shift-register (MC 14021) can be used without difficulty, since access is provided to all eight D-inputs. However, other shift-registers have only the capability of being reset in all stages simultaneously. This produces the very embarrassing all-zero state, which is not a permitted state in an m-sequence.

A simple way to avoid this difficulty is to make a p.r.b.s. generator using EXCLUSIVE NOR feedback. With exactly the same connections as described earlier for the EXCLUSIVE OR feedback, a "complementary" m-sequence is obtained. This has almost identical properties to the real m-sequence, except that the all-one state is now forbidden. Thus, simply resetting the shift register will cause the (now-permitted) all-zero state to serve as a starting reference, and synchronization can be readily achieved.

Shift register length (n stages)	Length of m-sequences ($2^n - 1$)	Number of feedback arrangements possible	Shift register output stage [Q] feedback connections (simplest case)
2	3	1	1, 2
3	7	2	1, 3
4	15	2	1, 4
5	31	6	2, 5
6	63	6	1, 6
7	127	18	3, 7
8	255	16	2, 3, 4, 8
9	511	48	4, 9
10	1023	60	3, 10
11	2047	176	2, 11
12	4095	144	1, 4, 6, 12
13	8191	630	1, 3, 4, 13
14	16383	756	1, 6, 10, 14
15	32767	1800	1, 15
16	65535	2047	1, 3, 12, 16
17			3, 17
18	etc.	etc.	7, 18
19			1, 2, 5, 19
20	etc.	etc.	3, 20
21			2, 21
22	$(2^n - 1)$	$\phi(2^n - 1)/n$	1, 22
23			5, 23
24			1, 2, 7, 24
25			3, 25
26			1, 2, 6, 26
27			1, 2, 5, 27
28		where $\phi(2^n - 1)$ is the Euler totient function for $(2^n - 1)$	3, 28
29			2, 29
30			1, 2, 23, 30
31			3, 31
32			1, 2, 22, 32
33			13, 33
34			1, 2, 27, 34

2. 3. PROPERTIES OF AN M-SEQUENCE

The characteristic used to define "randomness" is usually the auto-correlation function. For white noise, the continuous auto-correlation function is zero, except at one infinitely small point, as shown in Figure 33. A p.r.b.s. has an auto-correlation function which is constant (nearly zero) for all defined points in one period of the sequence, except at one point, where it is unity. If the auto-correlation function is examined on each side of this point, it reduces linearly to the constant (near zero) value, by the time the next clock pulse arrives.



In addition for an m-sequence, there are many useful characteristic features, which are summarized hereunder.

- (a) The period is $2^n - 1$
- (b) Each n-tuple (except the one forbidden one) appears exactly once each period
- (c) The number of ones in each period is 2^{n-1} , the number of zeros is $(2^{n-1} - 1)$. Note that the contrary is true for a complementary m-sequence.
- (d) The "shift and add" property. When a sequence is added (modulo-2) to a shifted version of itself, the resulting sequence is in turn a shifted version of the original.
- (e) If the sequence is sampled every f^{th} bit, then, when f is restricted to a power of 2, the same sequence results.
- (f) If, in the above operation, f is allowed to take all integer values between 1 and $(2^n - 2)$ then all the m-sequences of period $(2^n - 1)$ will be produced (each exactly n times) and no others.

Many of the above noted properties are essential for certain applications, as will become evident in the following discussion.

3. APPLICATIONS OF P.R.B.S.

P.R.B.S. may be found in many different electronic systems, and it has been shown earlier how to generate m-sequence using CMOS elements. In this section, a survey is made of various systems using p.r.b.s., and two specific examples are then discussed in detail

3. 1. GENERAL SURVEY

One obvious use of a p.r.b.s. is as a noise generator.

By choosing the correct combination of clock pulse period and number of shift register stages, the p.r.b.s. can be made to simulate, in a repeatable manner, the power spectrum of white noise over a controlled frequency range. In many applications, this provides a more useful noise source than the conventional techniques.

Examples may be cited as

- (i) Generation of Harmonic Spectra based on the clock frequency
- (ii) Dynamic measurement of system transfer function (see section 3.3).

The correlating properties of a p.r.b.s. may be applied to the measurement of precise time intervals, as for example in

- (iii) Radar ranging systems
- (iv) Fluid flow measurement.

For improved extraction of coded signals in noise without increase of mean signal power levels, p.r.b.s. have been used in

- (v) High resolution radar
- (vi) Synchronization of frames in telemetry codes (e.g. P.C.M.)
- (vii) Secure transmission of scrambled data (see also section 3.2).

A number of logic circuit designs have employed p.r.b.s., but, in general, with the increased level of complexity available in CMOS microcircuits, these are no longer of more than passing interest, except possibly to the microcircuit designer. However, a brief description follows here of a

- (viii) Programmed counter.

If an m-sequence is generated by an n-stage shift register, then it can be shown that the length of the sequence ($2^n - 1$) may be shortened, by using additional logic gates in the feedback, to cause a jump within the sequence ("Counting with Feedback Shift Registers by means of a Jump Technique" by P.R. Bryant, F.G. Heath, R.D. Killick-Trans. IRE on Electronic Computers, April 1962, pp. 285-6). Using this technique, the number of shift register states (i.e. clock pulses) per cycle may be chosen anywhere in the range from 1 to $2^n - 1$. The use of this technique is largely rendered obsolete by programmed counters such as MC 14510, MC 14516, MC 14522 and MC 14526.

Another interesting use has been in the design of a

- (ix) Digital to Analog converter.

This makes use of the properties of an m-sequence, that in a complete ($2^n - 1$) cycle the shift register state

1, 1, 1, 1, 1	1	occurs exactly once
X, 1, 1, 1, 1	1	occurs exactly twice
X, X, 1, 1, 1	1	occurs exactly four times
X, X, X, 1, 1	1	occurs exactly eight times
etc.		
etc.		(X is the "Don't Care" state)

The entire m-sequence is passed through a comparator containing the digital number to be converted. If a pulse is generated at the output every time coincidence occurs, then the number of output pulses in each cycle will correspond to the digital number. Integrating the output pulses will give the analog value of the digital number set into the comparator. This technique has now largely been rendered obsolete by the rate multiplier form of converter using the MC 14527 (see section B 1).

2. DATA SCRAMBLER

There are some very complex techniques used for communicating data under conditions of high security. It is beyond the scope of this discussion to do other than mention this fact, before proceeding to describe a simple "data scrambler".

A pseudo-random "data scrambler" can easily be constructed in CMOS, using three blocks for the transmitter and three for the receiver. There are three transmission lines required — one for the clock, one for the "scrambled" data and one for synchronizing the transmitter to the receiver.

The operation of the system can be seen from the schematic diagram (Fig. 34).

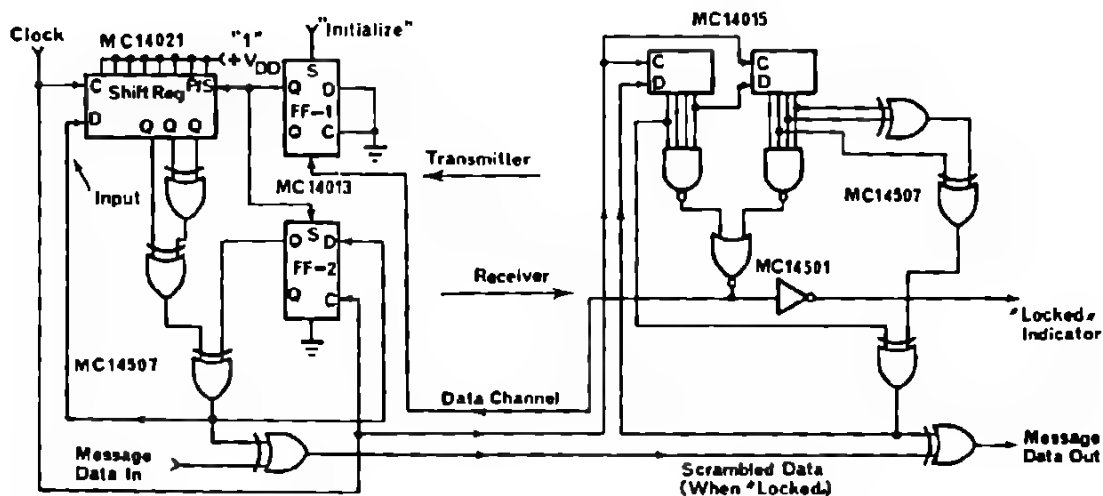


Fig. 34 PSEUDO-RANDOM DATA SCRAMBLER

The transmitter is basically a p.r.b.s. generator, against which the incoming data is EXCLUSIVE-ORED to scramble it. Decoding at the receiver is an identical process — scrambling the already scrambled data restores the required original. The MC 14021 is used to generate the transmitter p.r.b.s.. This 8-stage shift register has access provided to stages Q₆, Q₇ and Q₈, but to generate an m-sequence at least one other output stage is needed. There are three possible feedback combinations involving the last three shift register stages, but only one of these requires just one additional EXCLUSIVE-OR feedback connection. This is the combination Q₁, Q₆, Q₇ and Q₈, and is the one used here. Q₁ is obtained by taking the Q output of another D-type flip-flop which is run in parallel with the shift register input.

Exactly the same feedback connections are used in the receiver, where an MC 14015 (dual 4-bit) shift register is used. Synchronization is obtained by starting the MC 14021 (transmitter) at the all-one state, when the all-one state is also present at the (free-running) receiver. Since the MC 14015 (receiver) has access to all Q outputs the all-one state is detected by an 8-input AND (MC 14501) gate connected to all the outputs of the shift register.

After pressing the "initialize" button, the message data will be transmitted in clear, until the receiver reaches the all-one state. The transmitter is then started, the "Locked" indicator is energised and the scrambling process starts in synchronism at transmitter and receiver.

3. 3. LINEAR SYSTEM IDENTIFICATIONS

It is well known that the impulse response of a linear system subject to a white noise input, can be obtained directly by cross-correlating the input with the output. Conventional methods of identifying linear systems by their gain/phase frequency response or by their response to a step input change, may be extremely difficult to apply, in which case the correlation technique becomes attractive. Two particular problems suited to the cross-correlation technique are the identification of a system which may be easily saturated, and the identification of a system "on-line", without excessively disturbing its normal operation. This latter case is of major importance in systems employing adaptive control methods, where the impulse response is a parameter used in the control loop. A difficulty encountered in practice is that the noise source used must be "flat" over the range of the system response frequencies to be measured. The advantage of using a p.r.b.s. as the noise source is evident, in that the noise spectrum can be adjusted to suit the range of frequencies of interest. In addition, since digital techniques are used throughout, the cross-correlator becomes a simple analog switch driven by the p.r.b.s., with suitable delays included. In fact, the impulse response analyser can be realised entirely with CMOS digital circuits and an integrator (either digital or analog).

In constructing suitable cross-correlating equipment, the technique for obtaining the delayed version of the original p.r.b.s. needs some attention. There are three commonly used methods that have been described in the literature. One technique uses a shift register of length equal to the complete m-sequence, and the Q outputs corresponding to the required delays are selected. Another uses one standard shift register feedback system to generate the reference p.r.b.s., while the delayed versions are obtained by using additional EXCLUSIVE-OR gates, taking advantage of the "shift-and-add" property of m-sequences. The connections required to obtain all the delayed sequences may be determined by the technique described by S.H. Tsao ("Generation of delayed replicas of maximal length linear binary sequences" Proc. IEE, Vol 111, No 11, Nov. 1964, pp. 1803-1807. Also a useful discussion on this paper is to be found in Proc. IEE, Vol. 112, No 4, April 1965, pp 702-704). Using this method, however, generation of all the delayed versions of the original may require a large number of additional gates.

The third technique is of practical interest when only one delayed version of the p.r.b.s. is required at a time. Identical series are generated by two similarly connected feedback shift registers and by suppressing one clock pulse to one or other shift register, sequences with one clock pulse delay between them are generated. The circuit diagram of the system shown in Figure 35 is a cross-correlator using the latter technique to obtain the delayed p.r.b.s. The two generators are synchronized by starting both shift registers at the all-zero state (permitted, since the feedback is EXCLUSIVE-NOR). Each time the RETARD button is pressed, the two interconnected D-type flip-flops cause one complete



Fig. 35 P.R.B.S. CROSS-CORRELATOR FOR MEASURING THE IMPULSE RESPONSE OF A LINEAR NETWORK

clock pulse to be removed from the (otherwise continuous) series of pulses driving the first p.r.b.s. generator. The series produced by this is then used to control the input stimulus for the circuit under test. For this particular circuit, the stimulus is a voltage, $U/2$, which is alternately switched positive and negative with two analog switches (1/2MC 14016) by the delayed p.r.b.s.

The output voltage from the test circuit is now demodulated with two analog switches (1/2MC 14016) driven by the reference p.r.b.s. Processing this switched waveform by means of an integrator, whose time constant is much longer than the clock period, will give an output voltage level representative of the correlation for that particular delay between the two p.r.b.s. The entire cross-correlation function (i.e. the impulse response of the circuit under test) can then be obtained by advancing the second p.r.b.s. with respect to the first one, one step at a time, until all the steps in a complete cycle have been made.

4. CONCLUSIONS

The information provided here has been intended primarily to introduce the simplified mathematical background necessary for understanding p.r.b.s. In addition, techniques have been shown for generating such series with shift registers and EXCLUSIVE-OR gates using CMOS devices.

Owing to the extremely varied fields in which p.r.b.s. may be found, it is impossible here to present detailed discussions for all applications. However, as can be seen from the two examples included here, once the basic p.r.b.s. has been generated, the remaining problems are typical of those found in most digital system designs.

F MEDICAL APPLICATIONS

The aim of the designer of modern medical electronic equipment is to perform the required measurement with complete safety and minimum possible disturbance to the patient. This leads to the concept of battery-powered personalised portable units which are entirely self-contained. The availability of small components with very low power consumption is therefore a factor of prime importance in the design of such equipment.

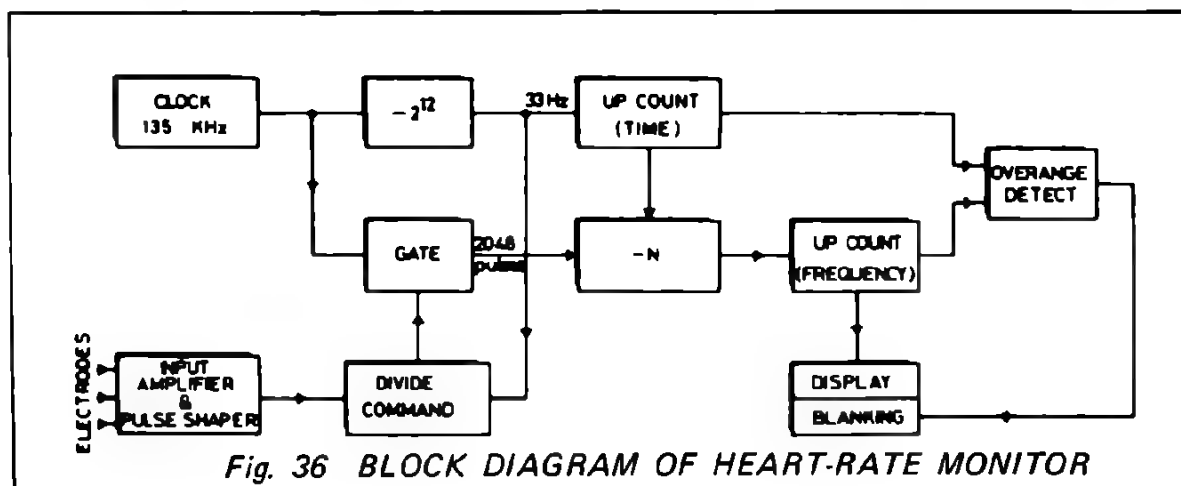
1. A PERSONALISED HEART-RATE MONITOR WITH DIGITAL READOUT

1. 1. INTRODUCTION

The heart-rate monitor described here features the use of the low power operational amplifier MC 1776 for analog processing and CMOS integrated circuit devices for all the logic functions.

1. 2. DESIGN CONCEPT

In designing this equipment, the problems associated with small, battery-operated, self-portable medical monitoring units were considered. In particular, this equipment is required to present a continuous optical display of the heart-rate as a 3-digit number to the wearer. A direct indication is provided, beat-by-beat, giving an accuracy better than $\pm 5\%$ under all real-life situations and environmental conditions. The system block diagram is shown in Figure 36.



The basis of the system is the extraction of the cardiac rhythm present in the electrocardiogram, using this then to calculate the number of beats per minute of the heart.

In order to obtain clean, artifact free, ECG signals, conventional electrodes are attached to the sternum of the patient. Figure 37 shows a stylised version of a typical ECG waveform, obtained using such an electrode configuration, with the salient features identified according to the usual nomenclature.

Fig. 37 SALIENT FEATURES OF THE ECG

Since the form of the ECG pattern may change from one beat to the next, an unambiguous identification of any individual feature may require pattern recognition procedures. However, the R-wave is always the largest amplitude signal present for the vast majority of patients, so in practice, the time interval between beats can be obtained on the basis of a simple amplitude discrimination. The classical process of counting the number of oscillations of a stable clock during the R-R intervals is employed for the time measurement. The heart-rate (in beats per minute) can then be calculated digitally, dividing a fixed number of pulses (2048) by the number corresponding to the time interval. The resulting number of pulses is then available for display as a three digit number, in this case using seven-segment light emitting diode arrays.

3. CIRCUIT DESCRIPTION

The complete circuit diagram employed to realise the heart-rate monitor is shown in Figure 45, and this is now considered in detail. Starting with the analog part of the unit, a high impedance differential operational amplifier (MC 1776) is used to raise the detected ECG voltage from the millivolt range to the order of volts, as shown in Figure 38.

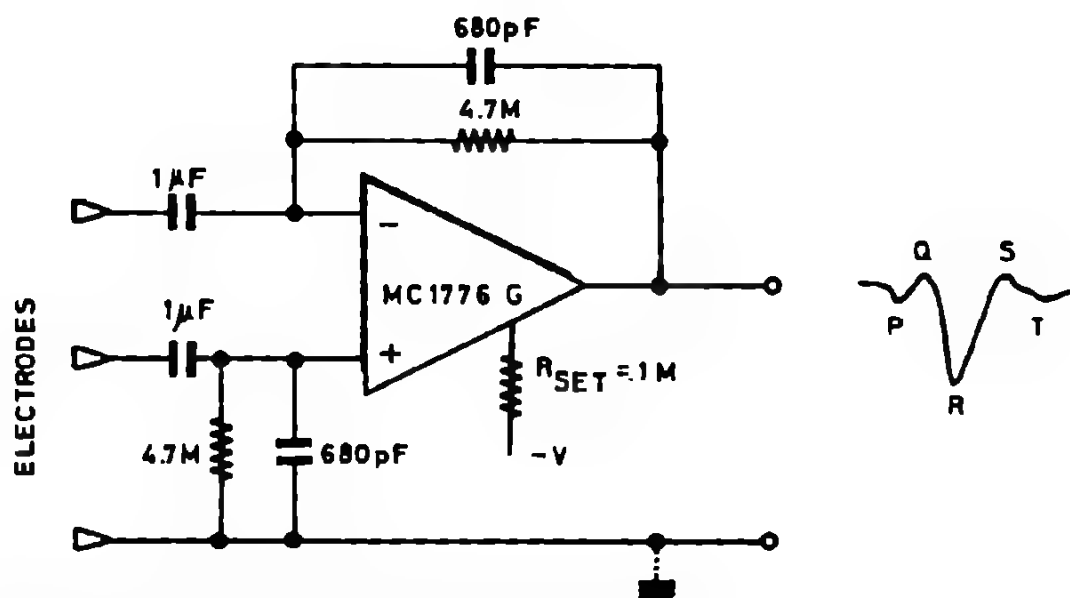


Fig. 38 INPUT AMPLIFIER CIRCUIT

With respect to ground, the electrodes may have a considerable common mode d.c. voltage, picked up by the patient from the environmental electromagnetic and electrostatic fields. For this reason, provision is made to use three electrodes, the additional one serving for the ground connection. This permits the common-mode rejection characteristics of the circuit to be retained, even when connection is made to other externally grounded equipment. The electrodes are capacitively coupled to the amplifier to eliminate amplification of d.c. changes at the skin/electrode interfaces. The final low-pass circuit configuration, used to reduce high frequency noise, results in an amplification of the ECG to about 1 volt in the frequency range of 1-100Hz.

It was pointed out earlier that the R-wave can be extracted from the ECG by amplitude discrimination. This function is performed in practice by a CMOS inverter with off-centre biasing. As shown in Figure 39, a variable resistor allows the threshold to be adjusted to the desired level.

The output of this shaping circuit is a pulse corresponding to the R-wave and of suitable amplitude to drive the CMOS logic time measuring circuits which follow.

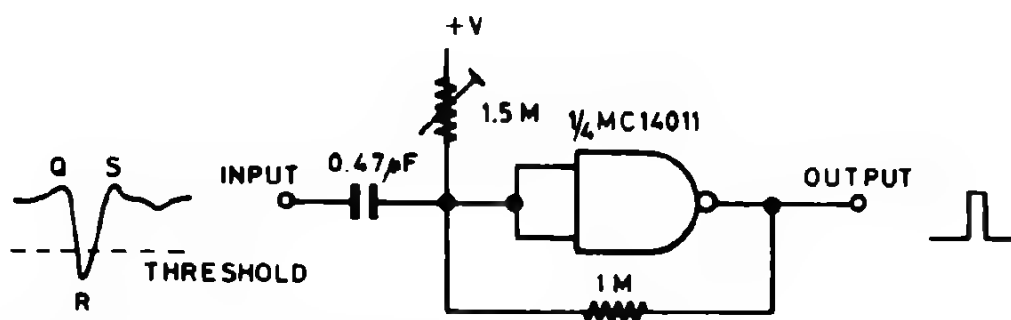


Fig. 39 PULSE SHAPING BY CMOS INVERTER

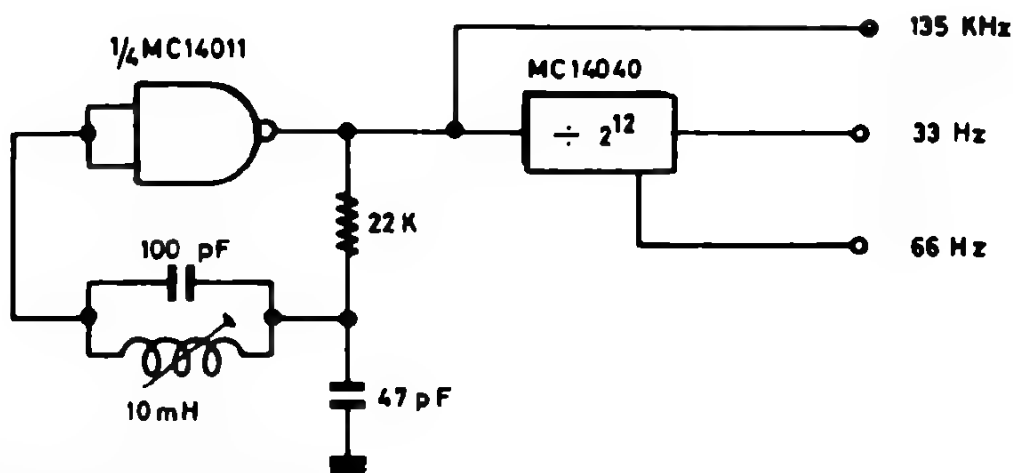
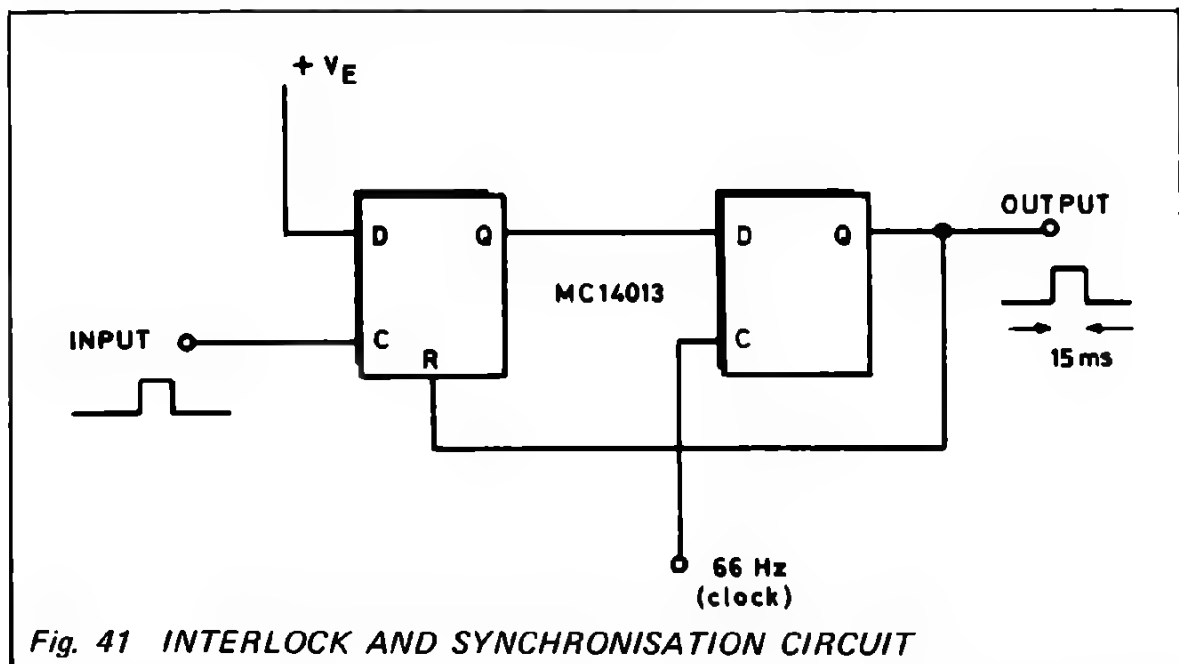


Fig. 40 STABLE CLOCK

A stable clock is required for accurate time interval measurements. In this case, a frequency of 135 kHz is chosen, and, for reasons which will become evident later, it is divided down to 33Hz (using a MC 14040) as shown in Figure 40. The frequency is determined by the resonant LC circuit, which provides a sufficiently stable and precise waveform for this application.

In order to eliminate multiple triggering of the measuring circuit, which may occur due to the width of the R-wave pulse, an interlock circuit is required, synchronised from the clock. The circuit in Figure 41 shows how two D-type flip-flops (MC 14013) are used to perform this function. When an R-wave is detected, the resulting output is a pulse 15 milliseconds wide, synchronised with the clock. The output of the interlock circuit is in fact used to initiate both the timing and the calculation circuits. Referring to the diagram in Figure 45, the action of the circuit can be followed.



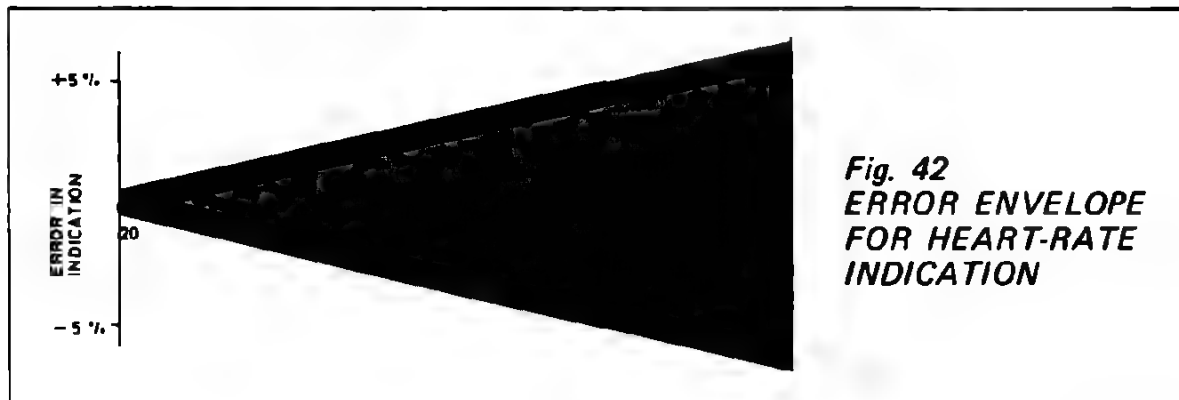
While the interlock circuit output is low, pulses from the clock at 33 Hz continuously enter the 2-decade BCD up-counter (MC 14518). The content of this counter is applied to the data inputs of the divide-by-N circuit (two MC 14522) which is inhibited in this condition.

When the interlock circuit output goes high, the divide-by-N input, which is connected to the 135 kHz clock, is enabled for 15 milliseconds (i.e. 2048 pulses are entered). The output pulses are totalised in another 2 1/2 BCD up-counter, giving directly, with these values, an equivalent number of detected R-waves per minute. Decoding of this BCD number to drive three 7-segment LED displays is then performed by three MC 14511 blocks.

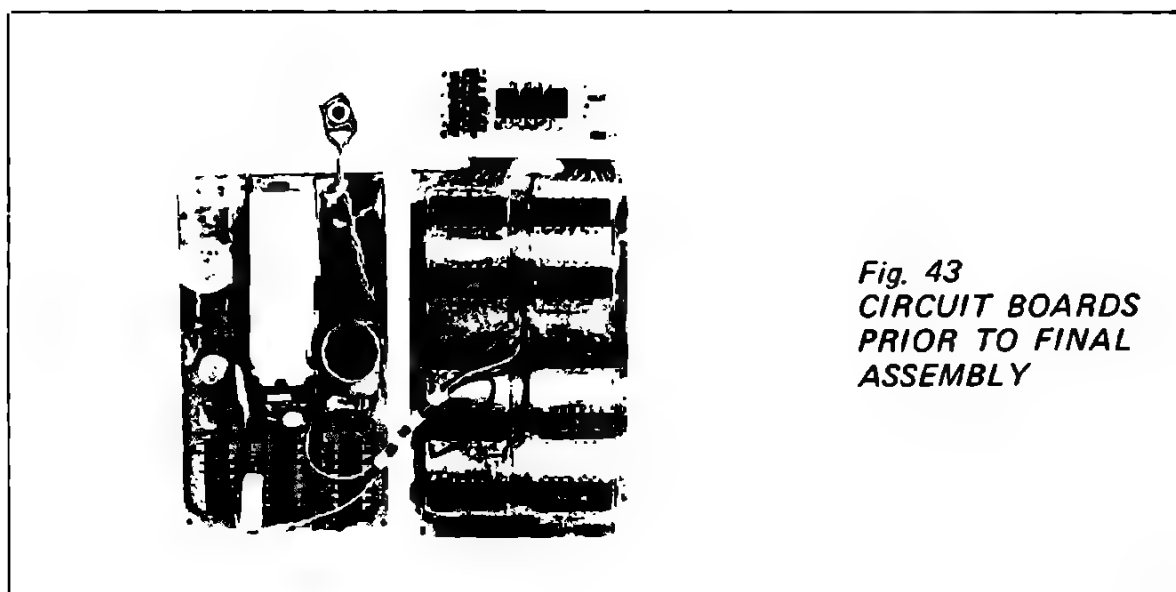
As the interlock circuit output returns to a low state, following the calculation, a 1μS pulse is generated, which is used to reset both up-counters, after the display drivers have been latched to hold the value just calculated. An over-range circuit is included which automatically blanks out the display if either the period or the frequency up-counters overflow (i.e. if the detected heart-rate falls outside the range 20-200 beats per minute). A latching flip-flop is used after the counter overflow detector (MC 14013) to hold the display blanked until a valid input is obtained.

1. 4. CIRCUIT PERFORMANCE

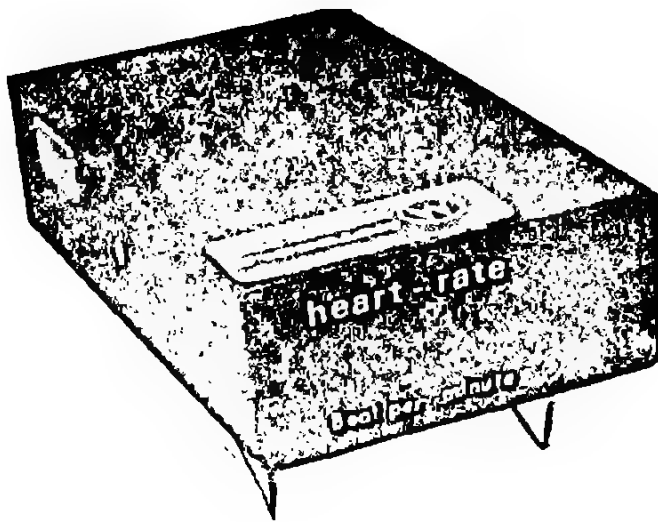
Since the measurement and calculation of heart-rate is performed digitally, there will be a quantisation error involved. In practice, this corresponds to the waiting time for clock synchronisation during the time measurement process. The largest errors in the display will occur then, when short times are measured (i.e. at rapid heart-rates, near the limit 200 beats/minute) and will amount to a maximum of $\pm 5\%$, as shown in Figure 42.



The equipment is powered by a triple mercury cell battery providing 4.05 volts at a rating of 1 amp. hour. The power consumption of the unit, with the display blanked, is about 600 microwatts, which should result in a lifetime of about a year for the battery. However, when working normally (heart-rate between 20–200 beats/minute) the power consumption will actually be around 250 milliwatts depending on the figures lit up in the display. Probably the practical lifetime of the battery, using the LED display, will be about one day of continuous use. There is no ON/OFF switch included in the circuit, since a simple disconnection of the electrodes will cause the display to be blanked out, there-



by reverting to the very low current drain condition. The interest in using new lower power-drain techniques for digital display is self-evident. To realise the unit described here, a total of 13 CMOS blocks and one MC 1776 operational amplifier are used as the active elements. The three circuit boards for the ECG signal processing, the digital processing and the opto-electronic readout are shown in Figure 43 before final assembly.



*Fig. 44
COMPLETED HEART-
RATE MONITOR*

The completed instrument, shown in the photograph, Figure 44, is assembled in an aluminium case 105 x 60 x 25 mm, and weighs 180 grams.

1. 5. CONCLUSIONS

By using low voltage micropower linear and digital circuit elements, it has been shown that small self-portable medical monitoring equipment can be built very easily. The range of digital processing functions which are now available in CMOS technology indicate that, apart from simply monitoring the R-wave of the ECG, much more complex measurements could be undertaken.

Of especial interest is the possibility of miniaturising this design. This is feasible if the battery size can be reduced, as could be achieved by using a different optical display, since then the size of the unit would be governed mainly by the problems of making connection to the component parts.

Apart from numerous applications in bio-medical monitoring, this class of personalised instrument introduces the interesting concept of practical human bio-feedback systems, which could prove to be a very powerful technique in medical treatment.

ECG SIGNAL PROCESSING

HEART-RATE CALCULATION

OVERFLOW

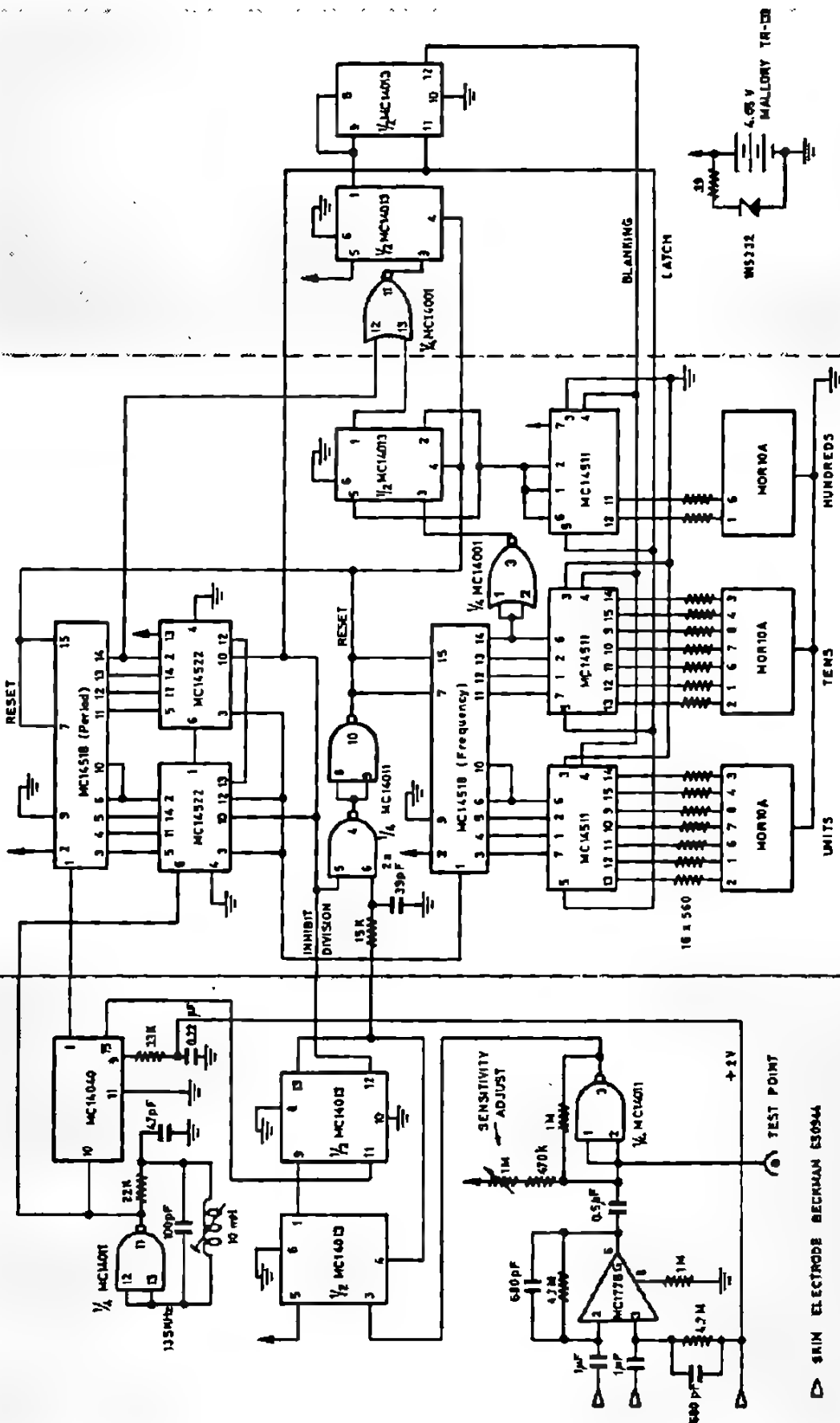


Fig. 10 Circuit diagram of the Heart-rate Monitor

▷ SKIN ELECTRODE BECKMAN ES0944

2. A DIGITAL CLINICAL THERMOMETER USING CMOS

2.1 INTRODUCTION

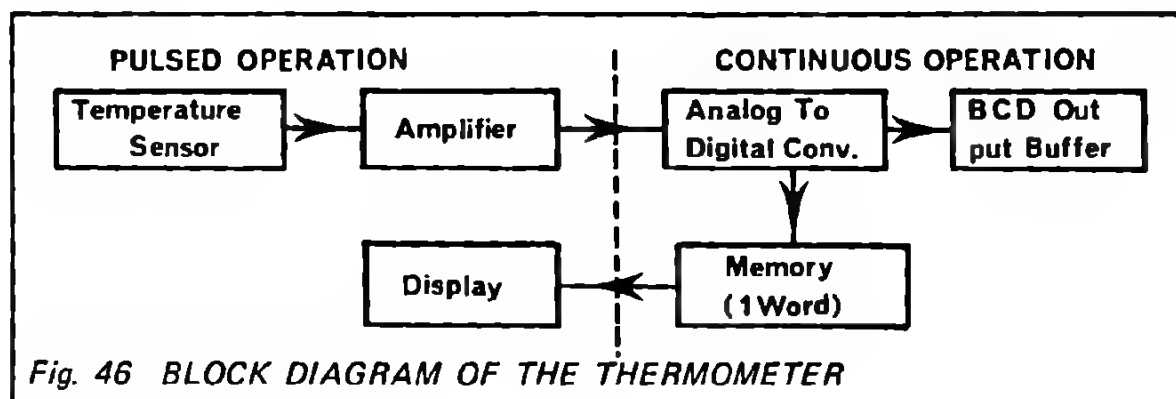
One of the more important parameters used in judging a person's state of health is his body temperature. Conventionally this is obtained by using a mercury-in-glass thermometer, an accurate instrument, but with the disadvantages of having an inherently long time response (and reset time) and also the possibility of errors in reading from the analog scale.

The digital thermometer described here is intended to minimize these problems and still result in a small hand-held instrument, operating from internal low-voltage dry-cell batteries.

2.2 DESIGN CONCEPT

The basic principle used for the temperature sensing probe, is the measurement of the base-emitter voltage of a silicon PNP transistor, held in contact with the skin. Since the voltage varies in a linear fashion with temperature, a 2 1/2 digit B.C.D. analog to digital converter with suitable scaling may be used to provide a direct digital readout of the temperature within 0.1°C.

To reduce the power consumption (so as not to drain the batteries unnecessarily), when in use, the display works in a pulsed mode — 1 second ON, 3 seconds OFF. However, since low power consumption CMOS logic is used, continuously running logic circuits provide the facility for memorizing and also for recalling the previous measurement, even after the unit has been switched off. The block diagram (Fig. 46) shows also that other external digital equipment (display systems, printers, etc.) may be connected by using the buffered B.C.D. output provided.



2.3 CIRCUIT DETAILS

A complete circuit diagram of the instrument is presented in Figure 53, details of which will now be enlarged upon.

The Sensor and input amplifier:

The PNP transistor (2N 3307), which serves as the temperature sensor, is connected in a simple grounded base configuration, as shown below in Figure 47.

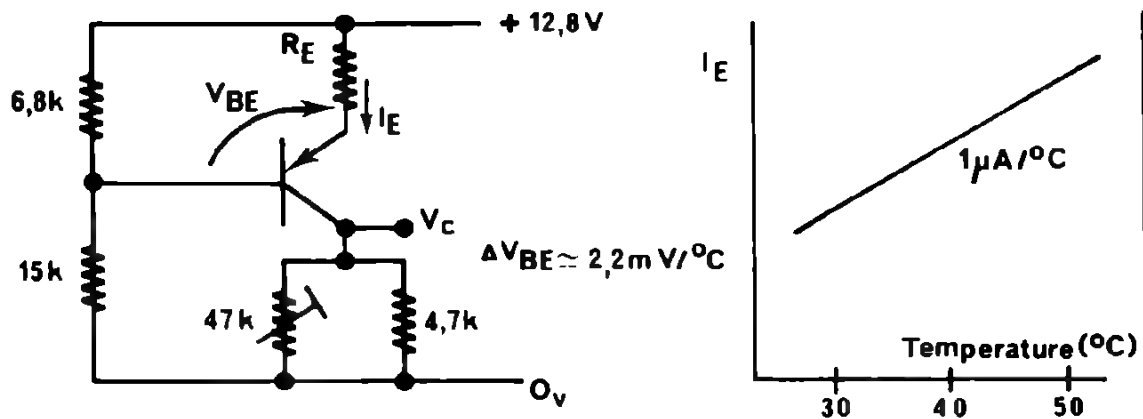


Fig. 47 TEMPERATURE SENSING CIRCUIT

As V_{BE} changes (linearly with temperature) then I_E and V_C vary. For 1°C change in temperature

$$\Delta V_{BE} = 2.2 \text{ mV},$$

and choosing the emitter resistor, R_E , appropriately ($2.2 \text{ k}\Omega$)

$$\Delta I_E = \frac{\Delta V_{BE}}{R_E} = 1 \mu\text{A}.$$

With the temperature at 30°C , the $47 \text{ k}\Omega$ trimming potentiometer is used to adjust the value of V_C to 5.30 volts, the reference voltage for the differential input amplifier which follows. This amplifier ($1/2 \text{ MC } 1558$) serves to transform the current change of $1 \mu\text{A}/^\circ\text{C}$ into a voltage change of $-100 \text{ mV}/^\circ\text{C}$ by means of the circuit below (Fig. 48).

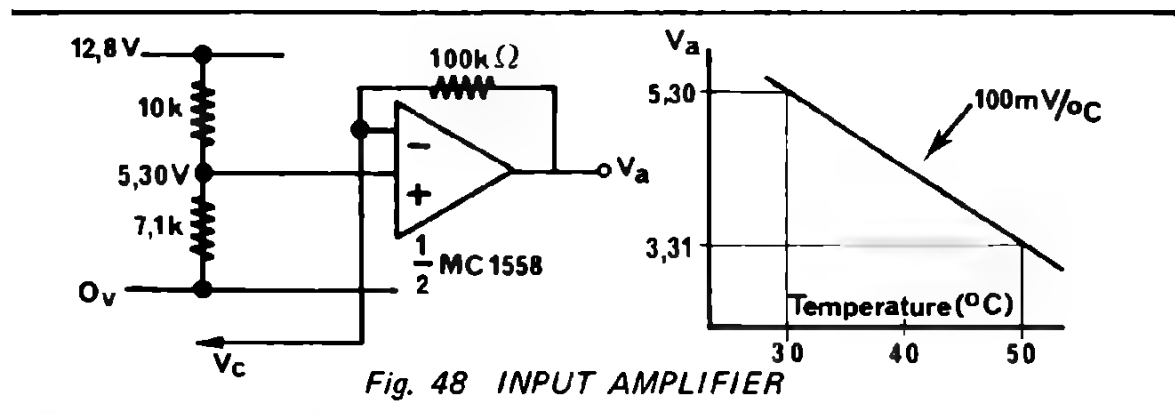


Fig. 48 INPUT AMPLIFIER

The analog to digital converter:

A $2^{1/2}$ digit B.C.D. tracking analog to digital converter, Figure 49, is used to convert V_a , the output voltage (5.30 to 3.31 volts), into digital form for display (30.0 to 49.9°C). The conversion is made by virtue of a digital to analog converter of the resistor ladder network form. The converter is forced to accept the correct digital input from continuously running up/down counters (MC 14516), the value of which corresponds to the required analog level.

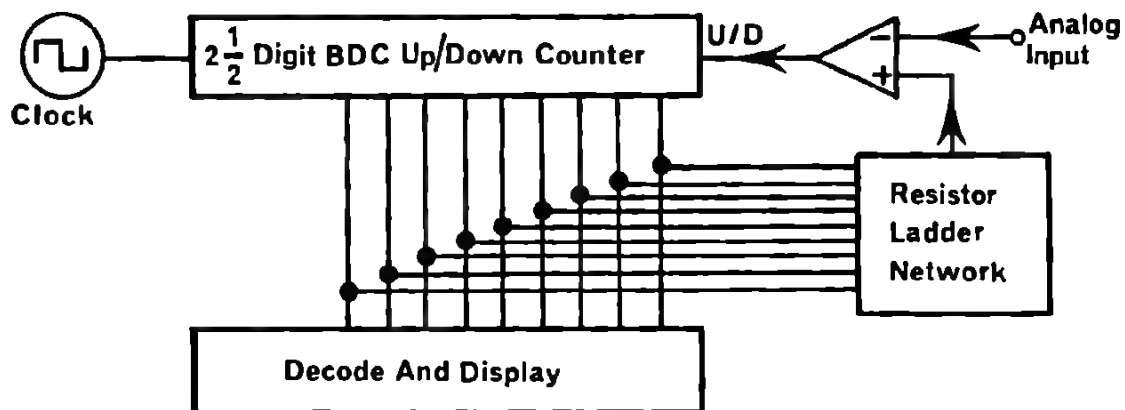


Fig. 49 TRACKING ANALOG TO DIGITAL CONVERTER

Since the output logic levels of CMOS devices are very close to the supply voltages (guaranteed to be within 10 mV), the up/down counters can be connected directly to the resistor ladder without the need for additional switches. The standard CMOS logic outputs (MC 14xxx series) have typically 750Ω impedance, so effective resistive loads exceeding $150\text{ k}\Omega$ should be employed if output loading is not to exceed 0.5% (i.e. the equivalent of the least significant bit). Using such high values implies a slow operating speed, owing to the circuit capacitances. This results in a switching time longer than $10\mu\text{s}$ (clock rate less than 100 kHz) and makes the conversion rate probably fall below 1 kHz. The resistor network is basically an $R - 2R$ ladder for each (4-bit) decade, from which a complete B.C.D. digital to analog converter is assembled using resistors of values shown in the diagram below (Fig. 50).

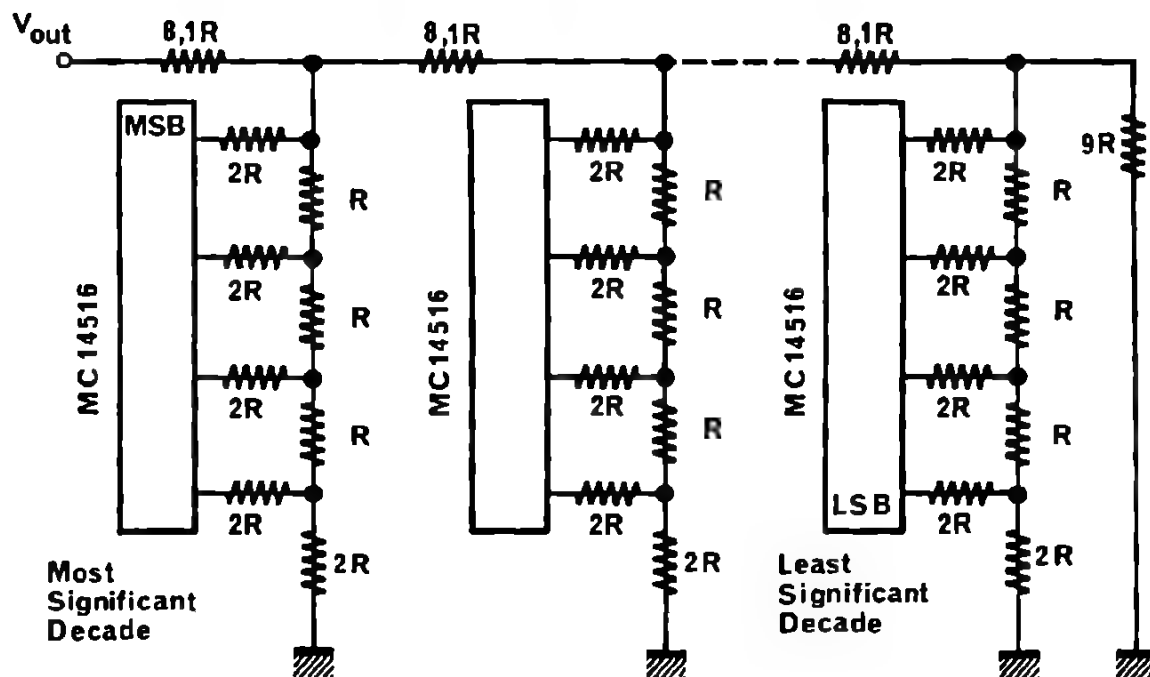


Fig. 50 B.C.D. LADDER NETWORK

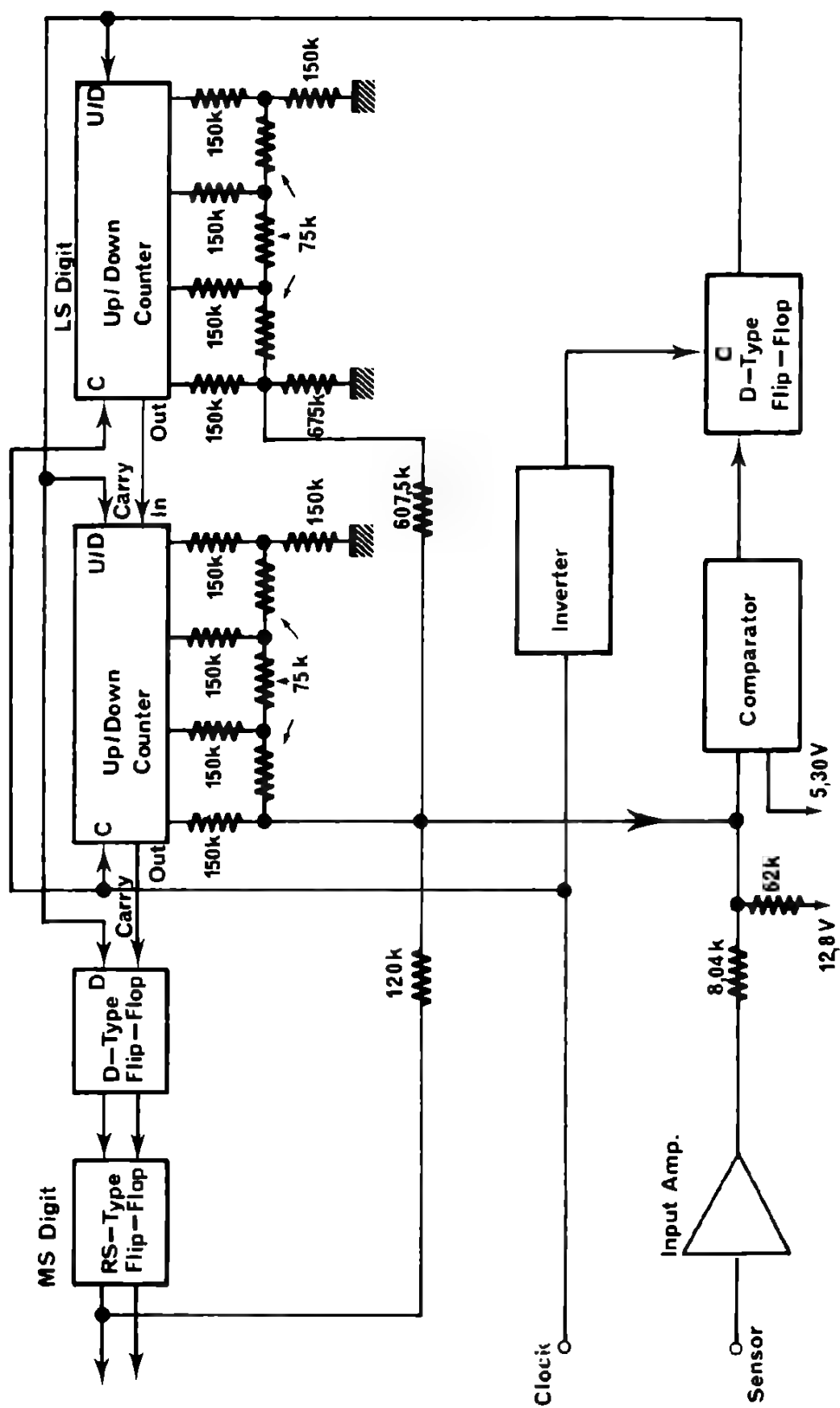
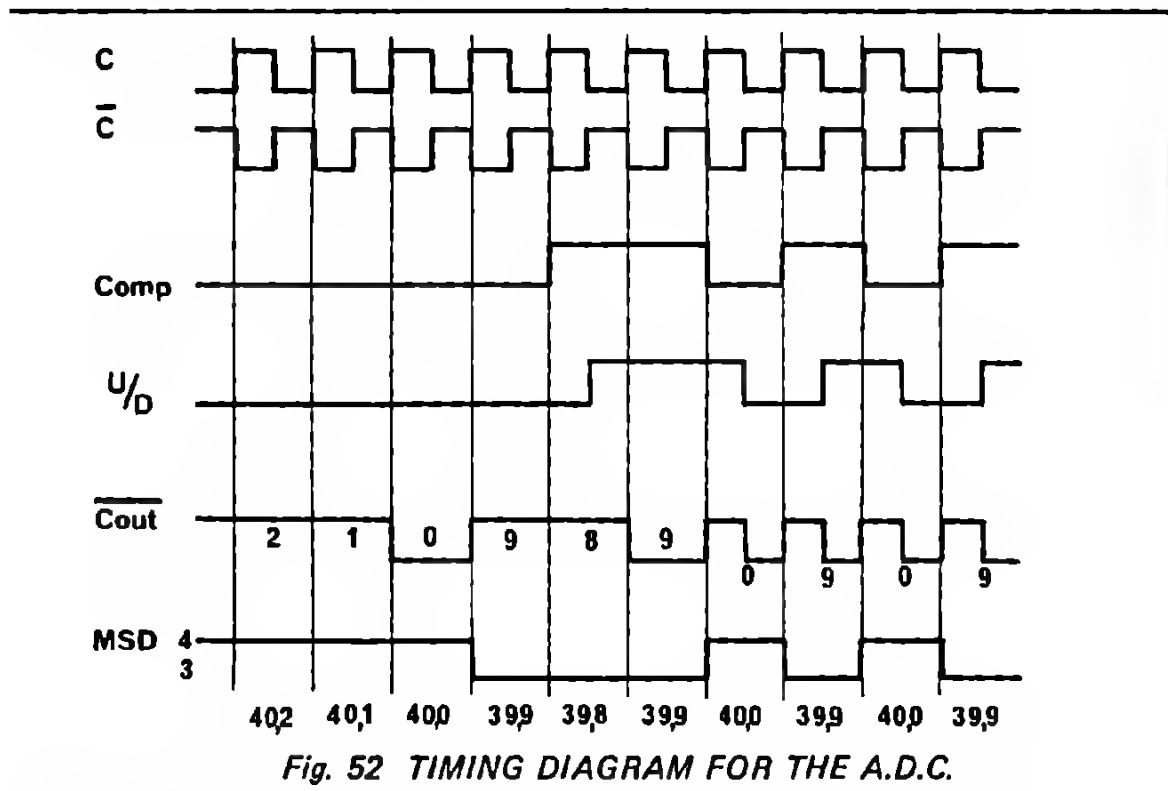


Fig. 51 BLOCK DIAGRAM OF THE 2 1/2 DIGIT B.C.D. ANALOG TO DIGITAL CONVERTER

In this case R was chosen to be $75\text{ k}\Omega$, giving $2R = 150\text{ k}\Omega$; $8.1 R = 607.5\text{ k}\Omega$; $10R = 675\text{ k}\Omega$.

It is required to make the digital outputs 30.0 to 49.9 correspond to the analog inputs 5.30 volt to 3.31 volts respectively. This necessitates calculating the resistor values to the summing point of the comparator, to give the correct polarity and full-scale end points. The results are as shown in Figure 51.

The digital counters are continuously driven MC 14518's, with the direction of count specified by the level of the U/D input. In this circuit the U/D command is made by the comparator, so that when balance is achieved between the analog input from the probe and the analog output from the D/A converter, the U/D command changes every second clock pulse, the MC 14518's oscillating between two adjacent digital numbers. Since the most significant digit is either the figure 1 or 4 there is no need for a complete decade counter for this, a D-type flip-flop is used instead. A block diagram of the counting system is shown in Figure 51, and an appropriate timing diagram in Figure 52.



4. DISPLAY

The major power drain on the batteries is due to the LED display. For this reason, when in use, the display is switched on for only one second in every four. When the display is on, the contents are latched to prevent readout flicker.

Decoding of the B.C.D. contents of the MC 14516s into 7-segment format for the LEDs is provided by the MC 14511s. Since only the figures 3 or 4 need to be displayed from the state of the D-flip-flop, no decoding is necessary and the drive current is obtained by using discrete components. In this unit the latching and blanking functions of the MC 14511 are needed; for the most significant digit, a

clocked R – S flip-flop is used to perform these functions.

When the instrument is switched off, all the logic circuits continue working except the display decoders, which are held in the latched condition, but with power for the LEDs disconnected. In this state, pushing the MEMORY button will re-connect the LEDs supply and allow the last latched value of the D/A converter to be re-called and displayed.

The state of the counters in the D/A converter can be obtained at any time from the B.C.D. output terminals which are connected to them via a buffer (MC 14010). This output represents the temperature, but only when the analog to digital converter is within its working range.

Out-of-range circuit:

When the analog to digital converter is within its working range, the U/D command will be switching regularly (at half the clock rate) between high and low states.

An indication as to whether this condition is present is easily obtained from the U/D command line. If this spends more time in one state than in the other, the mean d-c voltage, determined by integration, will tend towards the level of the supply voltage lines. A simple level detector then will show when the feedback has not been able to balance the system and therefore when the figures presented on the display are incorrect. This condition triggers an alarm LED showing that the temperature lies outside the range of the instrument.

2. 5. PERFORMANCE

The resolution of the digital/analog converter is 1 : 200 and with the scaling resistors set correctly, one step corresponds to 0.1°C.

All circuit components affecting the measurement have been selected so that normal variation in their values will not cause an equivalent change of more than 0.1°C of the display.

The power is supplied from two mercury cell batteries (Mallory TR-165R) of 6.75V each and a stabilized 12.8V is derived from these by mean of a zener diode. The power consumption is

- | | | |
|----|---------------------------|---------|
| a) | Analog processing circuit | 35 mW |
| b) | CMOS logic | 0.45 mW |
| c) | LED displays | 200 mW |

The batteries have a capacity of 0.5 amp.hour and it could therefore be expected then under normal operating condition of say 100 measurements per day, each taking 20 seconds to complete, that the instrument may be used for some 2 months before the batteries will require changing.

S	R	R	S	Q
AC1403				
D	C	C	Q	Q

Timepiece
Electronics

TIMEPIECE ELECTRONICS

A ELECTRONIC QUARTZ TIMEPIECE SYSTEMS

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 2. 4. TRIMMER CAPACITOR
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A ELECTRONIC QUARTZ TIMEPIECE SYSTEMS

I. GENERAL

An electronic quartz timepiece system consists of a quartz crystal controlled time-reference, an electronic divider circuit, an output stage to interface with a time display system (motor driven or fully electronic) and a power supply (Fig. 1).

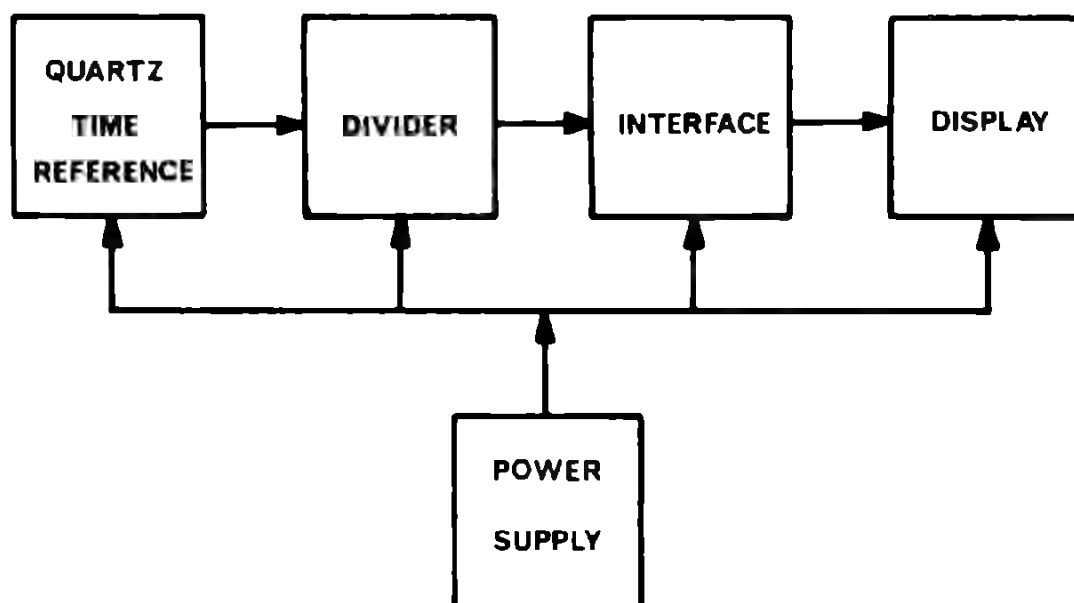


Fig. 1 ELECTRONIC QUARTZ TIMEPIECE SYSTEM

Modern technologies in the fabrication of integrated circuits, quartz crystals and micro miniature motors make it possible to build timepiece systems which are compatible with the severe requirements in wristwatches, such as low voltage, low current consumption, small physical dimensions, high reliability and low price.

It is most important that the individual components are specified with great care within the system boundary conditions, so that no difficulties arise in the interface areas between crystal and IC, and between IC and motor.

From this, and in the light of systems which are to be produced in high volume, the advantages of a fully compatible set of components are evident.

2. COMPONENTS

2. 1. QUARTZ CRYSTALS

The piezoelectric effect:

Some crystals develop, when subjected to mechanical pressure, electrical charges on their surfaces. This is called the piezoelectric effect, and it can be observed particularly well on quartz crystals. It was verified by Jacques and Pierre Curie in 1880.

The piezoelectric effect is reversible, i.e. an electric potential, applied across the crystal, will cause mechanical deformations in the crystal.

Therefore, when a crystal is subjected to alternating electrical charges, it will maintain its mechanical oscillations, and this at a very precise frequency.

These properties make the quartz crystal well suited as the resonating element of precise timepieces.

Crystal cuts:

Depending on the required performances, a crystal is cut to specific angles with respect to its natural crystal axes. Figure 2 shows the useful frequency ranges for given cuts.

NAME OF CUT	MODE OF VIBRATION	FREQUENCY RANGE [kHz]
5°X	LENGTH-WIDTH FLEXURE	10 TO 50
N T	LENGTH- WIDTH FLEXURE	4 TO 150
D T	FACE - SHEAR	60 TO 500
A T	THICKNESS - SHEAR	500 TO 125'000

Fig. 2 FREQUENCY RANGES FOR VARIOUS CRYSTAL CUTS

Every cut has its specific temperature characteristic. A comparison between an NT cut, DT cut and AT cut characteristic is given in Figure 3.

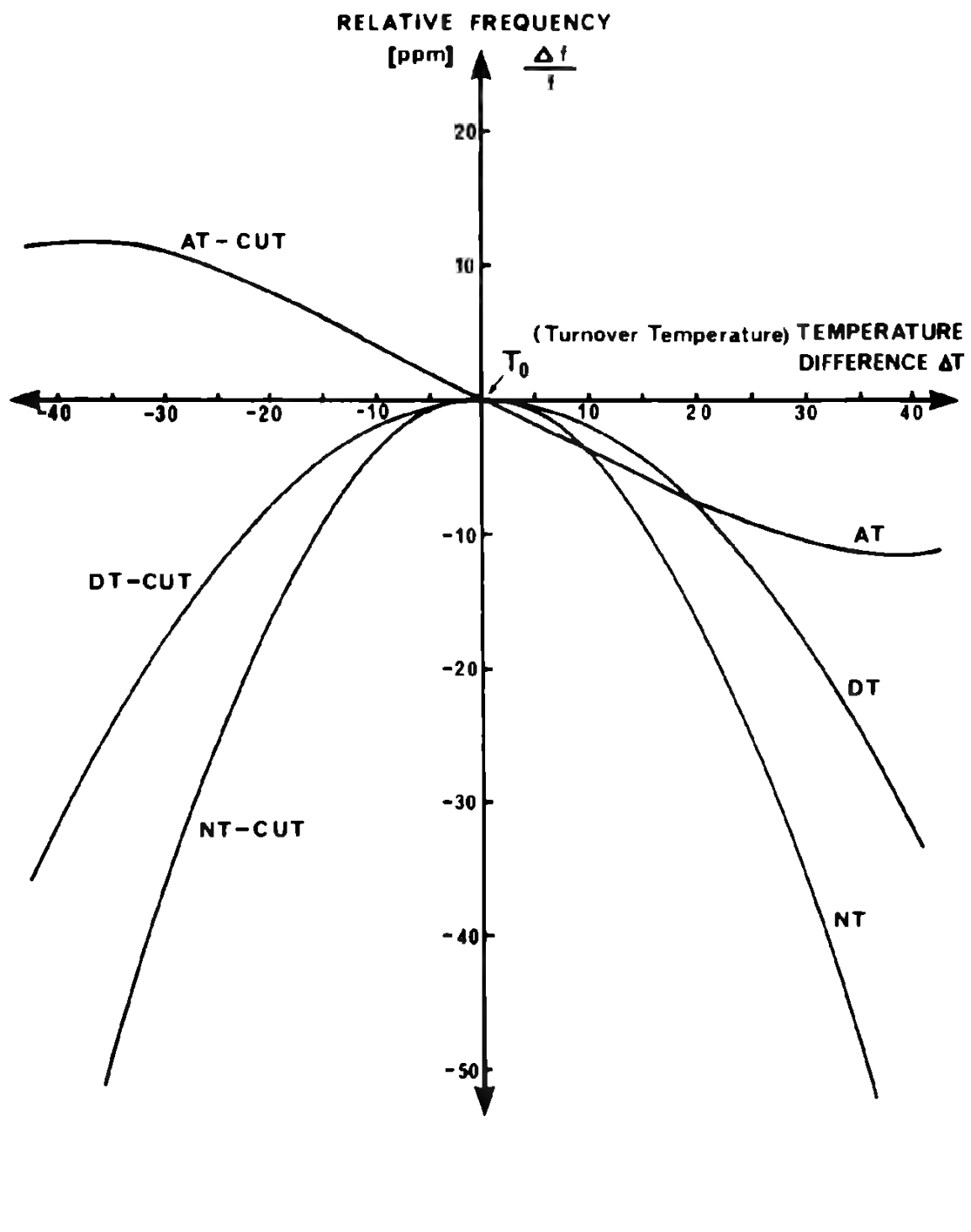


Fig. 3
TYPICAL TEMPERATURE CHARACTERISTICS OF NT, DT AND AT CUTS

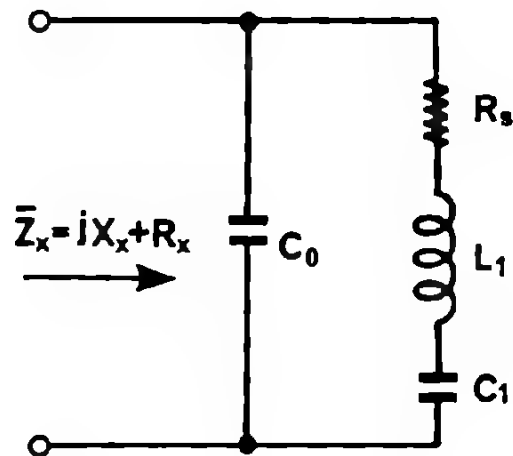


Fig. 4 EQUIVALENT CIRCUIT
DIAGRAM OF A
QUARTZ CRYSTAL

The quality factor Q is defined as

$$Q = \frac{2\pi f_s L_1}{R_s}$$

Q is proportional to the motional inductance L_1 and inversely proportional to the series resistance R_s and the motional capacitance C_1 . It is the very high value of L_1 and the very low value of C_1 in quartz crystals so useful in accurate oscillators. At series resonance frequency, the crystal reacts with a

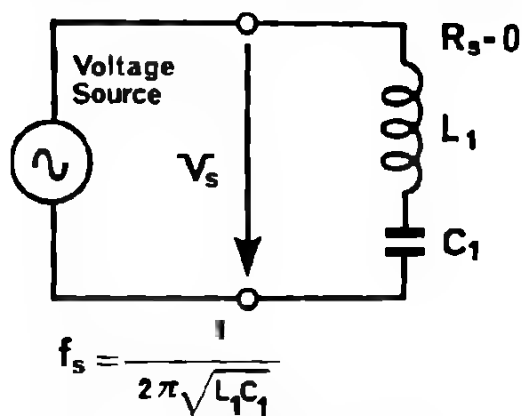


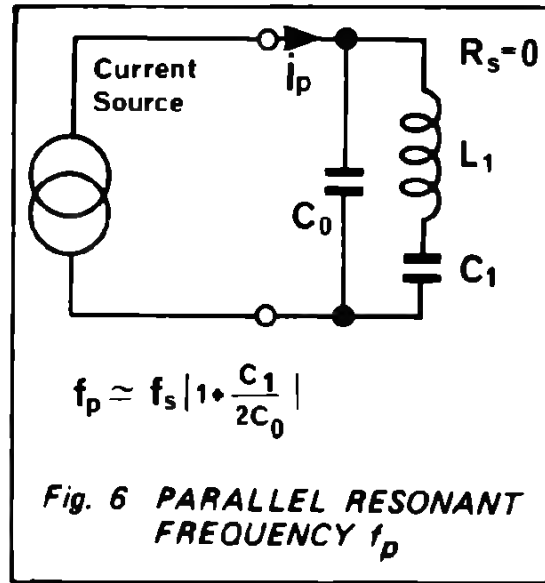
Fig. 5 SERIES RESONANT
FREQUENCY f_s

parallel resonant frequency f_p .
If in turn the crystal is driven by an ideal current source (infinite impedance), it will oscillate at its parallel resonant frequency f_p (see Fig. 6).

The $\frac{C_0}{C_1}$ ratio is in the order of

000 for the MTQ32. Therefore, f_p and f_s are apart from each other by only about 500 ppm. The difference $f_p - f_s$ is referred to as the natural bandwidth.

$$\Delta f_B = f_p - f_s \approx f_s \frac{C_1}{2C_0}$$



Resonant and Antiresonant frequencies:

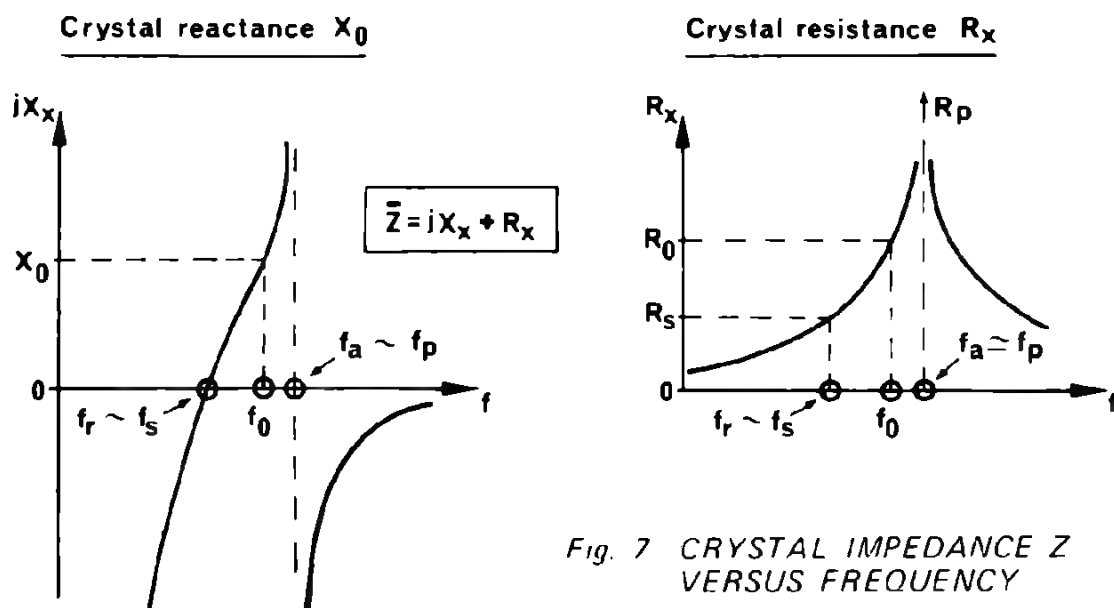
Under practical conditions, $R_S \neq 0$ and the generator impedance will have a finite value.

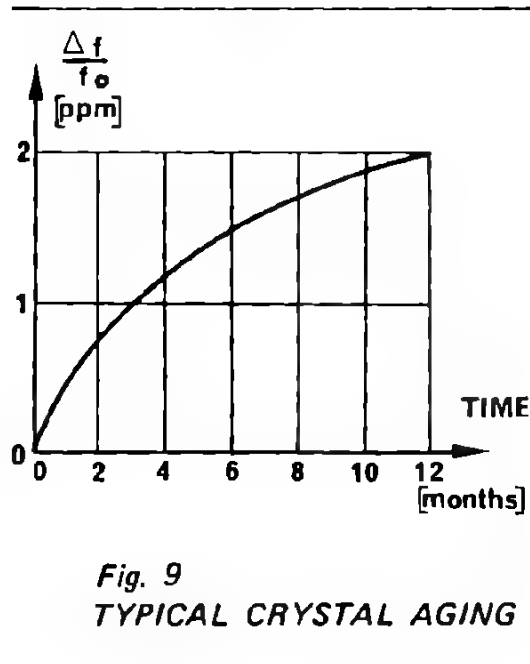
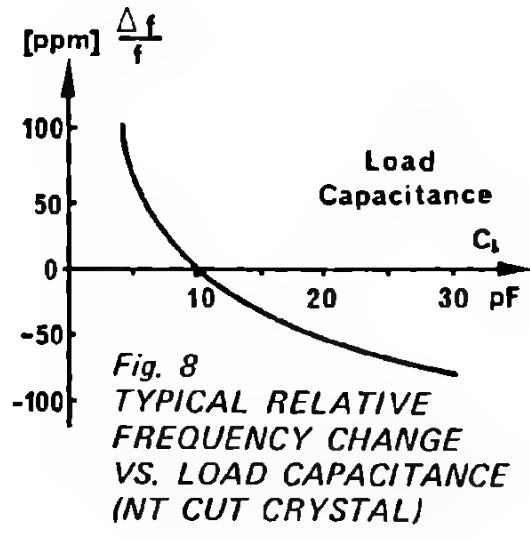
The real condition frequencies are called resonant frequency f_r and antiresonant frequency f_a .

However, f_r and f_a differ from f_s and f_p respectively by only a few parts per million, so that $f_r \approx f_s$ and $f_a \approx f_p$, for most practical considerations.

Resonant and antiresonant frequencies f_r and f_a are defined at zero and infinite crystal reactance X_x respectively (see Fig. 7).

In a practical circuit, the crystal will oscillate with a frequency f_0 between f_r and f_a . The circuits described here operate at f_0 close to f_p .







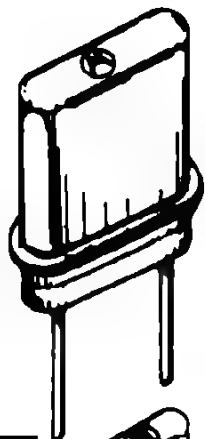

Shock:

In general, crystals will tend to reduce frequency drifts. The specific shock characteristics are for particular crystals.

As an example, the frequency drift of 1000g of 0.4ms duration, will not be significant. The shock duration is equally important. Total shock energy is a function of both amplitude and duration.

Summary of MOTOROLA's Timepiece crystals:
Figure 10 shows a summary of present MOTOROLA Timepiece crystals,
with their main specifications.

Fig. 10 SUMMARY OF MOTOROLA'S TIMEPIECE CRYSTALS

Dev. Type Number	Frequency (KHz)	Cut	Typical Temp. Coeff. (ppm/ °C°)	Preferred I.C	Max L	Dim (mm) H W	Package style
MTQ32	32.768	NT	-0.04	MTD130/131F MTD160/161F	18.8	4.2 3.3	
MTQ131	131.072	NT	-0.04	MTD180/181F	10.4	4.2 3.3	
MTQ245	245.760	DT	-0.02	MTD132P MTD134P	19.6	20.0 9.3	
MTQ262	262.144	DT	-0.02	MTD132P MTD134P	19.6	20.0 9.3	
MTQ279	279.620267	DT	-0.02	MTD132P MTD134P	19.6	20.0	
MTQ327	327.680	DT	-0.02	MTD132P MTD134P	19.6	20.0 9.3	
MTQ409	409.000	DT	-0.02	MTD132P MTD134P	11.4	11.4 5.1	

2. 2. INTEGRATED CIRCUITS

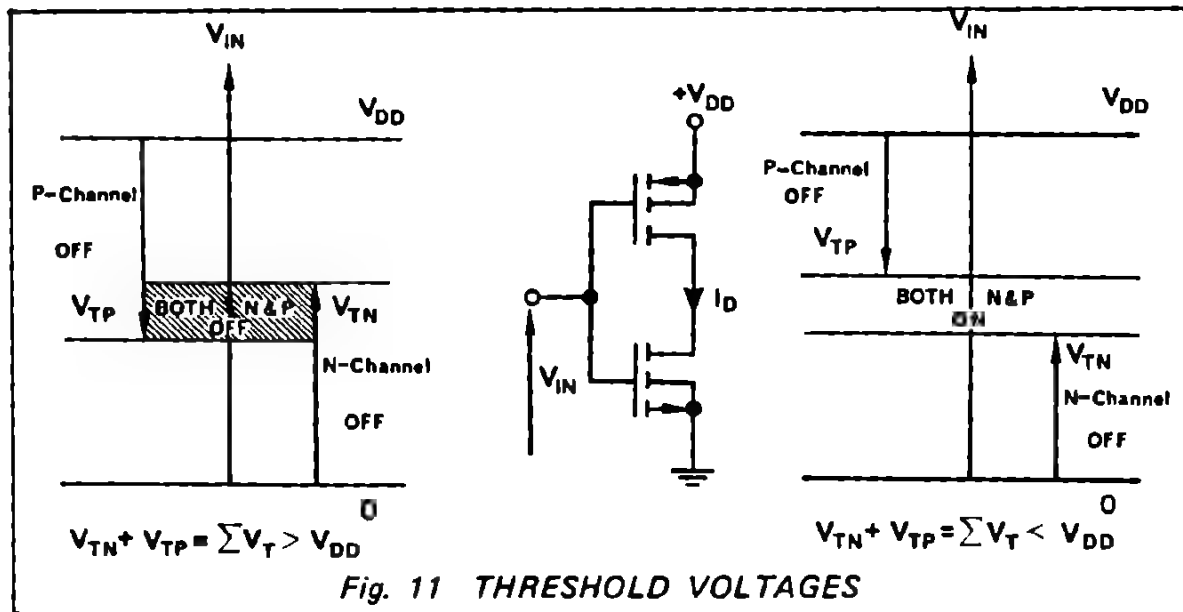
Technology:

All MOTOROLA timepiece integrated circuits (ICs) are fabricated in the Silicon Gate Complementary MOS technology.

Although not necessary from a performance standpoint, the Ion Implantation process is used in addition to improve production yields.

The major advantage of the Silicon Gate technology, over the conventional CMOS technology is its ability to reduce the threshold voltage V_T of the MOS transistors enough to allow operation of the ICs at very low supply voltages (1.35V or 1.5V).

With the Silicon Gate technology, threshold voltages are not a limiting factor.



Threshold voltage (see Fig. 11):
 The MOTOROLA timepiece circuits operate in a mode, where the sum of the n-channel threshold voltage V_{TN} plus the p-channel threshold voltage V_{TP} is typically larger than the supply voltage V_{DD} .

$$\Sigma V_T = V_{TP} + V_{TN} \quad \Sigma V_T > V_{DD}$$

For the basic circuit element, the CMOS inverter, this means that as the input voltage V_{IN} changes from 0 to $+V_{DD}$, one of the two transistors will always be off. No current will flow.

In comparison, if the condition were $\Sigma V_T < V_{DD}$, there would be a range for V_{IN} , where both transistors would conduct. Thus, an excessive current would flow.

The threshold voltage is defined here as the Gate-source voltage V_{GS} required to induce a drain current of $5 \mu A$.

Power consumption:

The dynamic consumption P_D of a CMOS inverter circuit is basically proportional to the frequency f_{IN} , to the load capacitance C_G and to the square of the supply voltage. Normally, the static power dissipation P_S is negligible, so that only P_D has to be considered.

$$P_D = f_{IN} C_G V_{DD}^2$$

Oscillator circuit
 The oscillator circuit shown in Figure 12 has proved to be an optimal solution for watch applications and many clock applications.
 It provides overall high performance:
 low power consumption
 wide frequency trimming range
 wide operating voltage and temperature range
 good frequency stability

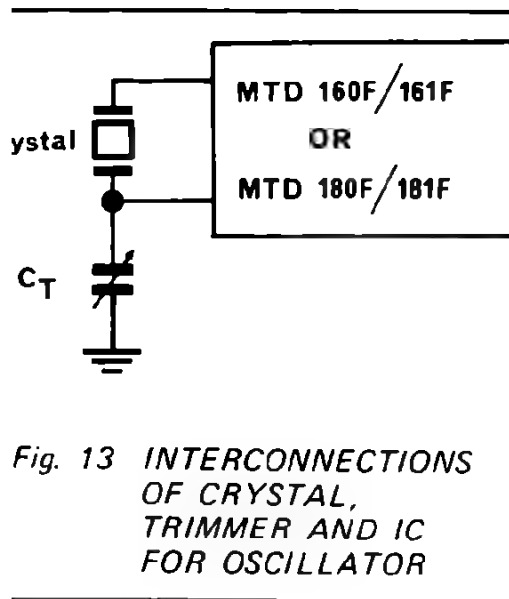


Fig. 13 INTERCONNECTIONS OF CRYSTAL, TRIMMER AND IC FOR OSCILLATOR

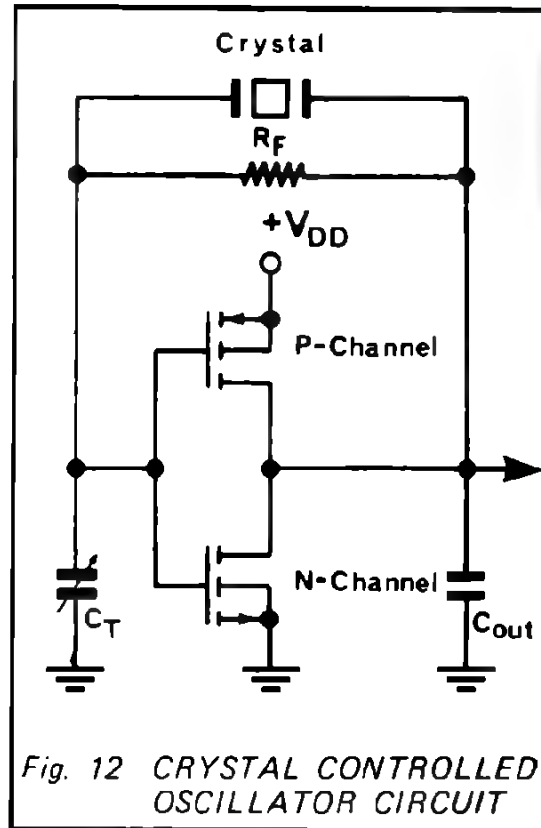


Fig. 12 CRYSTAL CONTROLLED OSCILLATOR CIRCUIT

In most MOTOROLA timepiece circuits for watches the feedback resistor R_F and the output capacitor C_{OUT} are monolithically integrated on the oscillator / divider / buffer chip. (Fig. 13).

Typical oscillator current versus frequency is shown in Figure 14.

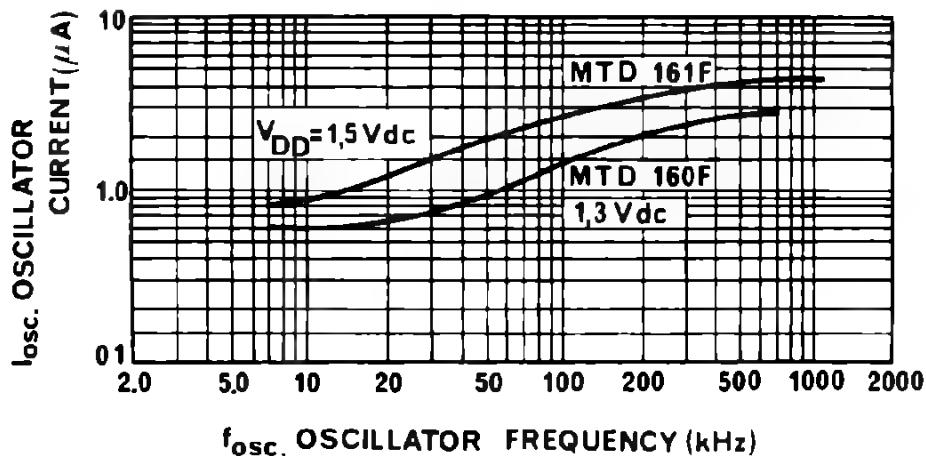


Fig. 14 TYPICAL OSCILLATOR CURRENT VS. FREQUENCY

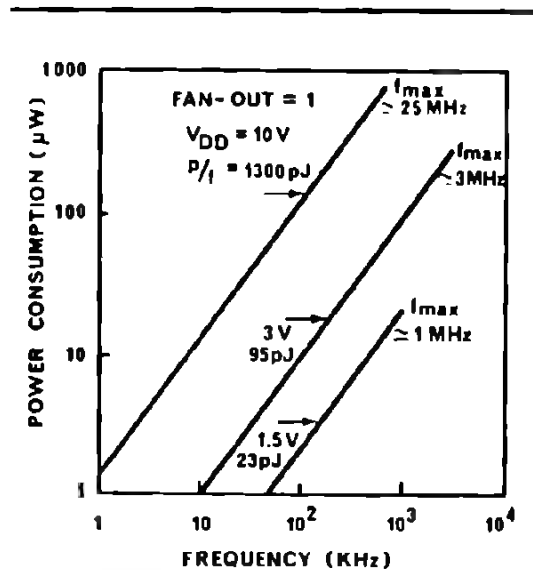


Fig. 15
POWER CONSUMPTION OF A
SINGLE FLIP-FLOP VERSUS
FREQUENCY

Divider chain:

Flip - flops used in divider chains are normally built as toggle flip flop using transmission gates and inverters as base functions. Their performances are as follows:

maximum toggle frequency at 1.5V:

1MHz typ

static power dissipation: 2 nW

Dynamic power consumption versus frequency is given in Figure 15 for a single flip-flop.

The Figure 16 shows the typical current consumption versus frequency of the total divider chain of a 16 stage divider (MTD 160/161 F).

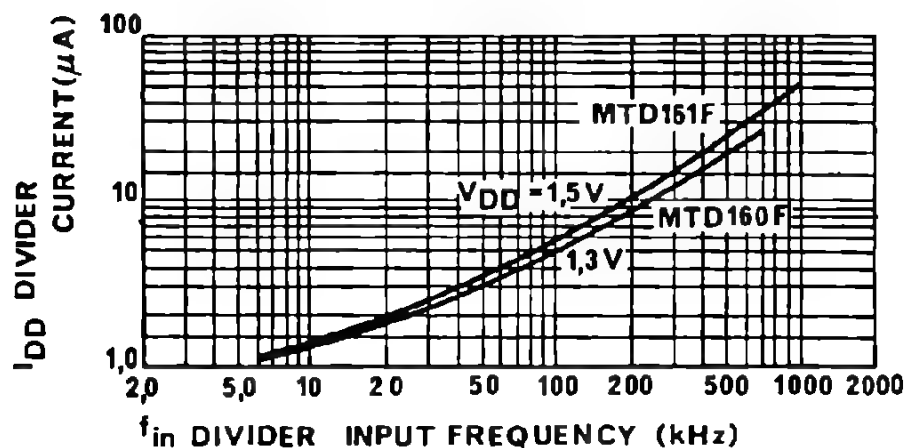


Fig. 16
TYPICAL CURRENT VERSUS FREQUENCY FOR A 16 STAGE DIVIDER

because the power consumption of a flip-flop is proportional to its input frequency, the first flip flop of a divider chain will consume approximatively 0% of the total power. The other 50% of the power are taken by the rest of the divider chain (Fig. 17).

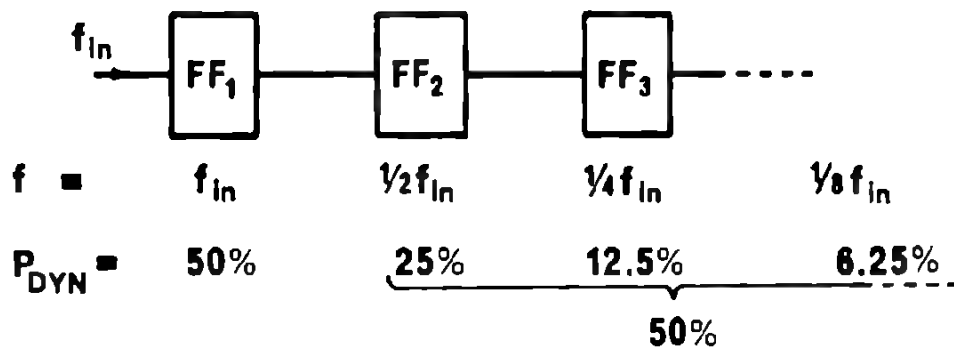


Fig. 17 POWER DISSIPATION IN A DIVIDER CHAIN

Output:
 Output pulse width generation:
 In order to reduce power consumption, motors are normally driven with short pulses. The 50% duty-cycle output of the flip-flops can be reduced to the required pulse width by gating or by a reset flip-flop, as shown in Figure 18 and 19.

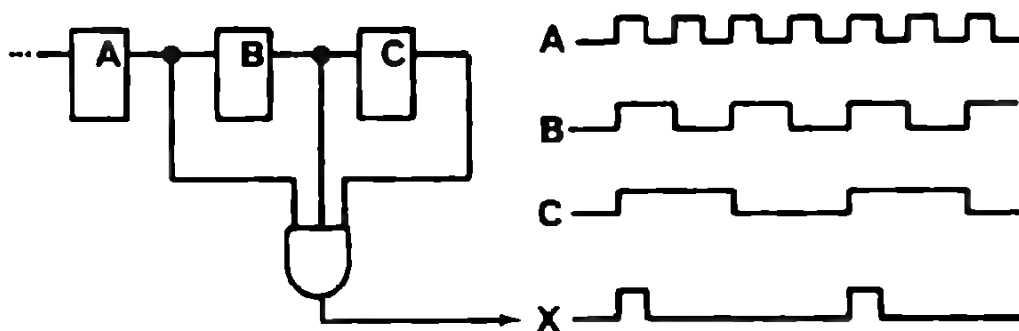


Fig. 18 OUTPUT GATING

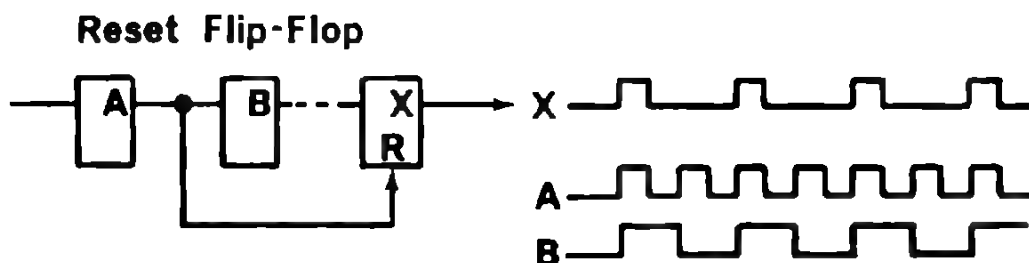


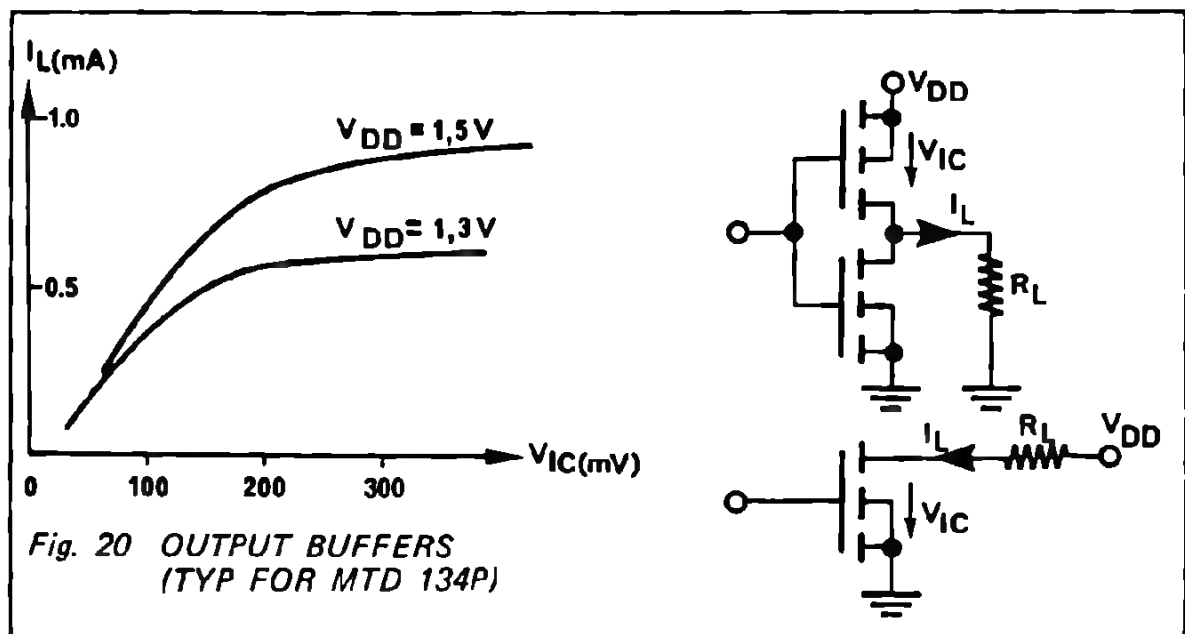
Fig. 19 OUTPUT RESET

Output buffer:

An output buffer is necessary to translate the voltage levels of the dividing and pulse forming stages into current pulses of sufficient amplitude to drive an electromechanical transducer (motor). The higher the needed output current, the larger is the chip area required for the output buffer transistors.



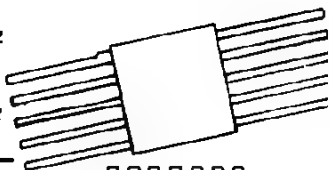
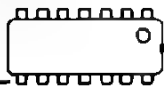

For a given chip area, the output transistor will have a voltage drop V_{IC} in function of the load current I_L .

Buffers can have a single transistor or be built as an inverter. In case of single transistor it can only sink current, whereas an inverter configuration can sink or source current. See also Figure 20.



A summary of the MOTOROLA Timepiece Electronics Integrated Circuits is given in Figure 21.

Fig. 21 SUMMARY OF MOTOROLA TIMEPIECE ELECTRONICS ICs

Type	Oscill	Divider	Pulse Width Control	Output Buffer	Supply Voltage Range	Preferred Crystal Frequency	Package
MTD130F	Yes	13 Stages	50 /	Unipolar	1.20-1.75	5.5 32KHz	
MTD131F	Yes	13 Stages	50 /	Unipolar	1.40-1.65	6.0 32KHz	
MTD160F	Yes	16 Stages	1.563 /	Bipolar	1.20-1.45	32KHz	
MTD161F	Yes	16 Stages	1.563 /	Bipolar	1.40-1.65	32KHz	
MTD180F	Yes	18 Stages	25%, -12.5% ... 0.195%	Bipolar	1.25-1.45	131KHz	
MTD181F	Yes	18 Stages	available on metal option	Bipolar	1.45-1.65	131KHz	
MTD132P	Yes	13 Stages	50 /	Unipolar	1.20-1.65	262KHz	
MTD134P	Yes	14 Stages	DC control on 4,9,10,11,12,13,14	Unipolar	1.20-1.65	262KHz	
MTD135P	Yes	15 Stages	50%	Unipolar	2.30-3.30	262KHz	

2. 3. STEPPING MOTOR

The MTM 1 and MTM 2 are bipolar rotary stepping motors for watch applications.

These motors are unidirectional and rotate 180° per input pulse. They are designed to operate at low pulse rates such as one pulse per second.

Principle:

During current pulses, the magnetic field generated in the coil will rotate the rotor, by repulsion, in the direction defined by the magnetic wire detent. The rotor will make a 180° turn, before locking again in the position given by the minimum magnetic resistance path of the detent.

The following impulse of reverse polarity will turn the rotor in the same direction again by 180°. This way, the motor has made two steps for a full turn. (See Fig. 22).

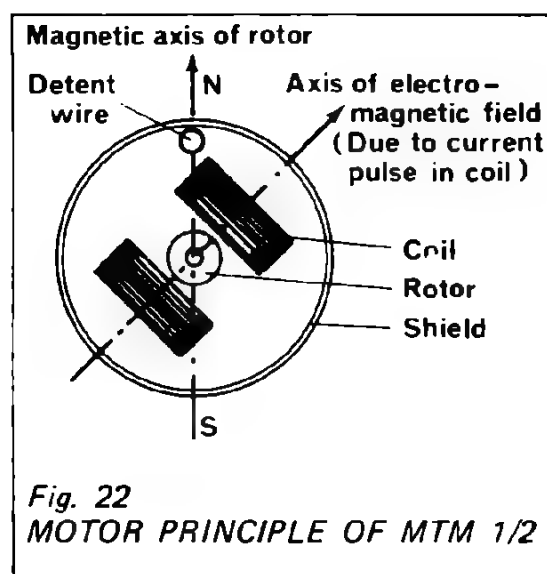


Fig. 22
MOTOR PRINCIPLE OF MTM 1/2

he use of the samarium cobalt mag
17 MG Oe) has given the possibility
performances.

he purpose of the wire detent is to
um magnetic resistivity. It is on thi
o current is applied to the coil.

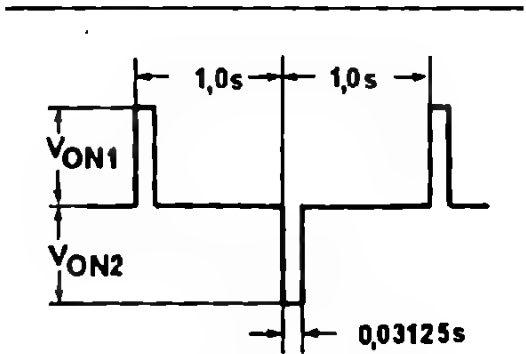


Fig. 23 TYPICAL MOTOR
DRIVE WAVEFORM

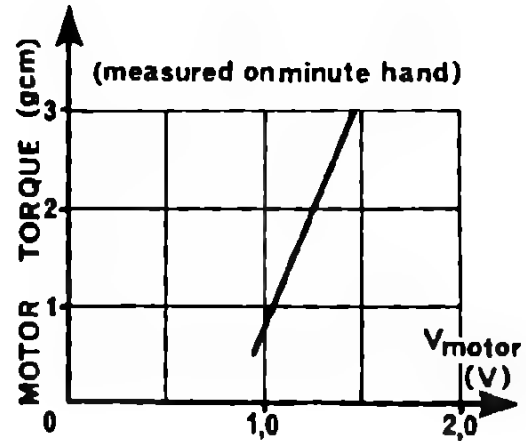
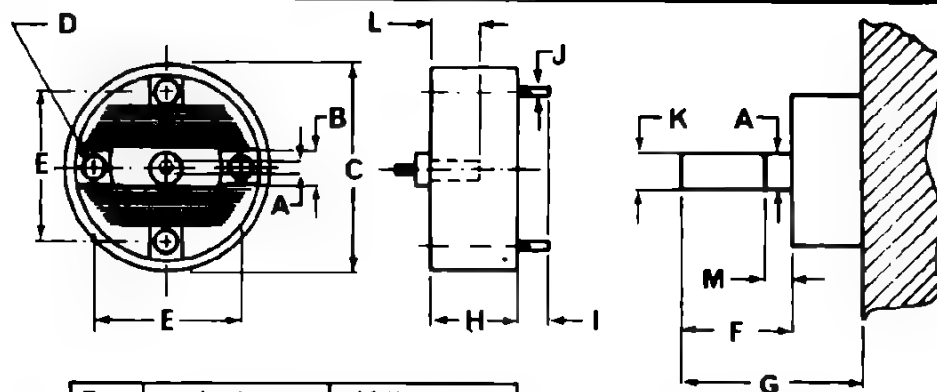
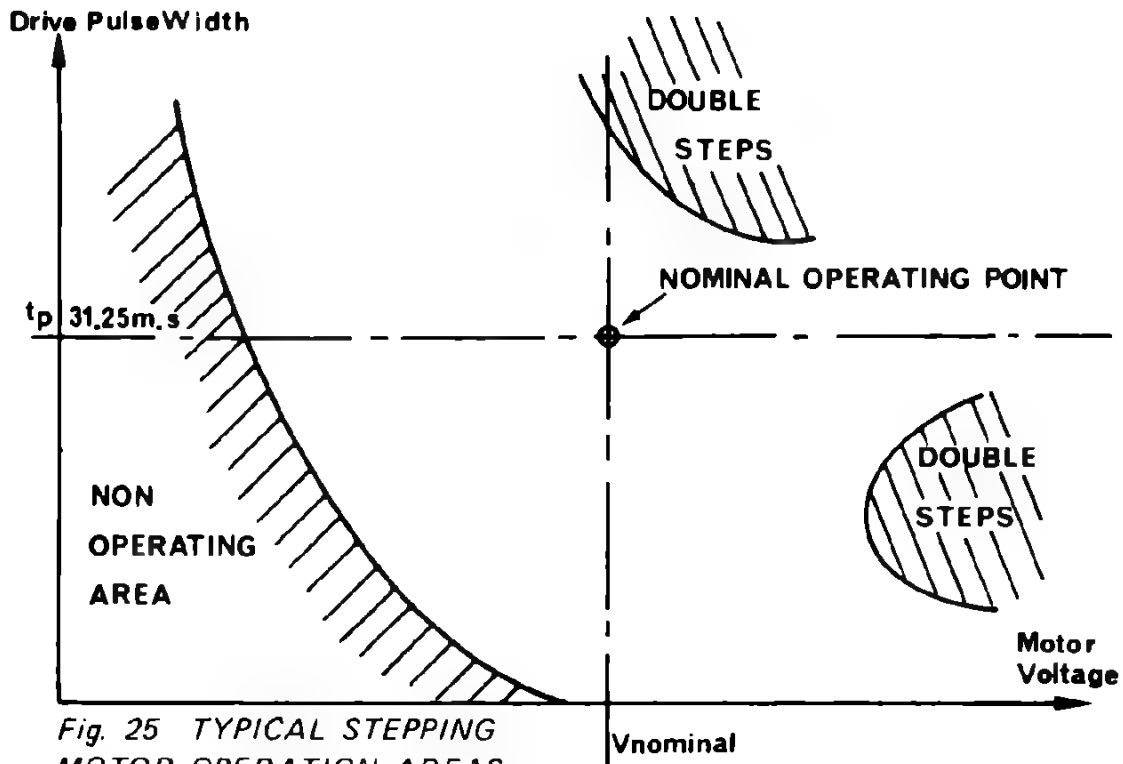
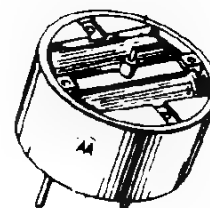


Fig. 24 MOTOR TORQUE VS.
MOTOR VOLTAGE



Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0094	0.0095	0.239	0.241
B	0.0392	0.0396	0.996	1.006
C	0.2458	0.2490	6.243	6.325
D	0.0190	0.0210	0.483	0.533
E	0.1890	0.1910	4.801	4.851
F	0.0235	0.0328	0.597	0.833
G	0.0420	0.0500	1.067	1.270
H	0.1050	0.1070	2.667	2.718
I	0.1660	0.1760	4.216	4.470
J	0.0070	0.0090	0.178	0.229
K	0.0092	0.0093	0.234	0.236
L	0.0500	0.0700	1.270	1.778
M	0.0035	0.0095	0.089	0.241
Axial Play	0.0010	0.0050	0.025	0.127
Rad Play	0.0003	0.0006	0.0076	0.0152



MTM 1: counter clock wise rotation
 MTM 2: clock wise rotation
 (view from pinion side)

Fig. 26 MECHANICAL DIMENSIONS OF MTM 1/2

2. 4. TRIMMERS

Requirements:

The purpose of the trimmer capacitor is to adjust the oscillator frequency to the required nominal value. With this, tolerances such as crystal frequency dispersion, IC frequency dispersion can be compensated for. In addition it will allow to re-adjust the timepiece system to account for future aging and future shock.

As outlined in 4. 2. a trimmer value of 6–35pF proves to be a good choice for watch systems.

Characteristics:

The trimmers MTT 02/03/04 are recommended for the MOTOROLA timepiece systems. These trimmers are temperature cycled by the supplier to avoid possible frequency instabilities with temperature changes once they are mounted in an oscillator circuit.

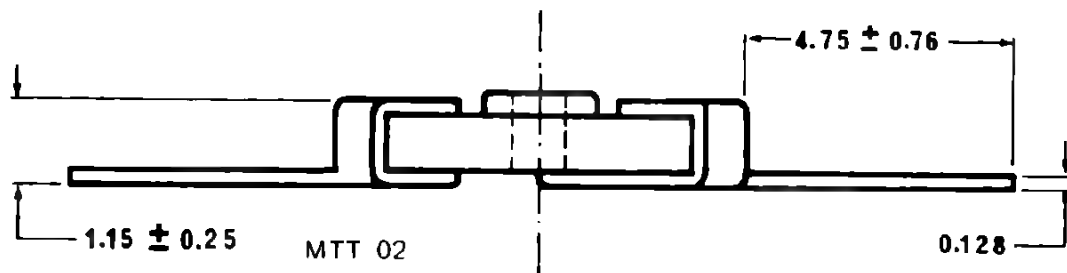
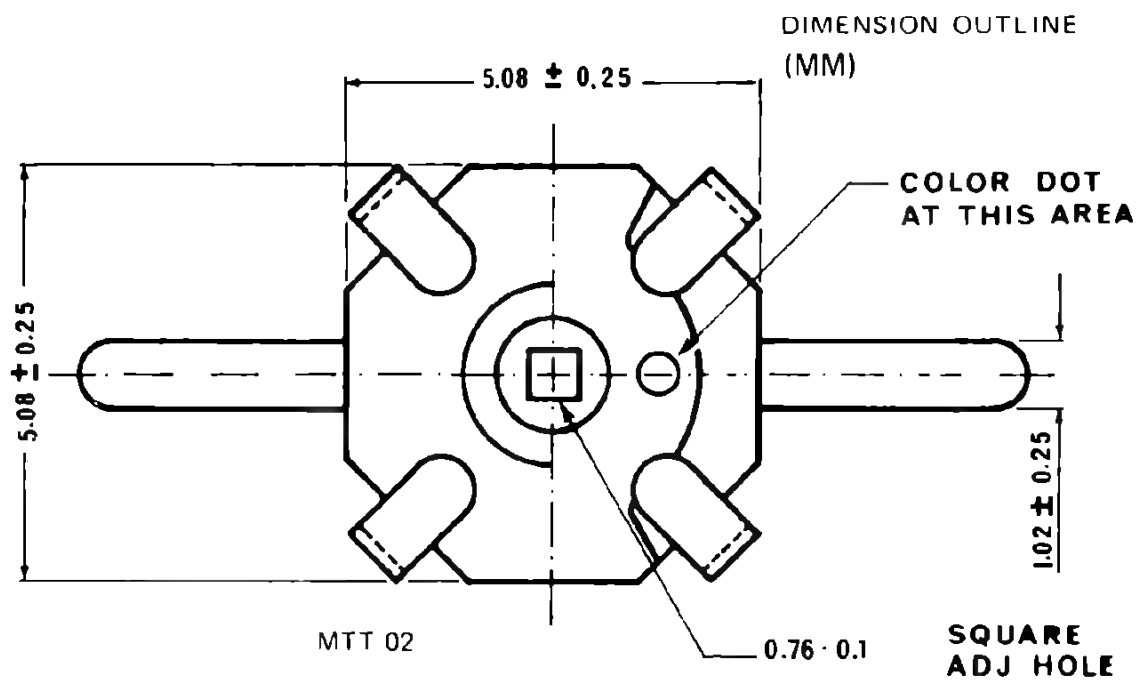
Electrical characteristics:

	Min	Max	Units
Capacitance range	6	35	pf
DC working voltage		100	Vdc
Q at 1 MHz	400		
Temp.Coefficient (–20°C to +35°C)	220	720	ppm/°C

Mechanical dimensions are shown in Figure 27.

The trimmers are available in three mechanical options:

MTT 02 leads straight
MTT 03 leads bent upwards
MTT 04 leads bent downwards



MTT 02 leads straight
 MTT 03 leads upwards
 MTT 03 leads downwards

Fig. 27 MECHANICAL DIMENSIONS OF MTT TRIMMERS

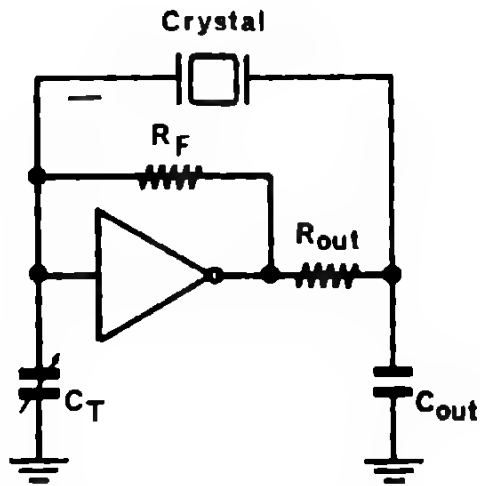


Fig. 28
OSCILLATOR CIRCUIT WITH R_{out}

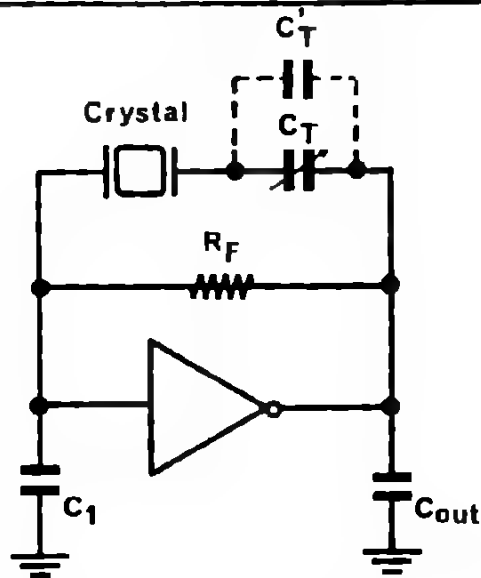


Fig. 29 OSCILLATOR WITH
SERIES TRIMMER

3. 2. OSCILLATOR CIRCUITS FOR

For applications, where the power supply is normally seen on silver oxide (1.58V to .25V) batteries, it may be advantageous to use the circuits shown in Figure 28 and 29.

The circuit of Figure 28 with the addition of a series trimmer improves frequency stability with supply voltage. It is not a higher oscillator start voltage. It is not the best chosen at about 100k Ω .

For DT cut crystals, the oscillator circuit provides frequency stability versus supply voltage. It is not a higher oscillator start voltage.

3. 3. OSCILLATOR PERFORMANCES

The stability of the oscillator frequency, and hence the accuracy of the time base, is mainly dependant on temperature changes, supply voltage changes, aging and shock.

With the exception of aging, all these effects will, in general, decrease the crystal frequency, i.e. the timepiece tends to be "slow". Aging will partly compensate for this by tending to increase the crystal frequency.

Frequency versus temperature:

In practice, the crystal is the dominant factor for the temperature performance of the oscillator. Therefore, the curves as shown in Figure 3 are also valid for total systems performances.

Frequency versus aging:

Only dependant on crystal aging. Refer to Figure 9.

Frequency versus shock:

Again, oscillator performance on shock is dependant on crystal only. See chapter shock, paragraph 2.1, page 12-6.

Frequency versus supply voltage:

Typical performances of $\frac{\Delta f}{f}$ versus V_{DD} are given in Figure 30.

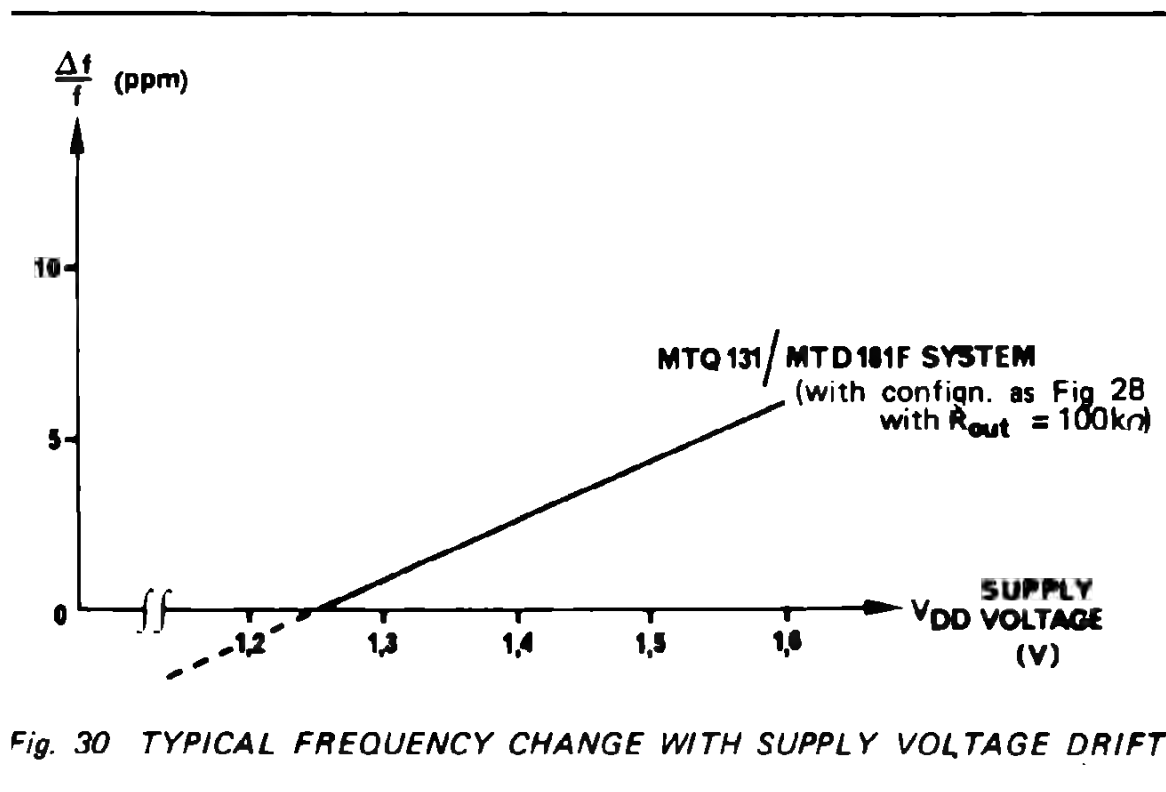


Fig. 30 TYPICAL FREQUENCY CHANGE WITH SUPPLY VOLTAGE DRIFT

4. CRYSTAL / IC INTERFACE

4. 1. TOLERANCES IN CRYSTAL CONTROLLED OSCILLATORS

For an oscillator circuit to be adjusted to the nominal frequency at any time, provisions must be made to compensate for crystal frequency tolerance, aging, shock and IC frequency dispersion.

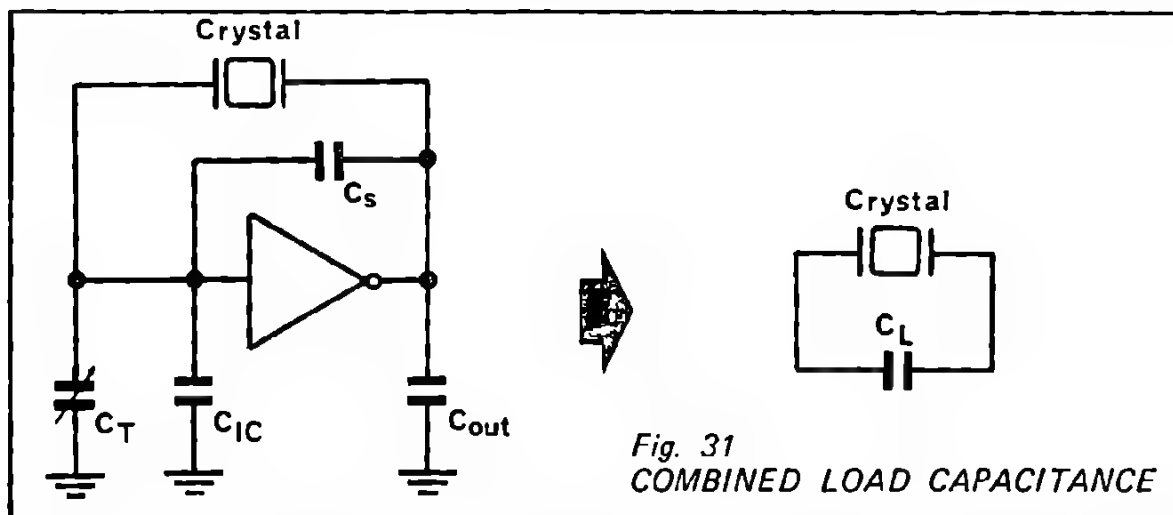
Typical maximum values for these tolerances are:

crystal frequency tolerance	40 ppm
aging (over several years)	12 ppm
shock (several shocks)	8 ppm
IC frequency dispersion	30 ppm

4. 2. CHOICE OF TRIMMER VALUE

The value of the trimmer capacitance C_T must therefore be chosen such that it can compensate for above tolerances. This would normally call for a trimmer with a wide capacitance range. However, in practice there are several limitations to the trimmer values. First, the minimum value of C_T should not be too small, for better oscillator stability (at low trimmer values, a small capacitance drift will create a large frequency shift, see also Figure 8). Second, the maximum value of C_T should not exceed 50 pF for good oscillator start performance. Third, for ease of adjustment, it is useful to choose the trimmer value range as small as possible (it is easier to adjust the oscillator if its frequency shift is small for a given rotation angle of the trimmer).

A trimmer of 6–35 pF has proven to be a good compromise solution to satisfy all requirements of the watch systems.



4. 3. CLASSICAL CALCULATIONS ON COMBINED LOAD CAPACITANCE

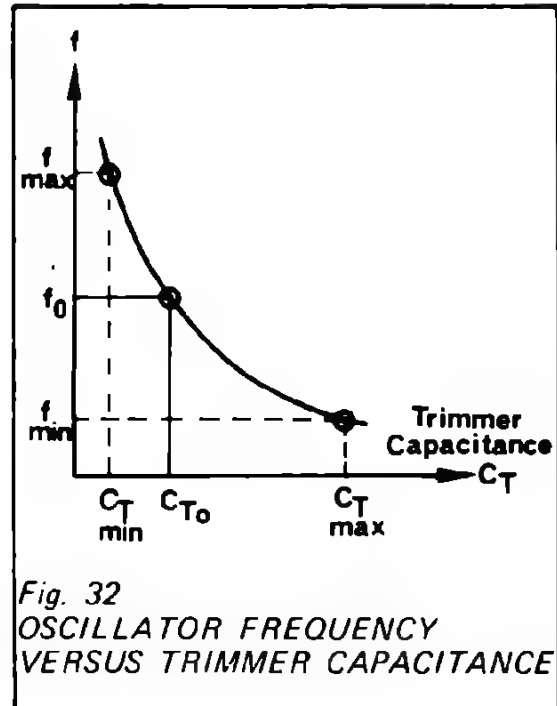
Consider an oscillator circuit as shown in Figure 31. In addition to the trimmer capacitance C_T and the output capacitance C_{out} there is a (parasitic) input capacitance C_{IC} of the IC and a stray capacitance C_S of circuit leads etc.. Under ideal inverting amplifier conditions, this capacitor network can be reduced to a combined load capacitance C_L as follows:

$$C_{IN} = C_T + C_{IC}$$

$$C_P = \frac{C_{IN} \cdot C_{out}}{C_{IN} + C_{out}}$$

$$C_L = C_P + C_S = \frac{(C_T + C_{IC}) \cdot C_{out}}{C_T + C_{IC} + C_{out}} + C_S$$

With C_T having a minimum and a maximum value C_{Tmin} and C_{Tmax} respectively, a maximum and a minimum frequency f_{max} and f_{min} will result (Fig. 32).



From this follows that the crystal should be cut to nominal frequency f_0 at a value C_{L0} corresponding to the nominal capacitance C_{T0} of the trimmer. Besides the fact that the above calculation is a large simplification of actual circuit behaviour, it is also true that the normally used crystal impedance meters do not work at very low crystal drive levels, so that the C_L value measured on the instrument will not correspond to the one encountered in the actual oscillator circuit.

Therefore, a more accurate and more practical solution is chosen for the frequency compatibility of crystal and IC.

4. 4. MIN / MAX Δf APPROACH

Of high importance in large volume timepiece production is the requirement, that no matching between components be necessary. That is, any crystal of a given lot should be usable with any IC, of a given lot. This is only possible with a well defined total system.

The "min/max Δf " method ensures a full frequency compatibility between crystal and IC. Basically, it consists of a defined frequency test of crystal and IC under actual circuit conditions. This test is made all the way through from production over quality assurance to the customers incoming inspection and final use. Full correlation of the systems parameters is therefore easily made at every level.

The method consists of testing all crystals with a worst case IC. Likewise, all IC's are tested with a worst case crystal.

Fig. 33
ACCEPT RANGES FOR
CRYSTALS

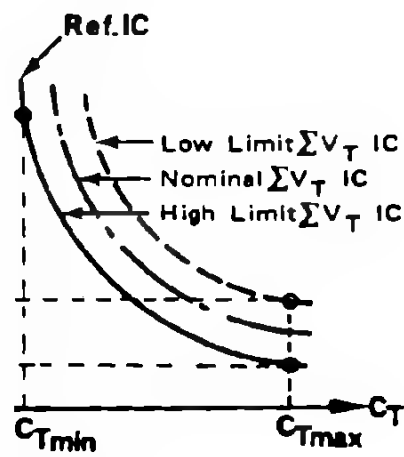


Fig. 34
ACCEPT RANGES FOR ICs

ace is the interface between motor
eral points have to be observed

the minimum required motor torque

MOTORS

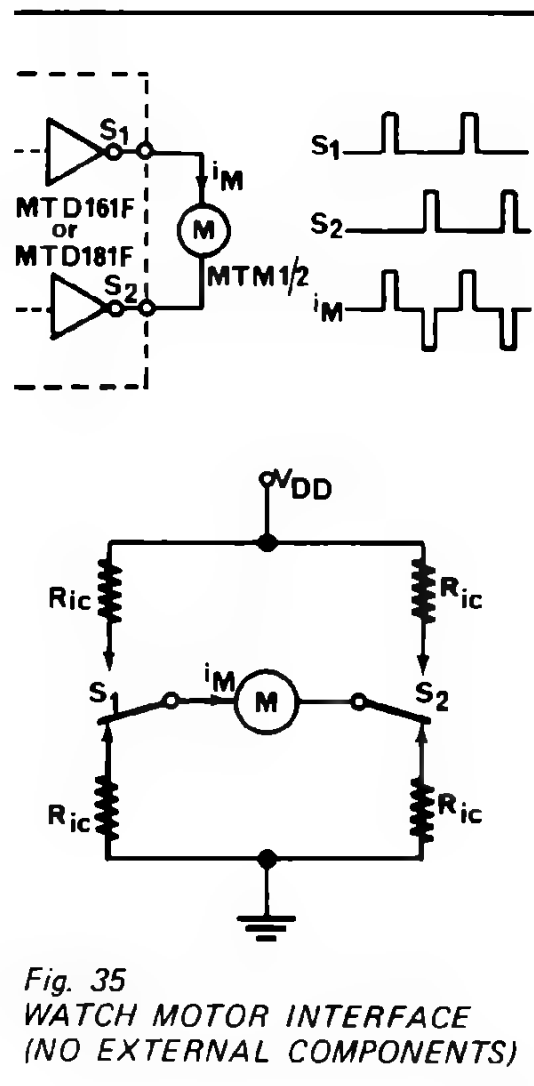


Figure 36 shows various examples of interface circuits.

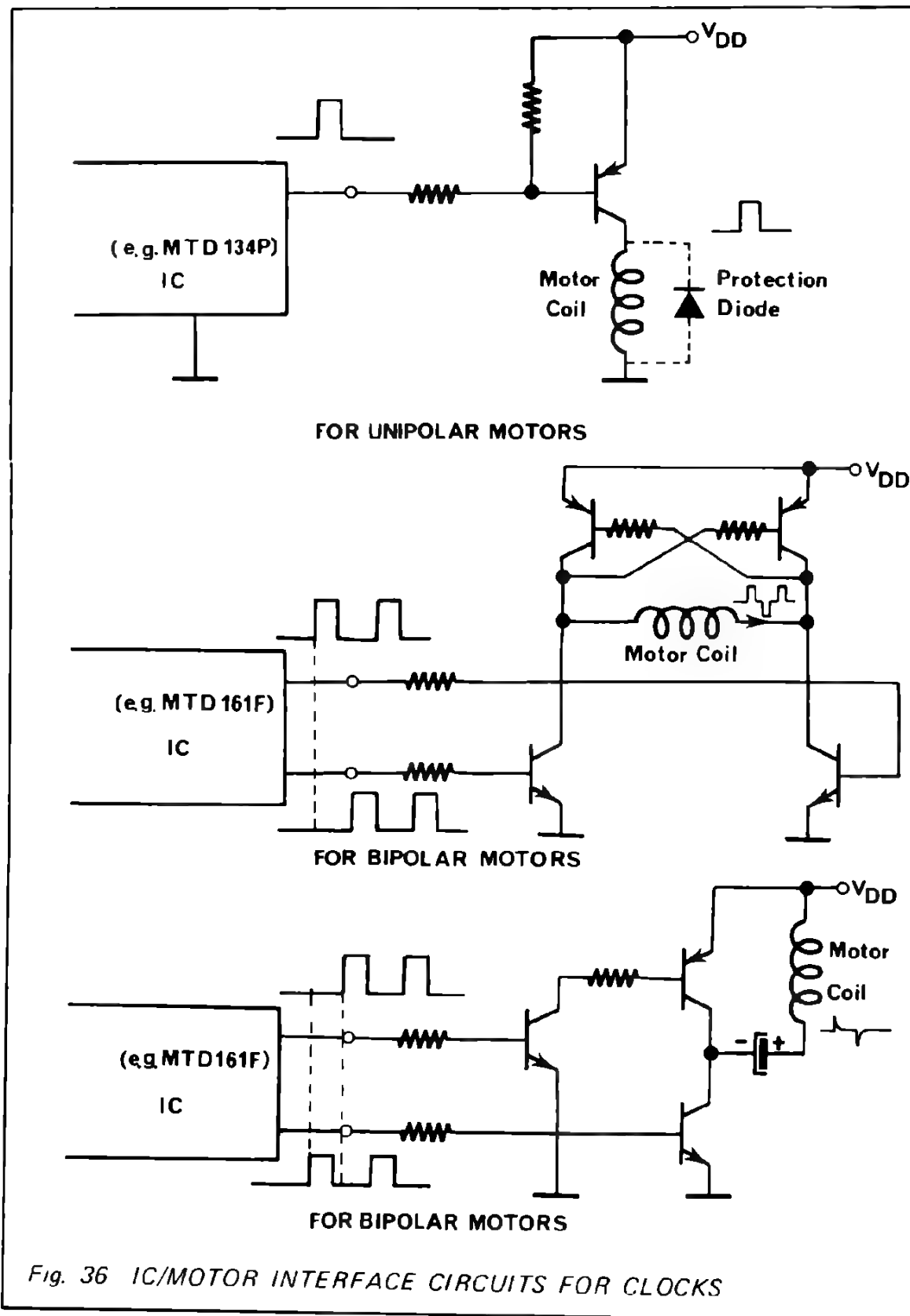


Fig. 36 IC/MOTOR INTERFACE CIRCUITS FOR CLOCKS

WATCH APPLICATION

32 KHz / 16 STAGE SYSTEM

1. DESCRIPTION

Today, the 32 KHz (more precisely: 32.768 KHz or 2^{15} Hz) crystal has become an industry standard. It represents an optimal compromise between the trend for high frequencies (lower cost of crystals) and the current consumption limits of volume produced ICs.

MOTOROLA offers a fully compatible set based on the 32 KHz crystal.

This system consists of:

- MTQ 32-2 - 32.768 KHz NT cut quartz crystal
- MTD 161F - Oscillator, divide by 2^{16} , buffer Integrated circuit in Silicon Gate CMOS technology
- MTM 1/2 - Miniature rotary stepping motor
- MTT 02 - Trimmer capacitor 6–35 pF.

Figure 37 shows how the individual components are interconnected.

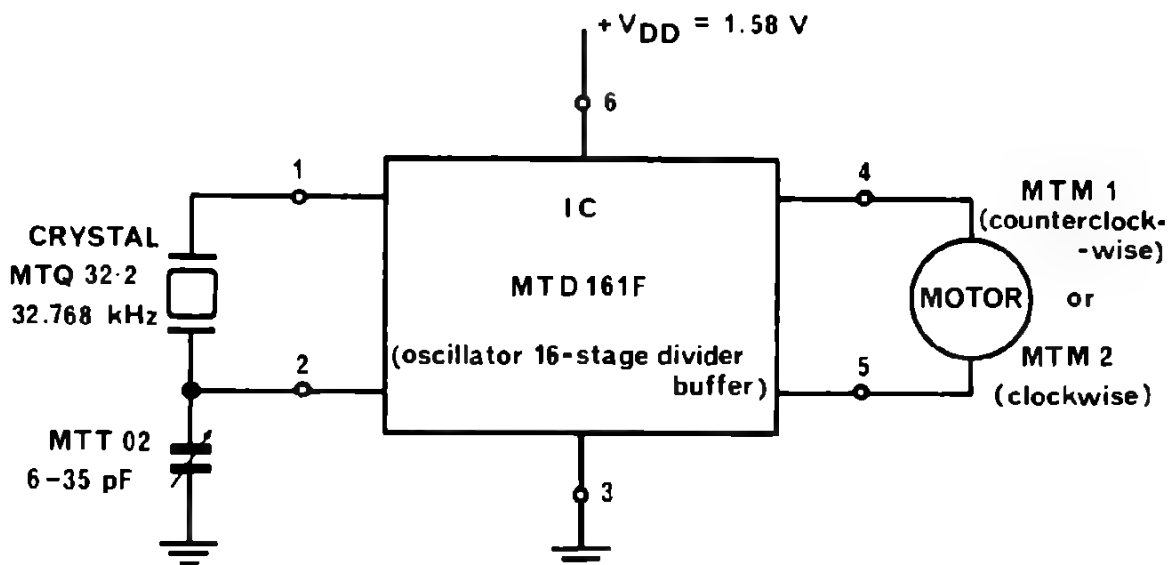


Fig. 37 32 KHz WATCH SYSTEM

1. 2. SPECIFICATIONS

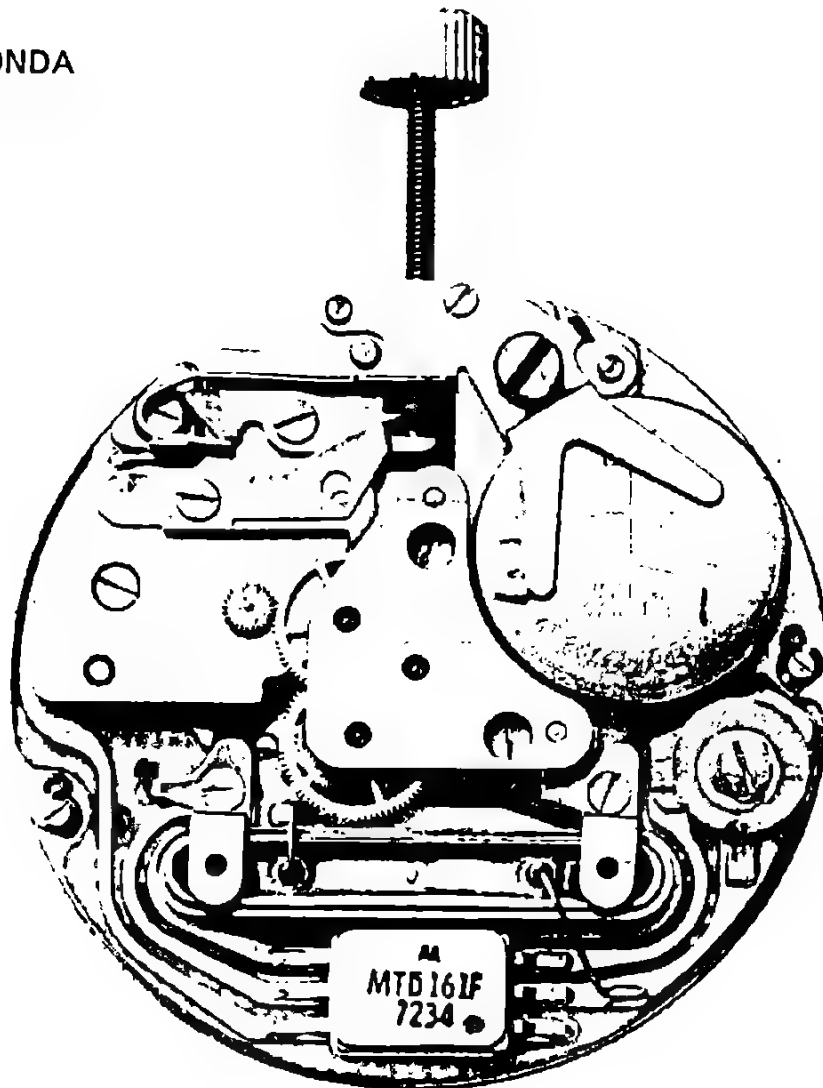
The system is designed to operate with a silveroxide battery (1.58V nominal). Under worst case conditions the motor will develop a torque of 2.0 gram-centimeter, measured at the minute hand of an ideal gear train. This assures a safety factor of 2 for a well designed day/date movement under heaviest load conditions (calender change).

Total current consumption of this system will not exceed $15\mu\text{A}$ at 1.58V supply. Typically, it will run around $12\mu\text{A}$. Thus, with a battery of 165mAh (EPX 77), the system will run for a minimum of 15 months, typically for 18 months.

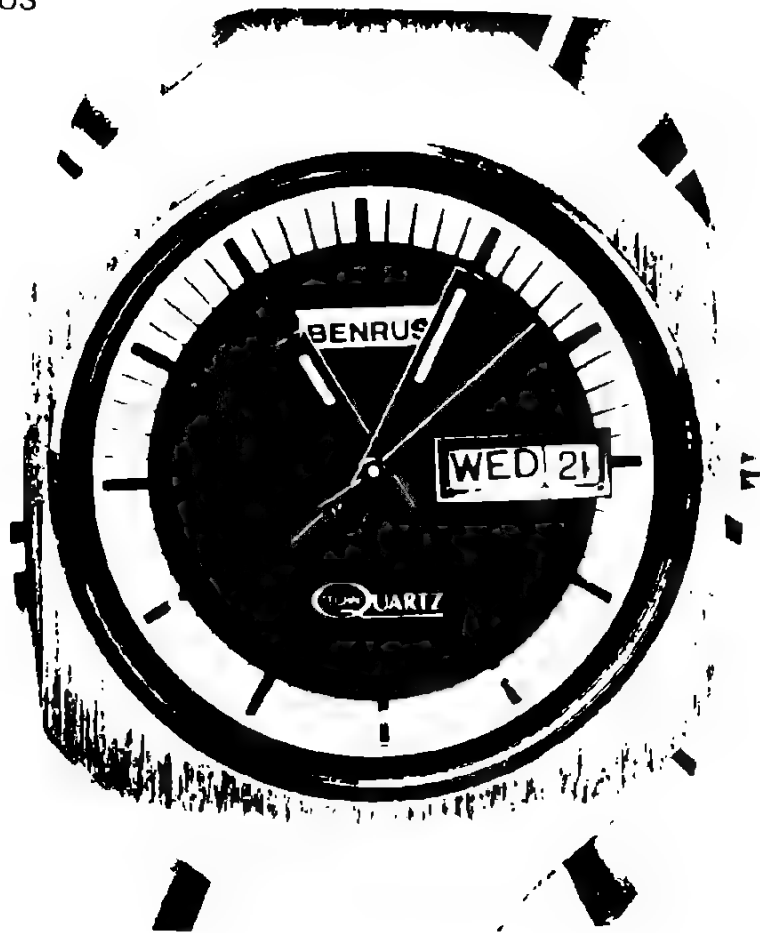
1. 3. EXAMPLES

Various examples of designs around the MOTOROLA quartz watch system are shown in Figure 38 and 39.

RONDA



BENRUS



131 KHz / 18 STAGE SYSTEM

1. DESCRIPTION

Most likely, the next frequency "standard" for quartz watches will be 131 KHz more precisely: 131.072 KHz or 2^{17} Hz).

With an NT cut crystal, the size of the package is significantly reduced over the size of the 32 KHz crystal package, thus allowing the design of a more compact watch movement.

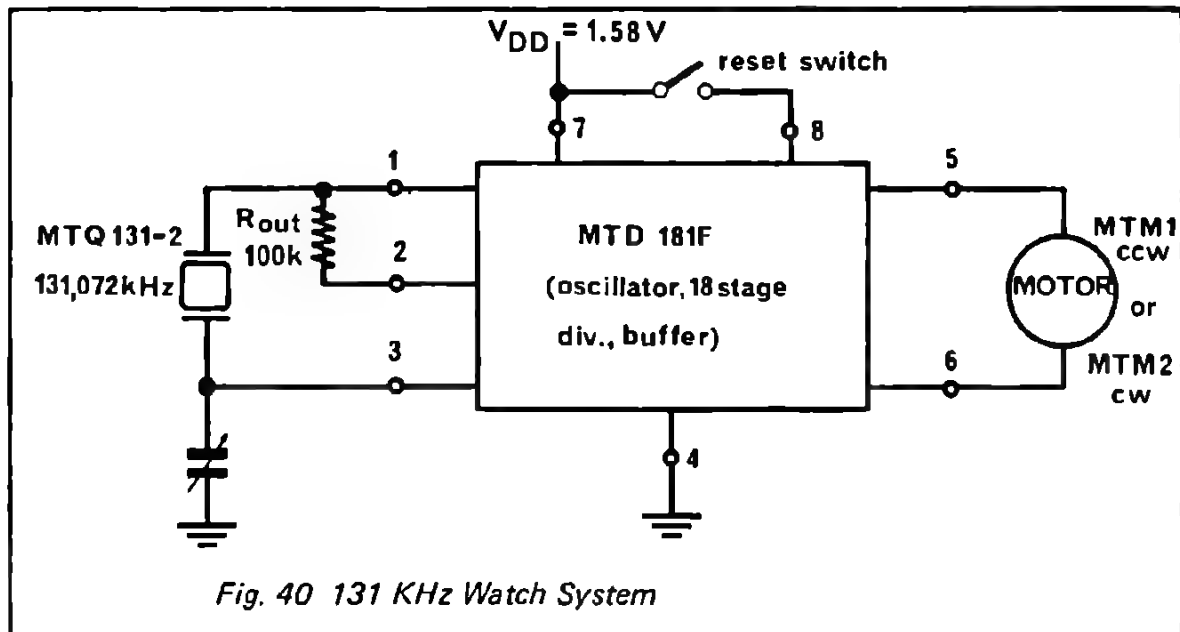
The dimensions of the 131 KHz quartz package do not exceed 10.4 mm x 12.2 mm x 3.3 mm.

For this frequency of 131 KHz, a new IC was designed. The MTD 181F is an 8-stage divider circuit, containing the oscillator circuit and output buffers to drive the MTM 1 or MTM 2 motors directly.

With this circuit, a new timepiece system is made available, consisting of

- MTQ 131-2 — 131.072 KHz NT cut quartz crystal
- MTD 181F — Oscillator, divide by 2^{18} , buffer circuit (Si Gate CMOS)
- MTM 1/2 — Miniature rotary stepping motor.

The interconnection diagram of the full system is given in Figure 40.



Note that this system offers an accurate reset feature. If pin 8 of the IC is connected to $+V_{DD}$, the divider chain is inhibited and a part of this chain is reset to zero. The motor will not get any pulses during this time.

When $+V_{DD}$ is removed from pin 8, it will take $1.000^{+0}_{-0.008}$ seconds before the motor will get its next pulse. The time setting error — otherwise up to 2 seconds — will only be dependant on the human response time for this unique system. (Human response time is in the order of 100 to 250 ms.)

In addition the MTD 181F offers the possibility to connect an additional resistor R_{out} in series with the oscillator inverter, as shown in Figure 40. R_{out} of approx. 100 k Ω further improves the frequency stability of the oscillator versus supply voltage changes.

2. 2. SPECIFICATIONS

Power supply voltage (silver oxide battery)

$V_{DD} = 1.58V$ typ

Current drain of total system, including motor

$I_{DD} = 14.0 \mu A$ typ
 $16.3 \mu A$ max

Battery life (using EPX 77 with 90% of rated 165 mAh)

$t_B = 14.5$ months typ
 12.5 months min

Motor torque (minute hand) under worst case conditions

$M_M = 2.0$ gcm min

I. OTHER SYSTEMS

The systems described in 1 and 2 represent the standard watch systems available from MOTOROLA.

In addition to these, many other systems possibilities exist to serve the individual requirements. Some examples are described below.

I. 1. SYNCHRONIZED BALANCE WHEELS

Existing electric watch movements with electro-mechanical balance wheels can be synchronized with a precise time signal derived from a quartz crystal. Using an MTQ 32 (32.768 KHz or 2^{15} Hz) and an MTD 131F (oscillator, 2^{13} divider, buffer), a time base signal of 4 Hz can be derived. Various circuit configurations are possible to drive the balance wheel.

Direct drive:

The balance wheel coil gets its impulses directly from the IC (Fig. 41).

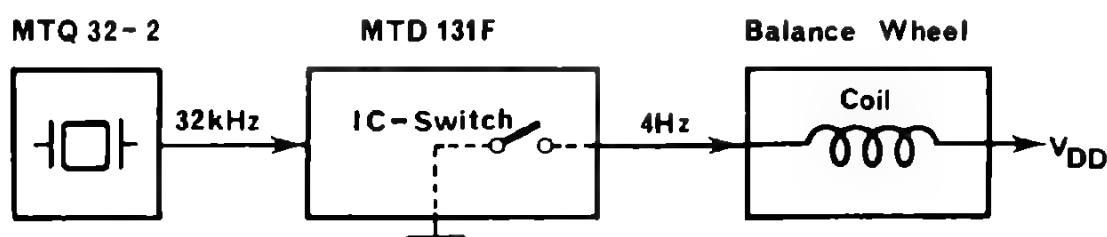


Fig. 41 DIRECT DRIVE OF BALANCE WHEEL

Synchronization with series switch:

The balance wheel coil will only get an impulse if the synchronizing signal AND the balance wheel contact are on (Fig. 42).

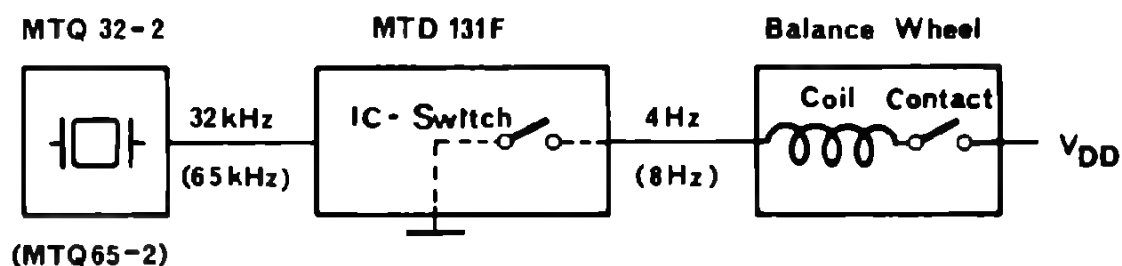
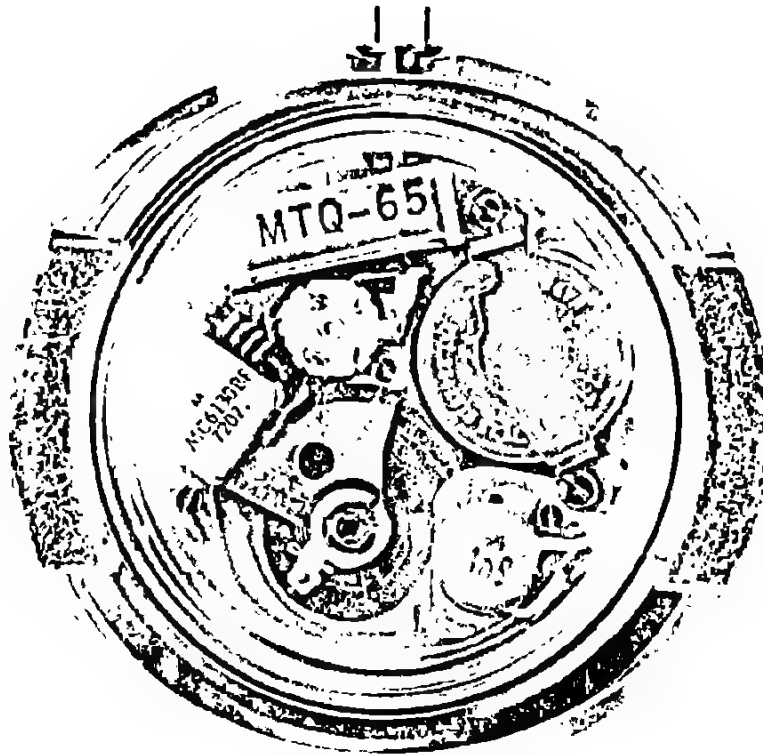


Fig. 42 SERIES SWITCH SYNCHRONIZATION

Here, the width of the current pulse (and thus the amount of energy given to the balance wheel) is simultaneously controlled by the time reference signal and by the amplitude of the balance wheel (via contact).

Other possibilities include synchronizations of the two-coil systems, omitting the balance wheel contact, and solutions where the movement will continue to work (with less accuracy, of course) in the absence of the synchronization signal.

Similarly, an 8 Hz signal can be obtained from an MTQ 65 and an MTD 131F. Example of application ROBERTA. See Figure 43.



3. 2. METALLIZATION OPTIONS

For some particular applications, it may become necessary to design a new metallization mask for a given IC.

With metallization options, given divider chains can be shortened, two-phase outputs may be changed into a unipolar output, etc.. It is important to note, however, that the metallization options can only change interconnections within a given chip layout, but they can never add devices to that chip.

Although metal options are basically possible on any IC, the basic chip of the MTD 181F is particularly well suited for this. The number of dividing stages can be cut down from a maximum of 18 to any desired number. The duty cycle (output pulse width) can be changed to any value $\frac{1}{2^n}$, with $n = 1$ to 10.

A buffered alarm output is also available on the chip. It will give an output frequency of 512 Hz when operated with a crystal of 262 KHz (2^{18} Hz) (clock application).

4. FUTURE TRENDS

For reasons of quartz crystal performance and price, there is a natural trend towards higher frequencies. The systems limiting factor is the current consumption of the oscillator and the first dividing stages. New circuit technologies and designs, such as ion implantation and dynamic dividers, will help to move towards higher frequency systems.

However, it is very important that a reasonable compromise be chosen between technical performance, practical feasibility and economical possibilities. This becomes particularly apparent for timepiece-systems which are intended for high volume applications.

C CLOCK APPLICATION

The quartz clocks can be divided into two major classes:

- Analog displays
 - mechanical
 - stepping motors
 - balance wheel motors
 - synchronous motors
 - electronic
 - light emitting diode (LED)
 - liquid crystal display (LCD)
- Digital displays
 - mechanical
 - electronic
 - Nixie tube
 - Seven segment
 - LED
 - LCD

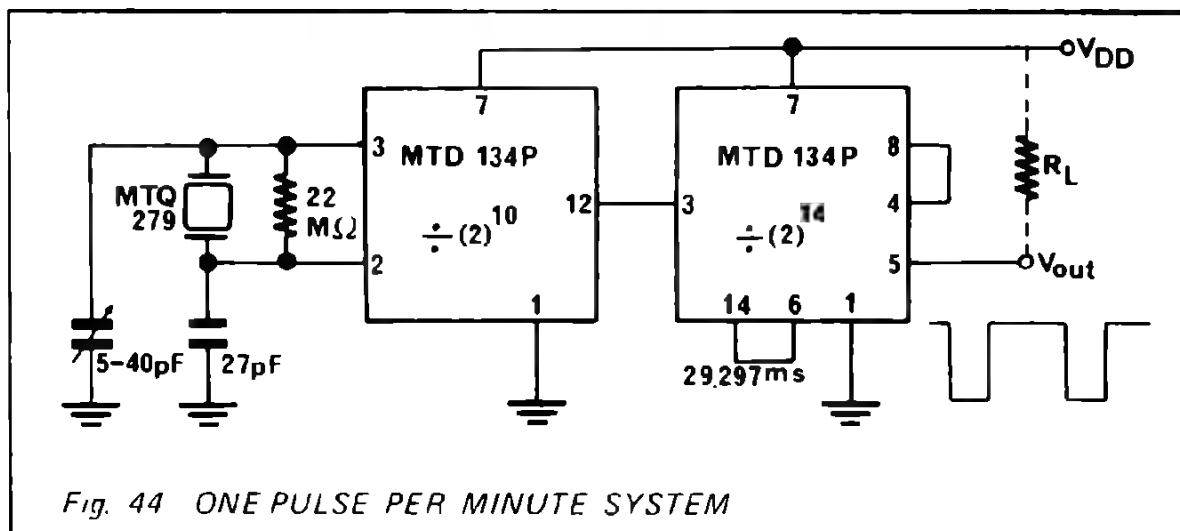
Due to the relative high cost of todays available electronic displays a significant part of all quartz clocks are of the mechanical type, mainly stepping motors and synchronized balance wheels.

Following is a listing of some of the quartz clock systems (the IC / motor interface is not included as it must be designed around the motor used).

1. ONE PULSE PER MINUTE OUTPUT SYSTEM

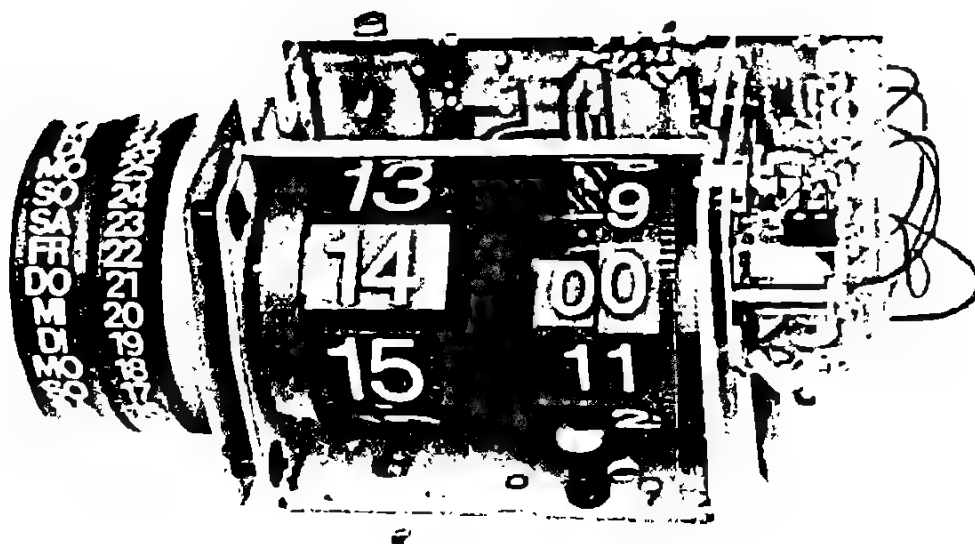
Many applications do not require the accurate one-second information. An accurate one-pulse per minute satisfies many applications such as desk clocks.

The proposed system is shown in Figure 44 and consists of the MTQ 279 (279.620267 KHz) crystal plus 2 circuits MTD 134P with a total of 24 stages.



This way an output frequency of $\frac{1}{60}$ Hz will result as can be seen below:
 $279.620267 \text{ KHz} \times 60 = 2^{24}$

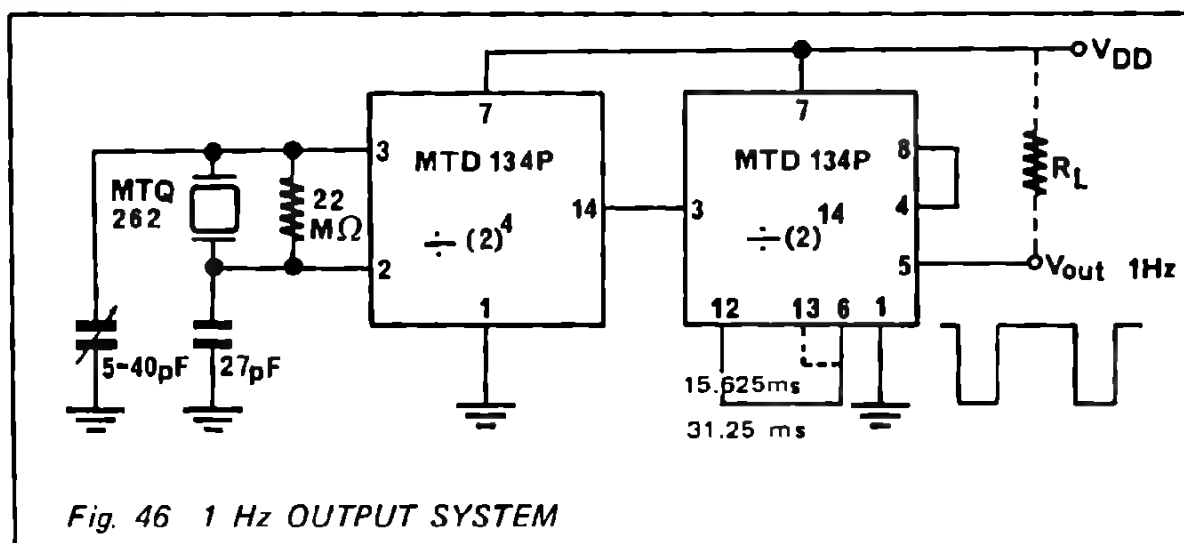
A practical example is shown in Figure 45, a digital desk clock by KUNDO.



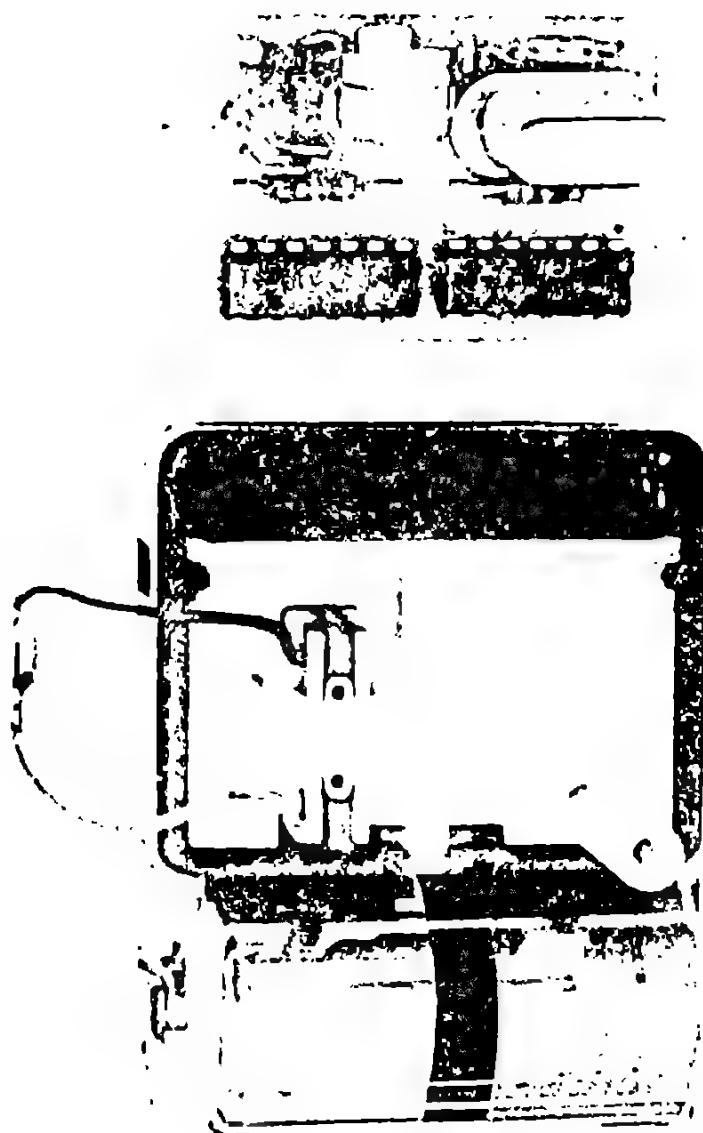
2. 1 Hz OUTPUT SYSTEM

Quartz clocks with second hands using stepping motors require a 1 Hz output signal.

The system proposed in Figure 46 consists of the MTQ 262 (262.144 KHz) crystal plus 2 circuits MTD 134P with 18 stages used.



An example of application is shown in Figure 47, an analog domestic clock by KUNDO.

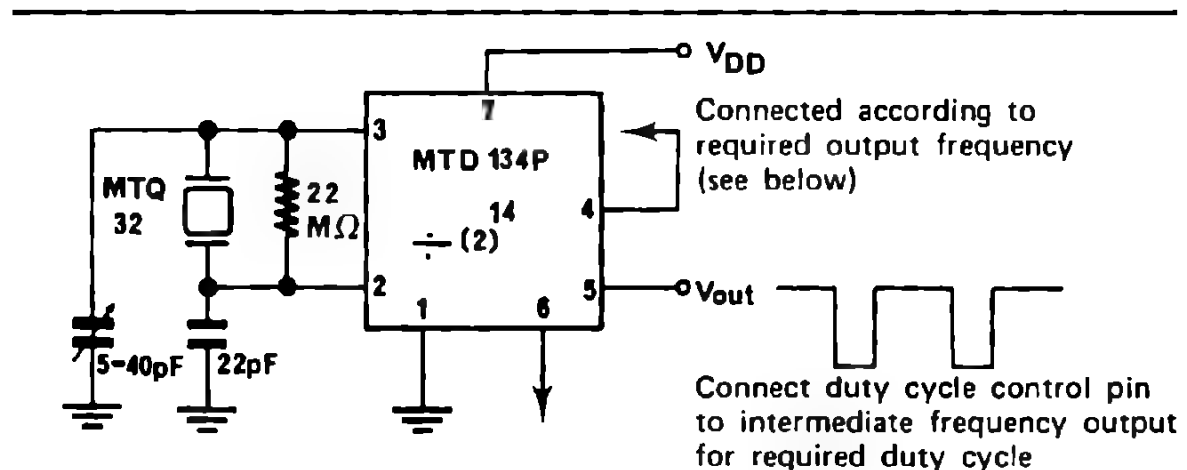


3. 2 Hz – 4 Hz – 8 Hz OUTPUT SYSTEM

These systems can be used to synchronize electro-mechanical balance wheel motors.

They are shown in Figure 48 and use a crystal MTQ 32 with the MTD 134P IC.

Depending on the required frequency, the output of the IC will be connected as indicated in Figure 48.



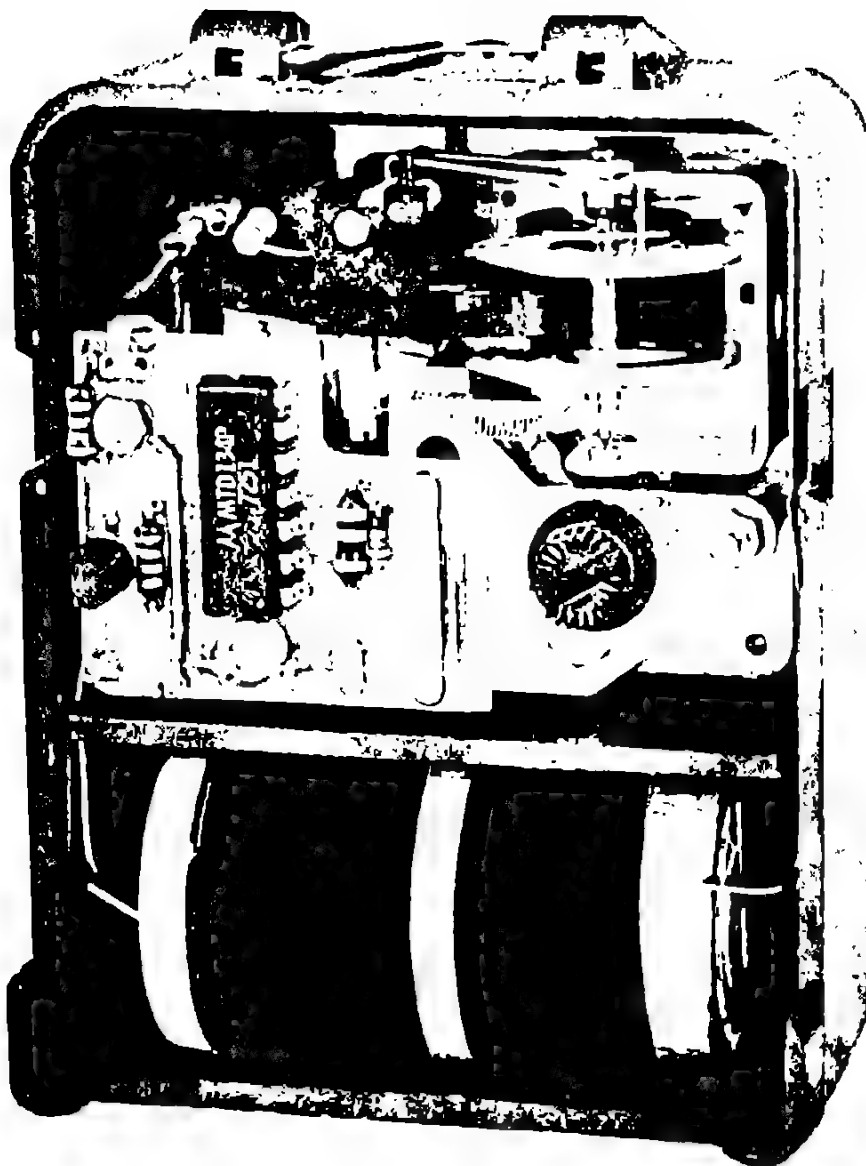
$f = 2 \text{ Hz}$ pin 4 connected to pin 8 (divide by 2^{14})

$f = 4 \text{ Hz}$ pin 4 connected to pin 9 (divide by 2^{13})

$f = 8 \text{ Hz}$ pin 4 connected to pin 10 (divide by 2^{12})

Fig. 48 2 Hz / 4 Hz / 8 Hz OUTPUT SYSTEM

imple of a practical solution is shown in Figure 49 with the clock from NET.



4 5 Hz OUTPUT SYSTEM

This system can also be used to synchronize electro-mechanical balance wheel motors.

The base frequency used in this application is 327.68 KHz, as indicated in Figure 50.

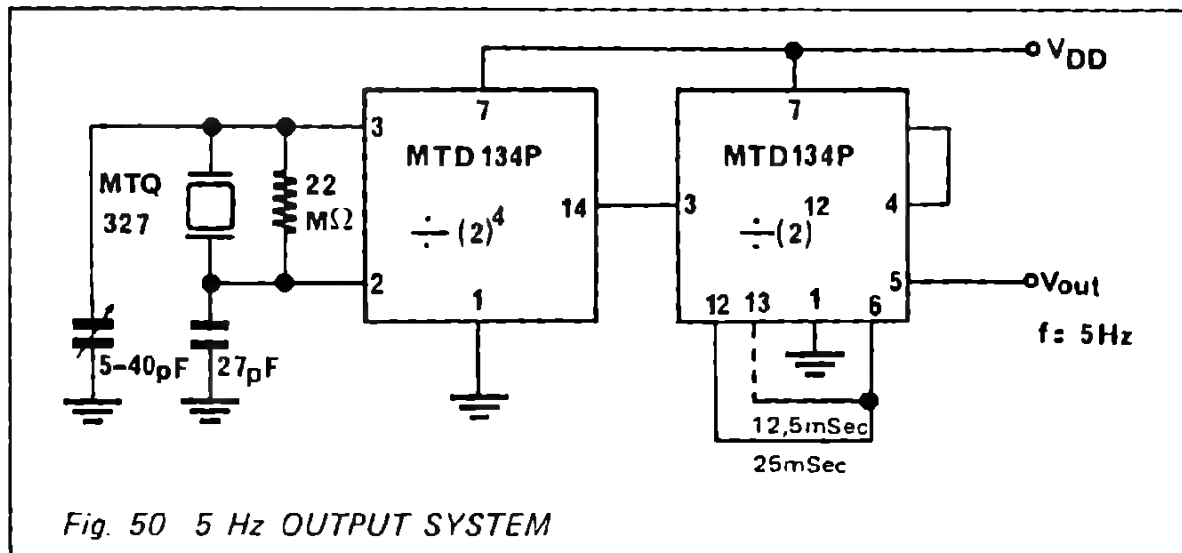


Fig. 50 5 Hz OUTPUT SYSTEM

Example of application: domestic clock from LA VEDETTE shown in Figure 51.

Possible application: synchronization of the "Mouvement de Paris" (ATO Licence).



32 Hz OUTPUT SYSTEM

n application of this system is used for 32 Hz synchronous motors.
his system uses the MTQ 262 crystal with the MTD 132 IC (13 stages) as indicated in Figure 52.

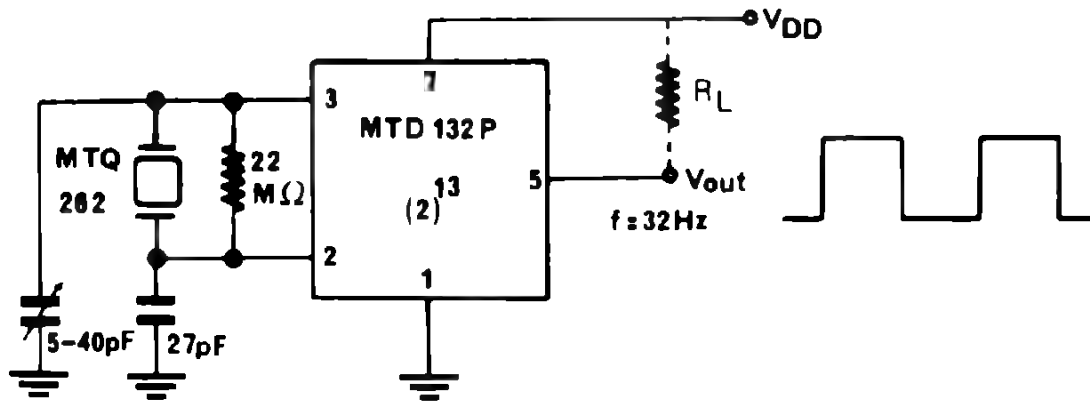


Fig. 52 32 Hz OUTPUT SYSTEM

50 Hz OUTPUT SYSTEM

ne of many applications possible with this system is the driving of 50 Hz
motors.

can also be used to replace the 50 Hz line frequency reference in some digi-
al clock systems.

his system uses the MTQ 409 crystal with the MTD 132P as shown in
figure 53.

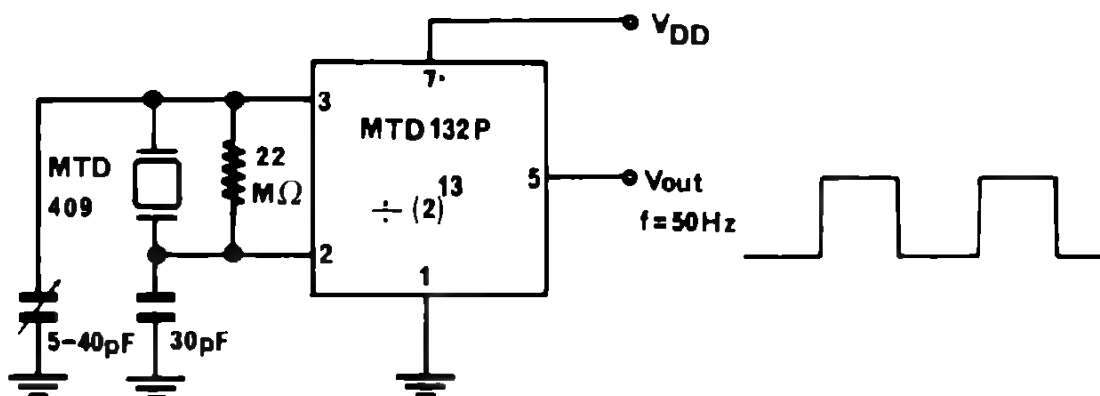
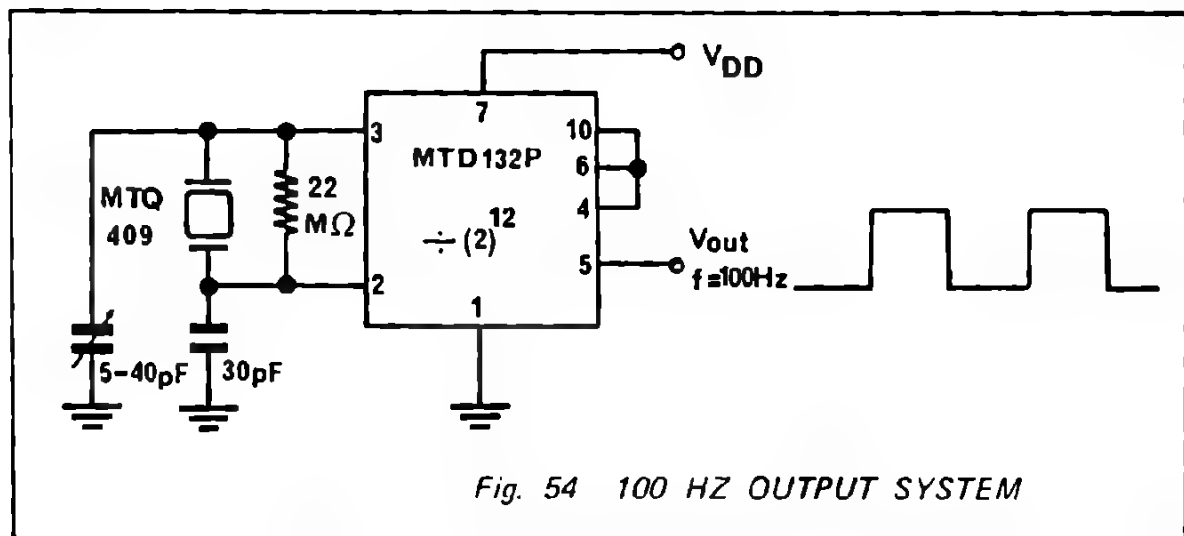


Fig. 53 50 HZ OUTPUT SYSTEM

7. 100 Hz OUTPUT SYSTEM

The base frequency of this system is also the 409 KHz, and the components used are MTQ 409 crystal with MTD 134P, of which 12 stages are used as shown in Figure 54.

Applications: stop clocks for sport competition timing.



3. ONE-PULSE-PER-DAY TIME BASE SYSTEM

An oscillator frequency of 397.682157 KHz, when divided by 34 binary stages, will produce one output pulse every day. The pulse width is cut down to 20 m by using an intermediate frequency output to reset the buffer flip-flop of the last circuit. This system can be built with one MTD 133P plus two MTD 135P. See Figure 56.

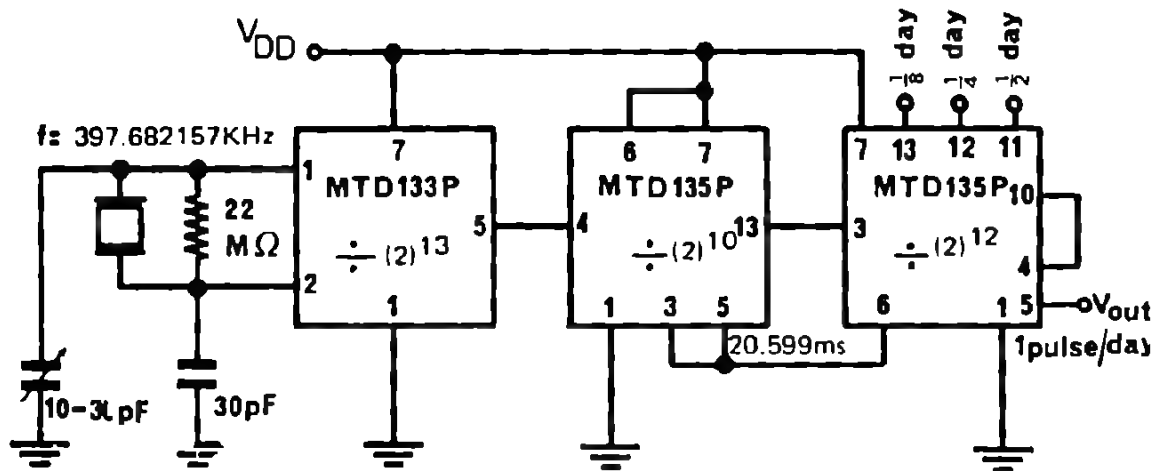


Fig. 56 ONE-PULSE-PER-DAY SYSTEM

4. ONE-PULSE-PER-MONTH TIME BASE SYSTEM

Finally, to obtain one impulse every month (12 pulses per year), the oscillator frequency of 418.097052 KHz is divided by 39 stages. The pulse width of the diagram shown in Figure 57 is reduced to some 20 ms.

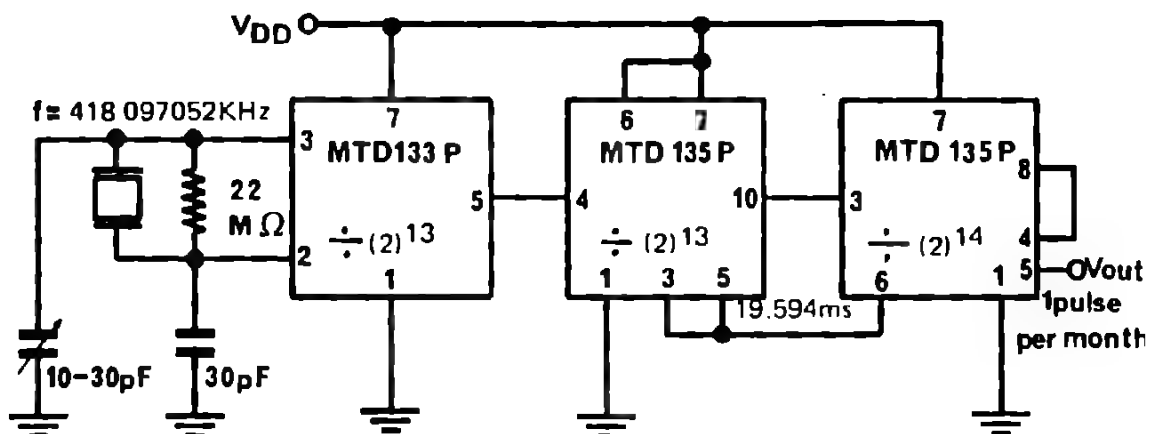


Fig. 57 ONE-PULSE-PER-MONTH SYSTEM

3 PRACTICAL HANDLING OF COMPONENTS

1. CRYSTAL

Although quartz crystals of the NT cut type are well protected against shocks, due to the 4 point suspension, it is suggested to take the required care when handling them. Figure 58 shows a cross section through an MTQ 32. It can be seen that the connection leads pass through a glass isolation.

When the crystal leads are bent, care must be taken not to exert any pulling force on these leads, as such a force may cause a shift of the crystal frequency. To avoid breaks of the glass isolation, it is important to observe a minimum distance of 1 mm between glass and lead bend, as shown in Figure 58.

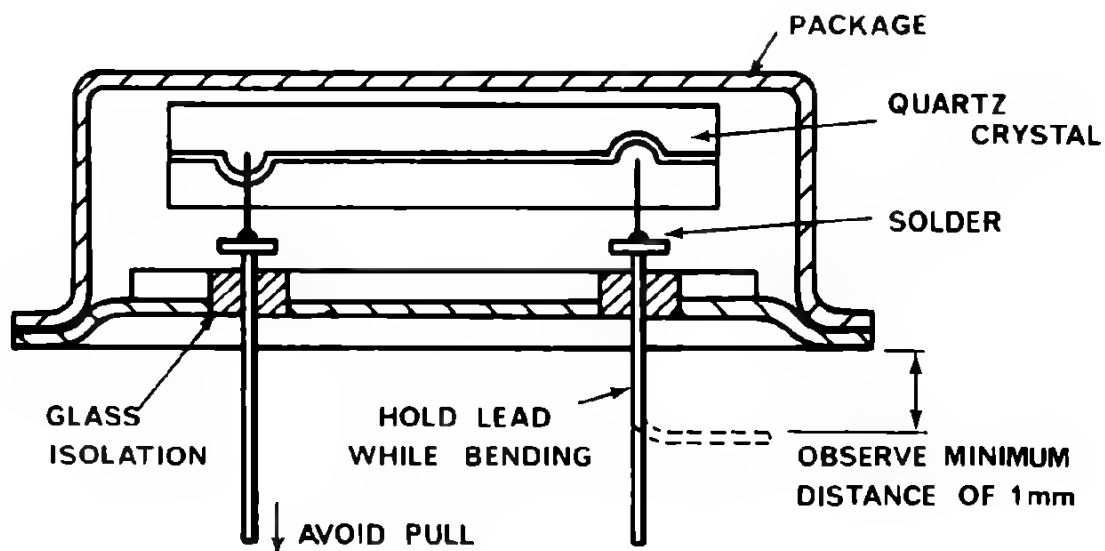


Fig. 58 CROSS SECTION OF A WATCH CRYSTAL

It is recommended to use a shock absorbant material when mounting the crystal on the PC board. This can be done by applying a drop of silicone rubber (General Electric RTV-112) between crystal case and PC board, or by putting a foam sleeve over the whole crystal package. Various other methods like spring-mounting can be recommended.

The crystal leads can be soldered with 60/40 lead tin solder for a maximum of 10 seconds at 234°C.

2. INTEGRATED CIRCUITS

All MOTOROLA Silicon Gate CMOS ICs contain circuitry to protect the inputs against damage to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages (normally 3V) to these high impedance circuits. In particular, it is useful to

- work on benches covered with a grounded metal plate
- use well grounded equipments only
- ground the tip of the soldering iron
- avoid nylon carpeting causing static charges
- use grounded tweezers to handle the ICs rather than touching them with the hands.

If the leads of the ICs have to be bent for mounting, they should be held with a tool to avoid mechanical stress on the glass sealing, as shown in Figure 59. Solder should be kept at a minimum distance of 1 mm from the ceramic package.

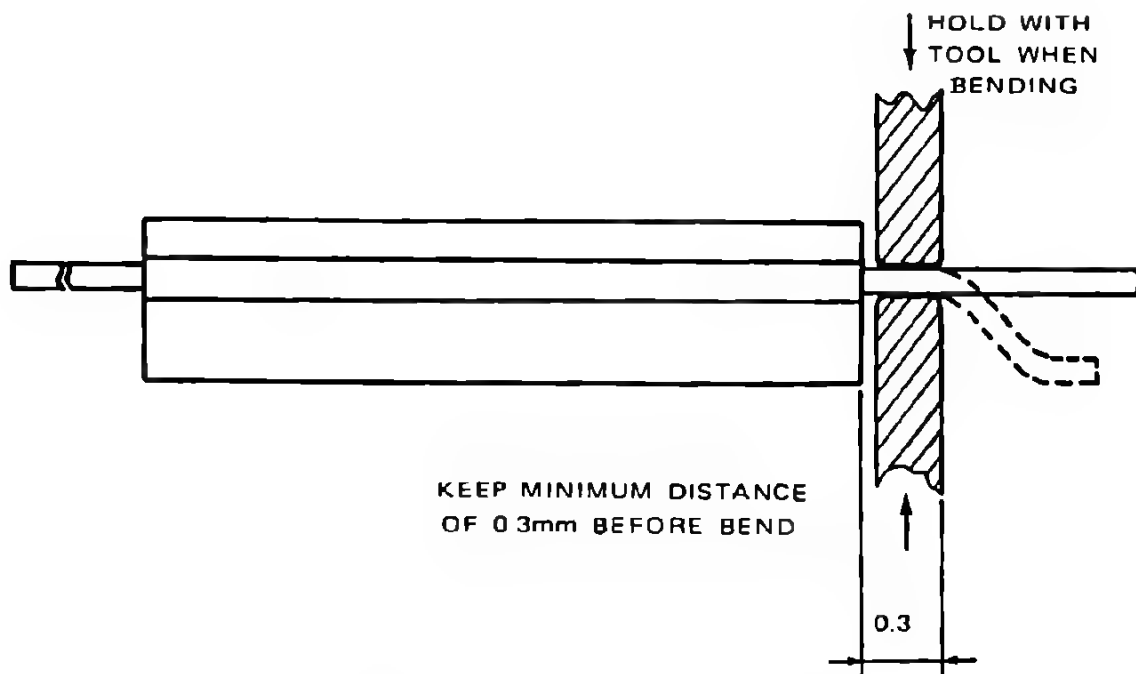


Fig. 59 LEAD BENDING OF CERAMIC IC PACKAGE

MOTOR

1. HANDLING

Greatest care must be taken when handling the miniature motors. The metal shield around the motor is part of the magnetic circuit. Any handling of the motor shield with pliers or tweezers must be avoided, as it may distort the shield and cause malfunction of the motor.

Therefore, it is best to handle the motor by its leads and its bearing boss.

2. SOLDERING

It is recommended to solder the leads of the motor to the PC board with low temperature solder (e.g. Ersin 461/14) at a maximum soldering iron temperature 200°C for 2 seconds max..

3. MOUNTING

It is suggested that the bearing boss be used to position the motor with reference to the gear train. Holes in the plastic bobbin allow to retain the motor in place by two selftapping screws (Fig. 60). The motor can also be glued to the base with silicon rubber (General Electric RTV-112).

The motor should be placed on a nonmagnetic mounting plate and away from magnetic materials.

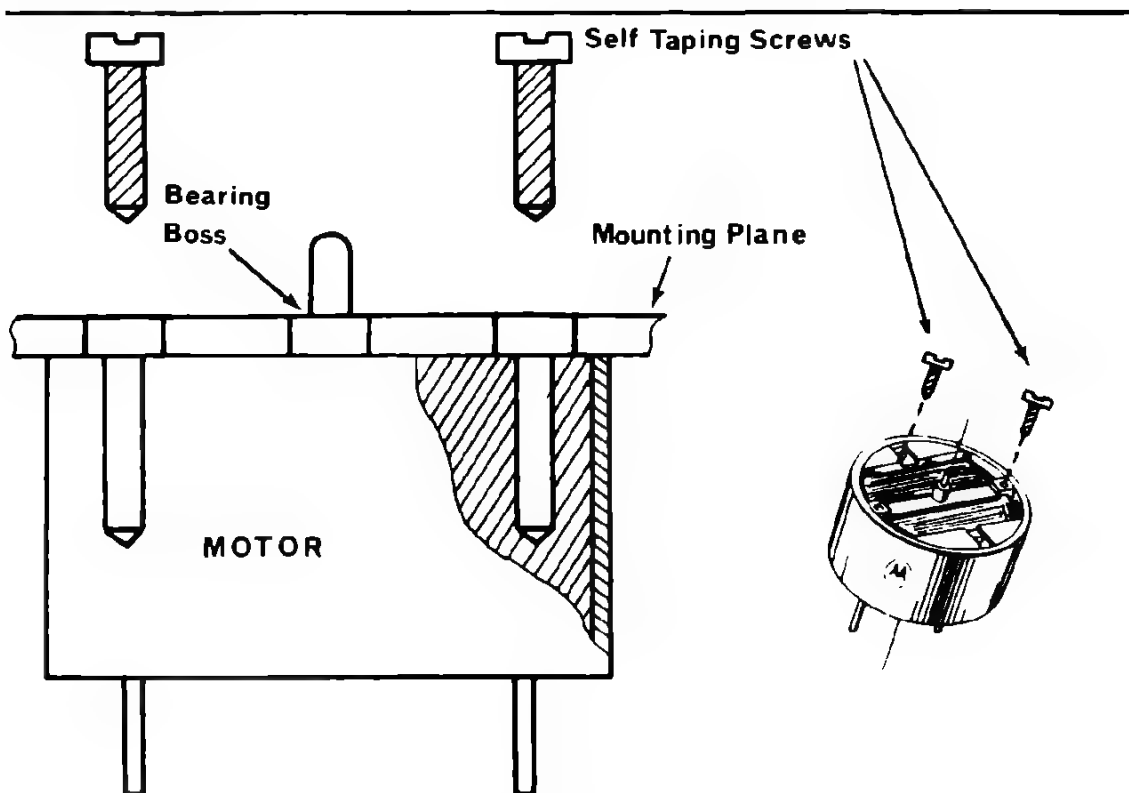


Fig. 60 MOTOR MOUNTING

3. 4. DRIVE PINION

Following precautions should be taken when mounting the drive pinion (non magnetic material) to the motor axle:

- support the opposite end of the axle so that all force is taken by the axle and not by the rotor or the bobin
- apply force parallel to the axis of the axle
- do not exceed 2 kg force applied to the end of the axis in a direction parallel to the axle.

4. TRIMMER

In order to minimize external influences of the frequency while trimming, it is recommended to position the trimmer such that the rotor terminal is connected to the circuit ground.

F MEASUREMENT TECHNIQUES

1. INCOMING INSPECTION AND AQL

1. 1. AQL (=ACCEPTABLE QUALITY LEVEL)

MOTOROLA Timepiece Electronics' systems and components are supplied to a well defined level of quality.

Supplier and user agree to a specific AQL (Mil. Std. 105D) value, which then becomes the base for the suppliers outgoing and the users incoming inspection of every shipped lot of systems or components.

The base of the AQL sampling plan is the MIL STD 105D, which indicates how many samples of a given lot size must be pulled and tested, and how many maximum rejects are allowed to be found in order to accept the lot.

Example (see also appendix 4, AQL table):

Assume:

lot size is 1000 pcs

AQL = 1%

Then:

80 samples must be pulled at random (level II):

- if up to 2 rejects of a parameter group (to be specified) are found, the lot is accepted on this group
- if 3 or more rejects of that group are found, the lot is rejected on this parameter group.

1. 2. INCOMING INSPECTION PARAMETERS

Items to be inspected on TPE products are essentially:

Integrated circuit:

- a) mechanical dimensions
- b) oscillator start voltage
- c) frequency test according to min/max Δf method
- d) output pulse
- e) current drain

Crystal:

- a) mechanical dimensions
- b) frequency test according to min/max Δf method described in Figure 33.

Motor:

- a) mechanical dimensions
- b) torque
- c) winding resistance

Trimmer

- a) mechanical dimensions
- b) capacity range

2. ASSEMBLY TEST

Following the assembly operations of the electronic module, a systems test will be required.

This test will include inspection criteria as follows:

2. 1. VISUAL INSPECTION

Solder connections

Positioning of components

2. 2. ELECTRICAL TEST

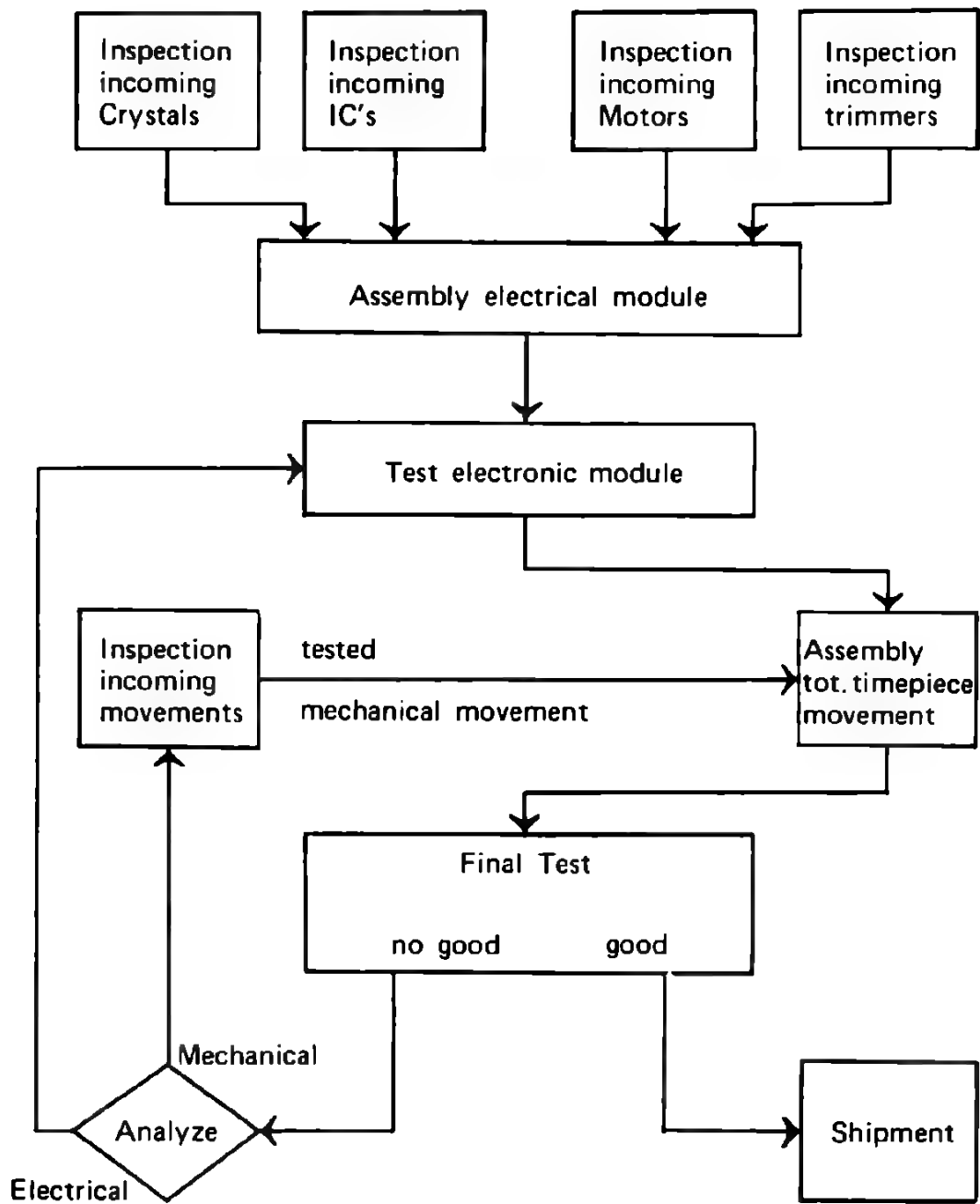
Frequency trimmability

Oscillator start voltage

Output pulse or torque (if the motor is part of module)

Current drain.

3 SUGGESTED FLOW CHART FOR A COMPLETE PROCEDURE OF ELECTRONIC TIMEPIECE ASSEMBLY



EQUIPMENTS

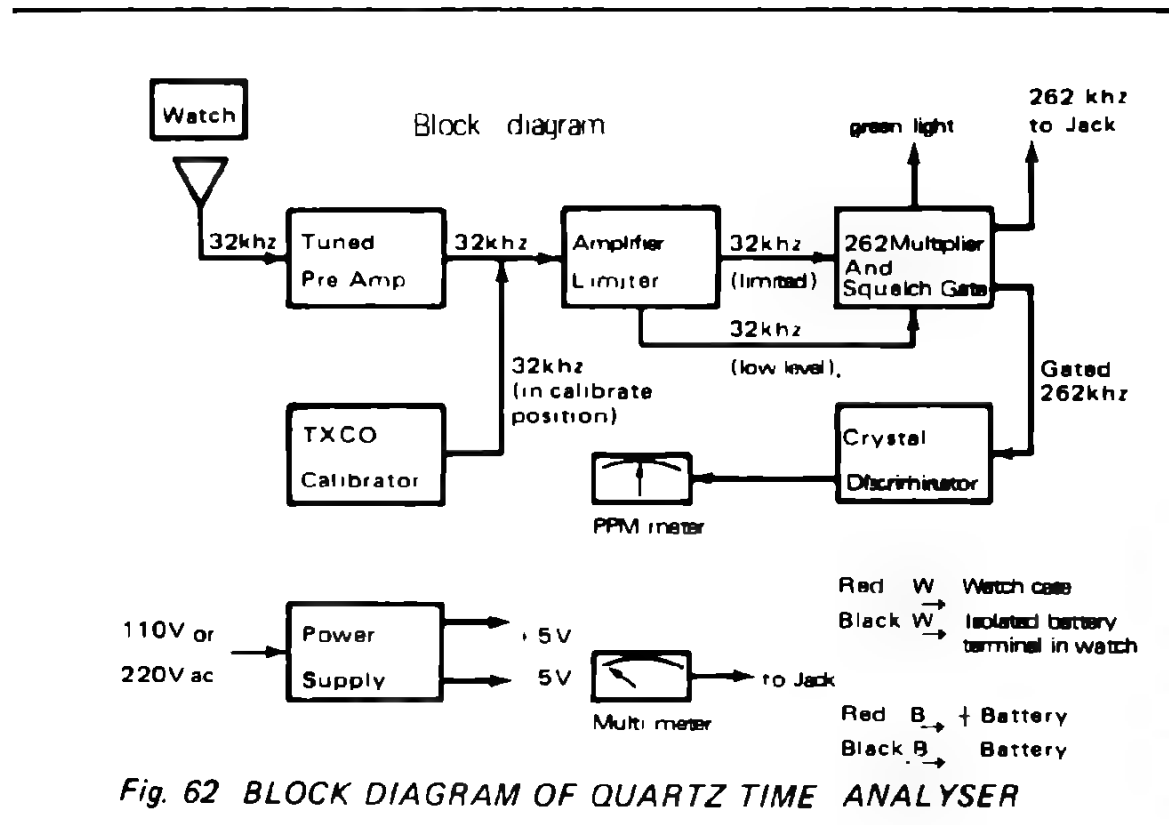
1. QUARTZ TIME ANALYZER (QTA)

The QTA (Fig. 61) is a unique instrument for production use. Without any connections, it allows to make fast frequency tests on components, sub-assemblies, assemblies and the final (but still open) watch.



The instrument picks up the high frequency radiation of the oscillator circuit and compares it to an internal high precision time reference (3.2768 MHz TCXO). The error signal is fed to an analog instrument and displayed directly in parts per million and seconds per month. Figure 62 shows the block diagram of the QTA.

The Quartz Time Analyzer was specially designed for Timepiece Electronics application (laboratory and production line).



I. 2. ADDITIONAL EQUIPMENTS

In addition to the QTA, a number of other instruments are of interest. The following lists a few of them:

Precise Ampere Meter

Ex. HP 412A — analog multimeter with DC-voltage ranges and ohm ranges

Oscilloscope

Ex. Tektronik Series 550–560

Power supply voltage

Ex. Minireg: Series 400 classical power supply

Power design model 2005

more sophisticated

digitally adjustable

with high accuracy

A frequency counter has proved to be very useful in a laboratory.

Recommended type:

HP counter type 5326A

or HP counter type 5326B with DVM DC-voltage.

All inquiries concerning timepiece electronics components
should be addressed directly to:

MOTOROLA Inc.
Timepiece Electronics
P.O. Box 8
1211 GENEVA 20 – Switzerland
Telex 23905
Telephone (022) 335607

APPENDIX

POWERS OF 2

Number Sequence for Division by Two

n	2 ⁿ
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1,024
11	2,048
12	4,096
13	8,192
14	16,384
15	32,768
16	65,536
17	131,072
18	262,144
19	524,288
20	1,048,576
21	2,097,152
22	4,194,304
23	8,388,608

2. TIMING ERROR TABLE

Timing Error versus Frequency
Change in Parts/Million (PPM)

$\Delta F/F$ (PPM)	Sec. Per Day	Sec. Per Month	Minutes Per Month	Minutes Per Year
1	0.0864	2.628	0.0438	0.5256
2	0.1728	5.256	0.0876	1.0502
5	0.432	13.14	0.219	2.628
10	0.864	26.28	0.438	5.256
20	1.728	52.56	0.876	10.502
50	4.32	131.4	2.19	26.28
100	8.67	262.8	4.38	52.56

3. TIME CONVERSION TABLE

Time Conversion Tables

	DAY	MONTH	YEAR
Seconds	86,400	2,628,000	31,536,000
Minutes	1,440	43,800	525,600
Hours	24	730	8,760

AQL TABLE

Acceptance
number
Rejection
number

Use first sampling
plan below arrow. If
sample size equals,
or exceeds, lot or
batch size, do 100
percent inspection.

Use first sampling
plan above arrow.

TABLE I sample size code letters				TABLE II-A Single sampling plans for normal inspection (Master table)																												
Lot or batch size	General Inspection Level Used		Sample size code letter	Sample size n	Acceptable Quality Levels, normal inspection (%)																											
	I	II			0.100	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000	1500	2500	4000	6500	10000		
2 to 8	A	A	A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
9 to 15	A	B	B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
16 to 25	B	C	C	4	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
26 to 35	C	D	D	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
36 to 50	C	E	E	6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
51 to 80	D	F	F	7	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
81 to 150	D	G	G	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
151 to 280	E	H	H	9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
281 to 500	F	I	I	10	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
501 to 1200	F	J	J	11	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
1201 to 3200	G	K	K	12	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
3201 to 10000	H	L	L	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
10001 to 35000	H	M	M	14	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
35001 to 150000	I	N	N	15	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
150001 to 500000	I	O	O	16	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
500001 to 1500000	J	P	P	17	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
1500001 to 5000000	J	Q	Q	18	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
5000001 and over	K	R	R	19	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	

5. BATTERY REFERENCE DATA

5. 1. WATCH BATTERIES

Silver Oxide Batteries

Manufacturer	Type No.	Diameter (mm)	Height (mm)	Rating (mA-hr)	Voltage (V)
Eveready (U.C.)	EPX77	11.56	5.59	165	1.58
Mallory	WS14	11.56	5.33	165	1.58
Ray-O-Vac	RW12	11.56	5.59	175	1.58
Ray-O-Vac	RW32	11.56	5.59	245	1.58
Ray-O-Vac	RW34	11.56	4.06	170	1.58

Mercury Batteries

Manufacturer	Type No.	Diameter (mm)	Height (mm)	Rating (mA-hr)	Voltage (V)
Eveready (U.C.)	354	11.56	4.19	150	1.35
Eveready (U.C.)	313	11.56	5.33	220	1.35
Mallory	WH3	11.56	5.28	220	1.35
Leclanché	MR42NM	11.60	3.60	140	1.36
Leclanché	MR43NM	11.60	4.20	160	1.35
Leclanché	MR44NM	11.60	5.40	200	1.35
Varta	7001	11.60	5.40	230	1.35

5. 2. CLOCK BATTERIES

Alkaline Batteries

Manufacturer	Type No.	Diameter (mm)	Height (mm)	Rating (mA-hr)	Voltage (V)
Mallory	MN1500	14.2	50.0	1800	1.5
Mallory	MN1400	24.4	50.0	5000	1.5
Union Carbide	E91	14.0	49.5		1.5
Union Carbide	E93	25.8	49.2		1.5
Varta	7244	14.5	50.5	1800	1.5
Leclanché-SAFT	R14S	25	49.5		1.5

Mercury Batteries

Manufacturer	Type No.	Diameter (mm)	Height (mm)	Rating (mA-hr)	Voltage (V)
Mallory	ZM9C	14.2	50.0	2400	1.4
Leclanché	MR90	14.1	49.5	2400	1.4

5. SYSTEMS CHOICE CHART

Required Output Frequency	Output: U Unipolar B Bipolar	Output Pulse Width (ms) (VAR: Variable)	SECOND IC		FIRST IC		CRYSTAL			Primary Application
			Type	No. of Stages	Type	No. of Stages	Type	Frequency (KHz)	Factorized Frequency (Hz)	
$\frac{1}{60}$	U	VAR	MTD134P	11	MTD132P	13	MTQ279	279.620267	$2^{24} \cdot 60$	CLOCK
1	U	500	MTD134P	14	MTD134P	15	MTQ32	32.768	2^{15}	CLOCK
1	U	VAR			MTD134P	4	MTQ262	262.144	2^{18}	CLOCK
1	B	32			MTD161F	16	MTQ32	32.768	2^{15}	WATCH
1	B	32*			MTD181F	18	MTQ131	131.072	2^{17}	WATCH
2	U	VAR	MTD134P	12	MTD134P	15	MTQ32	32.768	2^{15}	CLOCK
4	U	125			MTD131F	13	MTQ32	32.768	2^{15}	WATCH
4	U	VAR			MTD134P	13	MTQ32	32.768	2^{15}	CLOCK
5	U	3			MTD161F	16	MTQ327	327.680	5.2^{16}	CLOCK
5	U	VAR			MTD134P	4	MTQ327	327.680	5.2^{16}	CLOCK
8	U	62			MTD131F	13	MTQ65	65.536	2^{16}	WATCH
8	U				MTD134P	15	MTQ262	262.144	2^{16}	CLOCK
10	U	50			MTD134P	15	MTQ327	327.680	10.2^{15}	CLOCK
32	U	16			MTD132P	13	MTQ262	262.144	2^{18}	CLOCK
50	U	10			MTD134P	12	MTQ409	409.600	100.2^{12}	CLOCK

*Other pulse width on metal options.

7. FREQUENCY DIVISIONS

CRYSTAL		FREQUENCY AFTER DIVISION BY N STAGES												N=			
Type	Frequency (KHz)	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
MTQ32	32.768	32	16	8	4	2	1	0.5									
MTQ65	65.536	64	32	16	8	4	2	1	0.5								
MTQ131	131.072			32	16	8	4	2	1	0.5							
MTQ262	262.144				32	16	8	4	2	1	0.5						
MTQ279	279.620267												$\frac{1}{7.5}$	$\frac{1}{15}$	$\frac{1}{30}$	$\frac{1}{60}$	
MTQ327	327.680	320	160	80	40	20	10	5	2.5	1.25							
MTQ409	409.600		200	100	50	25											
XTQ524	524.288						16	8	4	2	1	0.5					

8. REFERENCES

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John P. Buchanan, "Handbook of Piezoelectric Crystals for Radio Equipment Designers", Wright Air Development Center, 1956, Wright-Patterson Air Force Base, Ohio.

F.H. Musa and R.G. Daniels, "The Crystal-Controlled Electronic Wristwatch System: A Silicon-Gate C-MOS-MSI Approach" Proceeding of 25th Annual Symposium on Frequency Control, sponsored by U.S. Army Electronics Command, Fort Monmouth, New Jersey.

J.K. George, "C-MOS Aluminium Gate and Silicon Gate Processing for Watch/Clock Circuits", Proceeding of the 1972 EPN International Electronics Seminar, Paris, France, April 7, 1972.

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C. Brugger, "Systèmes intégraux de base de temps pour montre à quartz et pendulette". *Société Suisse de Chronométrie*, October 13, 1972.

CHAPTER 13

Custom Design

CUSTOM DESIGN



- A INTRODUCTION**
- B CUSTOMER -
MANUFACTURER
INTERFACE**
- C MOTOROLA'S
EUROPEAN DESIGN
OPERATIONS**
- D COMPLEXITY AND
ECONOMY OF
LSI CIRCUITS**
- E DEVELOPMENT
PHASES OF A CMOS
CUSTOM IC**

A INTRODUCTION

Let's first step backwards in the history to the beginning of the digital integrated circuit technology, starting with the RTL family. The complexity of these circuits was mainly given by technological limitations. However, the implementation of logic modules of the first order such as Gates, Flip-Flops, etc. was feasible and yielded a limited range of a few dozen logic modules.

The second generation of a logic family which was based on an improved technology, allowed the implementation of more complex circuits, e.g. counters, decoders, shift registers, etc. The higher circuit complexity which resulted yielded a larger number of logic modules.

Today, very complex logic modules up to single chip calculators are implemented using MOS technology. The very large circuit complexity is one of the main characteristics of the MOS technology and will yield a very high variety of logic modules. Therefore, a standardization of logic modules is becoming more and more difficult. Best use of the large-scale integration (LSI) capability of the MOS technology will be achieved by relating the integrated circuit design to the particular project. This means that the semiconductor manufacturer becomes more and more involved in the design of systems rather than in the design of standardized logic building blocks which in the past was entirely up to the systems manufacturer. This fact raises the requirement for a new kind of cooperation between systems and semiconductor manufacturers.

B CUSTOMER — MANUFACTURER INTERFACE

As explained in the previous section, with the progress of LSI technology, the semiconductor manufacturer is taking over more and more of the design work previously done by the systems house. Because of this, the systems manufacturers are forced to modify their design procedures.

Initially, the systems house needs to have an exact understanding of the systems function in order to give the semiconductor manufacturer a detailed functional description or specifications of the logic involved for the particular project. This is essential in order to avoid changes of the logic in a later development phase of the integrated circuit which could cause significant delays in the design.

The semiconductor manufacturer should be consulted on problems concerning the realization of the logic. Due to his wide experience he will be able to give assistance to the systems design. In addition, his CAD facilities are useful tools in order to optimize and speed up the circuit design.

Summarizing, we can say that both, the systems "know how" of the systems manufacturer and the "know how" on integrated circuit technologies of the semiconductor manufacturer are required for the development of a complex circuit. A close cooperation of the two is essential to obtain an optimum product.

C MOTOROLA'S EUROPEAN DESIGN OPERATIONS

In order to enable a close cooperation with the European customers on the design of complex circuits, MOTOROLA has established a complete design operation in Europe, located in Geneva. This center is equipped for the IC design of digital and linear circuits, implemented in MOS (CMOS, N-channel, etc.) or bipolar technology.

All design activities including circuit design and simulation, layout design and artwork generation are performed entirely at this center. Processing of the prototypes also is done at one of MOTOROLA's European plants. The necessary engineering of the prototypes can be performed at the design center with the center's own LSI test equipment.

The European design operation is well equipped with a large range of CAD facilities. For the digital circuit design, the following computer programs are available :

- DC analysis (non linear)
- Transient analysis
- Logic simulation, suitable for synchronous and asynchronous logic
- Test sequence check program

Computer facilities are also applied to the layout generation. The following methods illustrate to what extent and to what benefit the computer can be utilized.

1. Manual method :

This method is characterized by customized hand layout generation. Repetitive logic structures will be implemented in custom made cells which will be placed and connected manually. This method yields the smallest chip size possible. The main disadvantage of this method is the long time required for layout generation.

2. Standard cell method (Polycell LSI) :

This approach is based on a standardized family of logic cells such as gates, flip-flops, shift register cells, etc. These cells are stored in a computer library. The placement and interconnection of these cells is usually done by computer. It can also be done manually. Checkplots of the layout are drawn by a plotter. The actual artwork is obtained from a ruby cutter, a photo plotter or a pattern generator.

Very short development time for layout, artwork generation and lower development cost are the attractive features of this approach. However, this approach does not yield optimum chip size and hence does not produce the minimum price possible. Therefore, it mainly is used for low volume production projects.

3. Customized cell method

This approach represents a mixture of the two above mentioned methods. Each particular project is carefully analyzed and split into suitable cells. Some of the cells might be taken from a standard cell family, the others are customized.

The placement and connection is done manually. In order to minimize the drafting work for the layout, to achieve flexibility for layout modifications and to generate the artwork on a plotter, a computer controlled interactive graphics system is utilized.

This approach will result in a sufficiently small chip size and in a reasonably short development time.

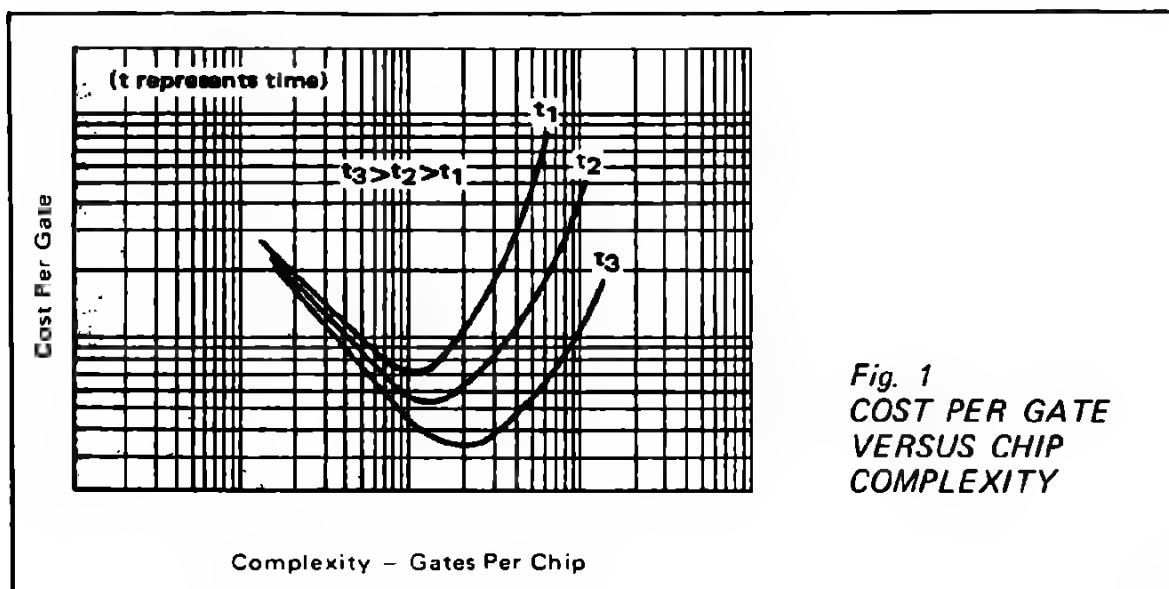
At our European design center the last mentioned customized cell method has been chosen and a complex computer controlled interactive graphic system has been installed. This is in accordance with the general policy to develop and to produce medium and large volume products.

D COMPLEXITY AND ECONOMY OF LSI CIRCUITS

Speaking about the complexity of an integrated circuit mainly means speaking about the volume of logic implemented on a single chip which can be expressed in the number of gates per chip. In order to study the economy of a system implemented in LSI circuits, the cost of an integrated circuit as a function of the complexity is of interest.

The cost of an integrated circuit is mainly given by the cost of the chip and the packaging cost. The latter one depends on the number of pins of the package and on the package material. On a given technology the chip size gives the cost of the chip where also the relationship between the chip size and the average wafer probe yield is essential.

Figure 1 shows the typical relationship between the complexity and the cost per gate which can be generated for a given technology. The cost per gate decreases towards an optimum value by increasing the chip size. Below this optimum value of the chip complexity the cost per gate is dominated by packaging and testing costs that are incurred on a unit base. Above this optimum value the decrease of yield causes the chip cost to become dominant. In fact, the minimum cost per gate point is a measure of the production state of the art. As continuous development improves the tomorrow's semiconductor technology, the optimum value of chip complexity will gradually increase.



Before studying the economics in further detail, it can be summarized that the complexity of an integrated circuit influences the cost per gate. The development of an extremely small circuit is often questionable. The cost per gate will increase such that one approaches an economical limitation by the low complexity of the circuit. However, to make it economically feasible, the fractional development cost has to become a negligible portion of the price which means in this case very high volume production.

On large systems the designer has to optimize the economics by the partitioning. The goal obviously is to minimize the overall systems cost. The chip size range has to be selected in order to be economical for the period of the production. An additional cost factor, final equipment packaging, should also be considered in partitioning. As the chip complexity is increased, fewer chips are required and the overall assembly costs on a per gate basis are reduced. The effect of equipment packaging is that the economical chip size will be somewhat higher as indicated by semiconductor considerations alone. The partitioning preferably is done in cooperation with the systems and the semiconductor manufacturer since both know their costs involved and their goals.

Regarding the economy of an LSI approach the development cost of the IC always has to be considered. Depending on the complexity of the circuit, the development cost of an IC can be up to \$ 50,000. For an economical IC approach considerably high production quantities are always involved in order to reduce the fractional development cost per IC. The economy of an LSI approach may be illustrated on the following example. This example demonstrates that even assuming the same cost for the integrated circuits for both approaches yields considerable saving in the total cost of the LSI approach.

	CMOS APPROACH		CMOS LSI APPROACH	
	1 pc-board with 50 IC's		0.2 pc-board with 2 IC's	
	\$	\$	\$	\$
Integrated circuits	40 x 1.20	48.00	2 x 24.00	48.00
PC-board incl. assembly	1 x 10.00	10.00	0.2 x 10.00	2.00
Test of PC-board	1 x 4.00	4.00	0.2 x 4.00	0.80
Connections	1 x 2.00	2.00	0.2 x 2.00	0.40
System wiring	1 x 4.00	4.00	0.2 x 4.00	0.80
Case (partly)	1 x 4.00	4.00	0.2 x 4.00	0.80
Power supply (200mW)		2.00		2.00
Fractional IC dev. cost at the volume of 60K				1.00
TOTAL COST		74.00		55.80

The calculation on the above example shows the cost saving by implementing an LSI approach in a complex digital system. This example will be typical for complex digital systems, however, it will not be applicable to every application since it is based on some assumptions.

This calculation has been done on a pc-board base. With the standard CMOS approach 40 packages will be replaced by two LSI circuits, packaged in 24 or 40 pin DIP's. Under the assumption that 10 LSI circuits may be placed on the same size pc-board, the system package density will be 5 times higher as for the standard CMOS approach and will yield to cost saving on the systems level.

At this point the reliability advantages of the LSI approach should also be mentioned. Since the failure mechanisms of the standard CMOS and the LSI approach are the same, the total bonding count and soldering count become essential in considering system reliability. Due to the higher circuit complexity of the LSI approach in the above example, the total number of connections will be reduced by approximately a factor of 8. This will yield a remarkable increase in system reliability.

E DEVELOPMENT PHASES OF A CMOS CUSTOM IC

MOTOROLA's design operation can handle designs at different development stages. Black-box specifications of a system or logic diagrams or something in between can be the starting point. In any case it is suitable to establish good communications between the system designer and the IC designer as early as possible to be able to find better and cheaper ways to design a system. Not only pin count has to be taken into consideration during the development but also system speed, maximum die size for a given package, package price, etc.. To be economical, logic and system design have to be fitted to the CMOS technology. Transmission gates and dynamic logic for example were not used in older technologies like TTL, but can be used to a great extent in the CMOS technology. Generally speaking, some types of gates (e.g. functional gates) or flip-flops are more suitable than others for a given technology, and often an extensive rethinking of the system or logic supplied by the customer has to take place before starting integration.

The system design is an intermediate step between the black-box specification of the system and the logic diagram. The different functions that the system has to perform are implemented on a system diagram using big functional blocks (like shift registers, ROM's, adders, etc.). The chosen technology has an influence upon system design. Speed considerations for example might dictate a parallel structure rather than a serial one for a section of the system. The fact that CMOS has extremely high input impedance allows to use capacitive storage and dynamic operation for some sections of the circuit. This is very interesting in terms of speed and total chip size area. The following steps of the development of the IC (partitioning and logic design) can also have a retroactive influence on the system design.

Partitioning:

The success of complex circuit integration is heavily dependent upon an intelligent system partitioning. In building up systems with standard small integrated circuits, it is for economical reasons important to limit the number of gates. However, in integrated circuit design (MSI or LSI) the number of gates is not so important, but minimization of external connections to the package (pin,count) is mandatory. One can get to such an extent that sometimes serial data transmission is used in order to save pins in spite of the additional logic involved. The partitioning is predominantly dictated by:

- available economical packages
- pin count
- cavity size of the package
(possible maximum die size a package can house)
- technological/economical chip size limitations
- power dissipation limitations
(for CMOS not applicable except for driver circuits).

Logic Design:

Considerable expertise is necessary in this field. Philosophies of logic design which are applied in discrete design are not always applicable in LSI logic design. The interconnection area of a chip can be as big as the active area. Therefore, it might sometimes be interesting to introduce additional logic when this allows significant area saving in the interconnection area. In the system design section, dynamic techniques and the high input impedance characteristic of MOS devices were mentioned. Transmission gates which are very simple structures in MOS, are extremely useful, especially for clocking purposes and in some cases for logic simplifications. Since today's LSI circuits have a very impressive complexity, the logic has to be verified before the actual lay-out work can start. In MSI-LSI design, errors are very expensive and, therefore, techniques for checking the logic design have been developed. There are two ways to do this: Computer simulation and breadboarding. Breadboarding of CMOS systems can very often be used because the wide range of standard products offered by MOTOROLA makes it possible to implement many different kinds of logic function. However, for larger systems it is more convenient, and most of the time mandatory to use computer simulation. Logic simulation can be performed for complex circuits up to the system level (over 4000 gates) by computer programs, developed by MOTOROLA.

Circuit Design:

As explained earlier, a cellular approach is used for the lay-out. The cells are the building blocks of the circuit, each type of cell corresponds to one logic gate or logic block. The first thing is to decide which cells are needed for a given circuit. Some of the cells will be custom designed, some will be picked out of the computer library of our graphic system. All the cells are then thoroughly checked out for the given operating range (power supply and temperature range, speed, etc.). The verification is done by performing AC and DC electrical simulation by means of computer programs. These programs, also developed by MOTOROLA, use sophisticated transistor models including such effects as channel length modulation, surface mobility degradation, etc.. The DC simulation program can for example plot transfer characteristics (output voltage or current as a function of the input voltage or current) and it includes also a so called solveback feature (that means that it can calculate which input voltage produces a given output voltage).

The AC simulation program has been made very efficient by using sparse matrix inversion techniques so that the behavior of circuits including up to 80 transistors and 100 modes can be simulated by using only a few minutes of computer time.

Lay-out:

As soon as the logic is determined and simulated, and the cells are designed and analyzed, the lay-out can start. As we have seen in the partitioning of the whole system, it is equally important to generate a good topological plan of the chip. For economic reasons this is performed manually (unless total computer lay-out techniques are used).

The topological plan is then used to place the cells. At the same time the interconnections between the different cells and the input/output pads are drawn together with the cell outlines (only origin of cell and cell name are indicated) on a mylar sheet. A grid arrangement is on the mylar sheet, and this must be very accurate in order to enable the digitizing of this composite drawing.

Digitizing and Mask Preparations:

After the lay-out of a circuit has been completed and carefully checked out, it is digitized, i.e. numerically coded with a machine called Digitizer, and automatically stored in our graphic system. A plot of the stored information is then drawn automatically including the inside of the cells. This can now be compared with the original composite drawing as well as with check plots of the individual cells. Since errors can be generated during digitizing, a special editing station is available on the graphic system. Also modifications can be introduced and both tasks can be performed very fast thanks to the interactive nature of the graphic system. This system is also equipped with automatic lay-out violation detection programs.

Now the artwork is ready for photoreductions and step-and-repeat operation. MOTOROLA's European production facility, fully compatible with the US Production facilities, will then process the prototypes.

The organization of the graphic system is shown in Figure 4. A mini-computer drives three or more stations in time sharing:

A digitizing station where the drawings are numerically coded (drawings of cells or composite drawings showing the placement of the cells and the interconnect) and sent to the memory of the computer. A cathode ray tube can be assigned to the digitizer section to assist in this work.

An editing station where a cathode ray tube is used in conjunction with a data tablet to modify a lay-out.

A plotting and mask cutting station where check plots are made and mask layers are cut on rubilith.

The computer library is stored on a magnetic disc. Magnetic tapes are also used to store some part of the library which is not used very often or description of finished circuits.

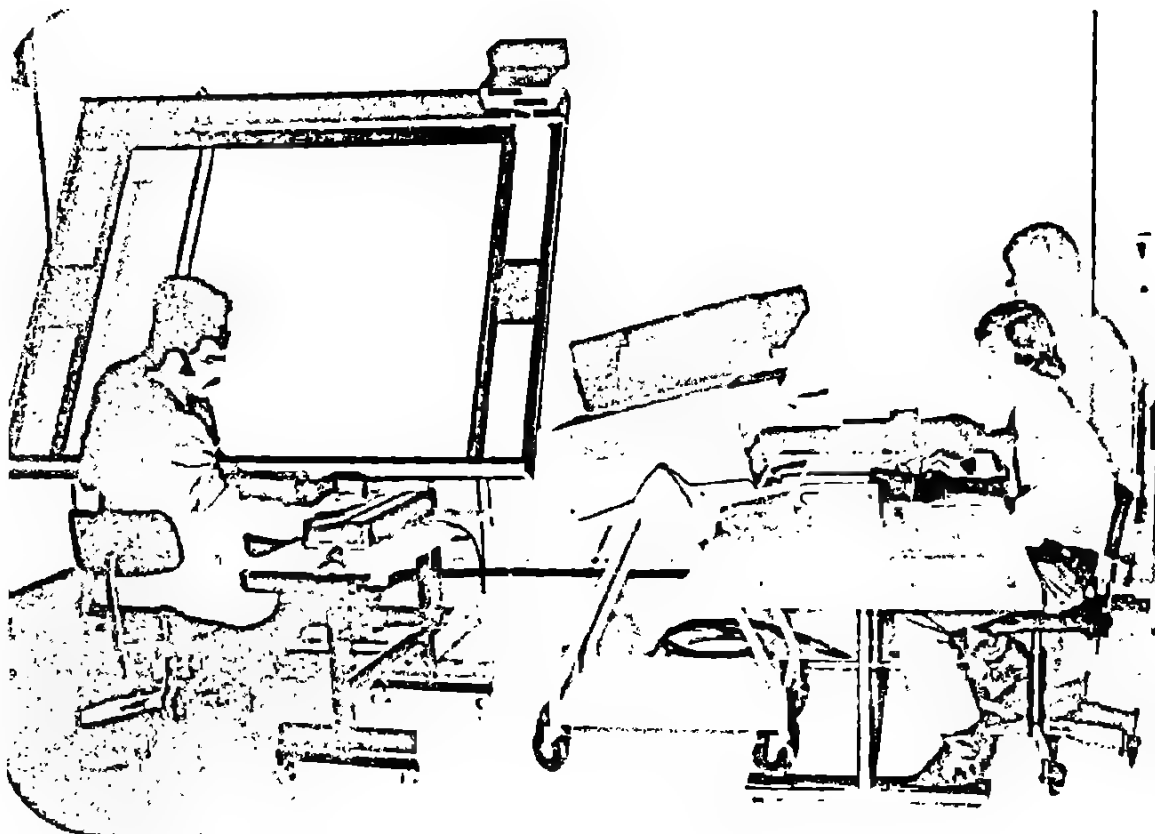
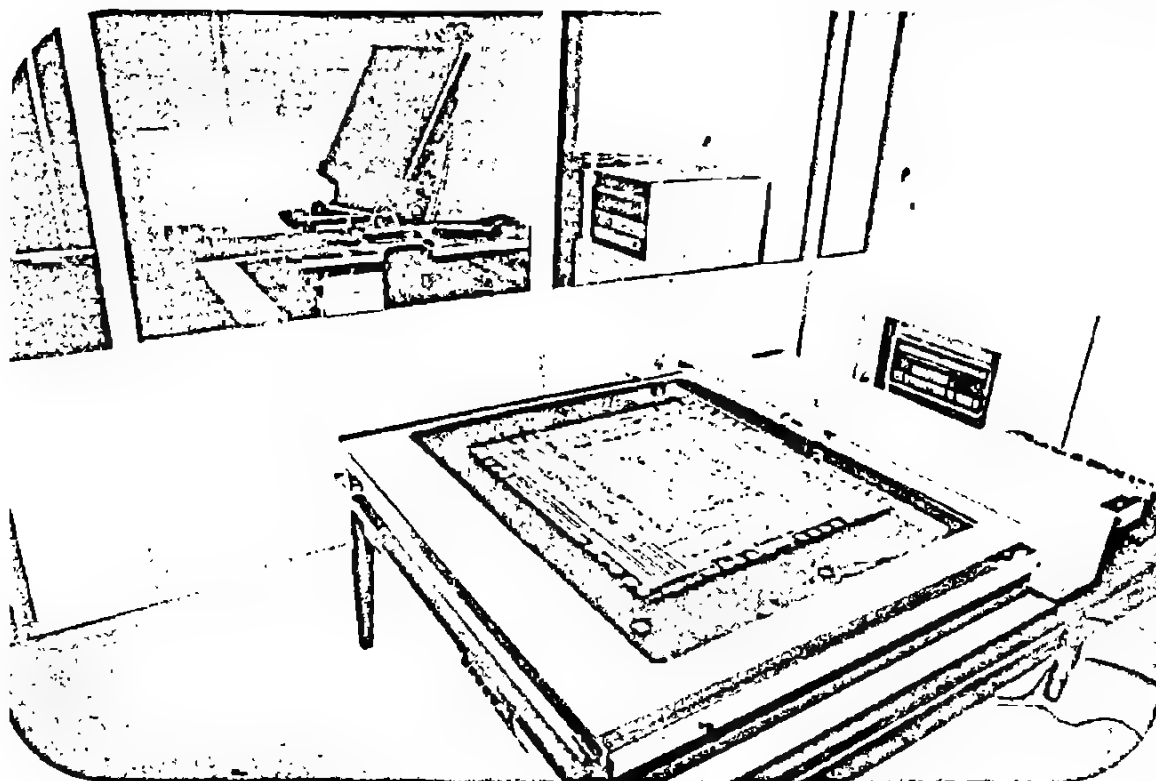
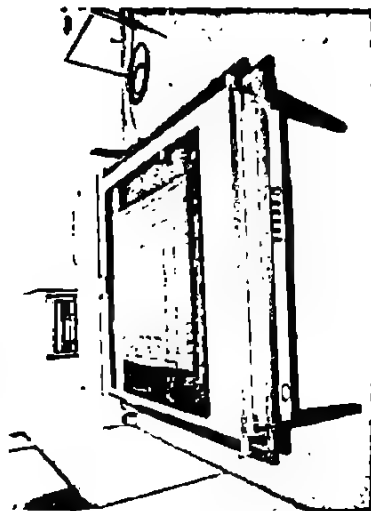


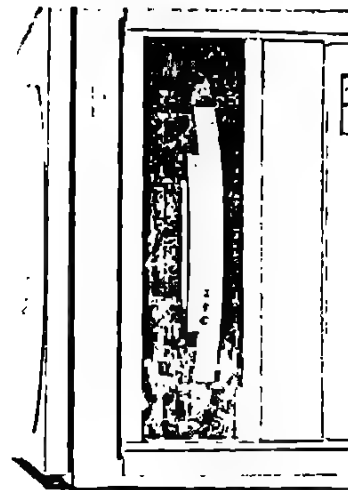
Fig. 2 GRAPHIC SYSTEM

Fig. 3 MASK CUTTING TABLE





PLOTTING AND MASK CUTTING STATION



MAGNETIC DISK

Fig. 4 ORGANIZATION OF THE GRAPHIC SYSTEM

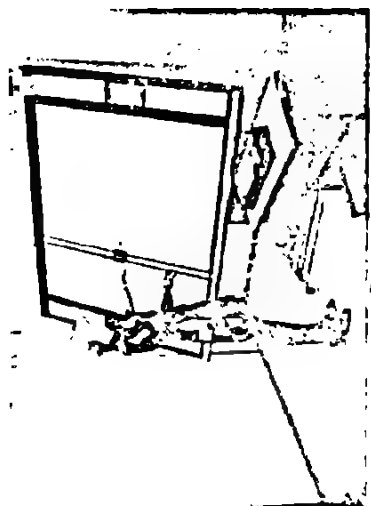
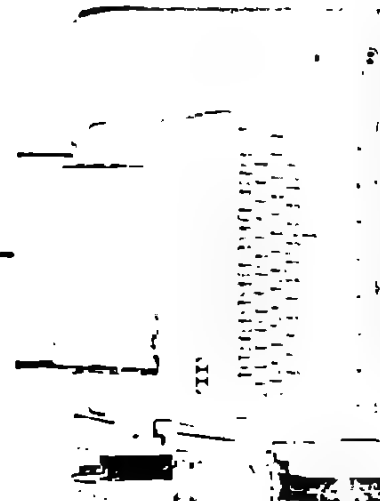


C.R.T. AND DATA TABLET



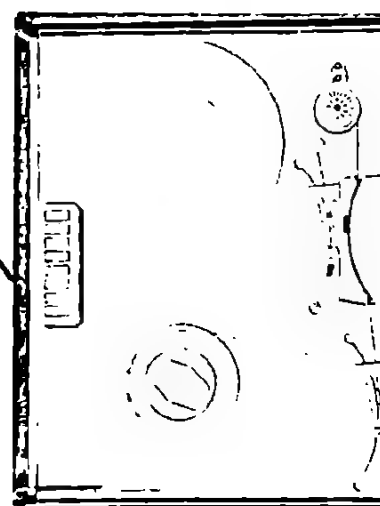
NOVA 1200
MINI-COMPUTER

TELETYPE



DIGITIZING TABLE

MAGNETIC TAPE



Testing:

The calculation of a functional test sequence is generally done in parallel with the mask fabrication by the designer of the circuit. The test sequence is the one which will be used for probe and final test in the production plant to check the logic function performed by the circuit.

The designer is assisted in this task by a computer program: he supplies a description of the logic diagram of the circuit and proposes a test sequence. In return the program tells him which of the possible faults are being detected by this test sequence and which are not. The faults considered by the program are as follows:

Logic nodes of the circuit "stuck at 0", or "stuck at 1". By successive approximations the designer is going to extend this test sequence up to the moment where he is satisfied with it.

Prototypes are then assembled, tested and sent to the customer for system integration. For complex systems a redesign might have to be done. After customer approval, the part is released to production.

Summary:

The above presentation is a simplified description of the processes involved in designing integrated circuits up to the LSI level.

MOTOROLA has now a complete design facility in operation in the Headquarter in Geneva. This facility, in conjunction with the European factory, will greatly improve communications and interaction between MOTOROLA and European Customers.

Fig. 5 Motorola's European Production Facility



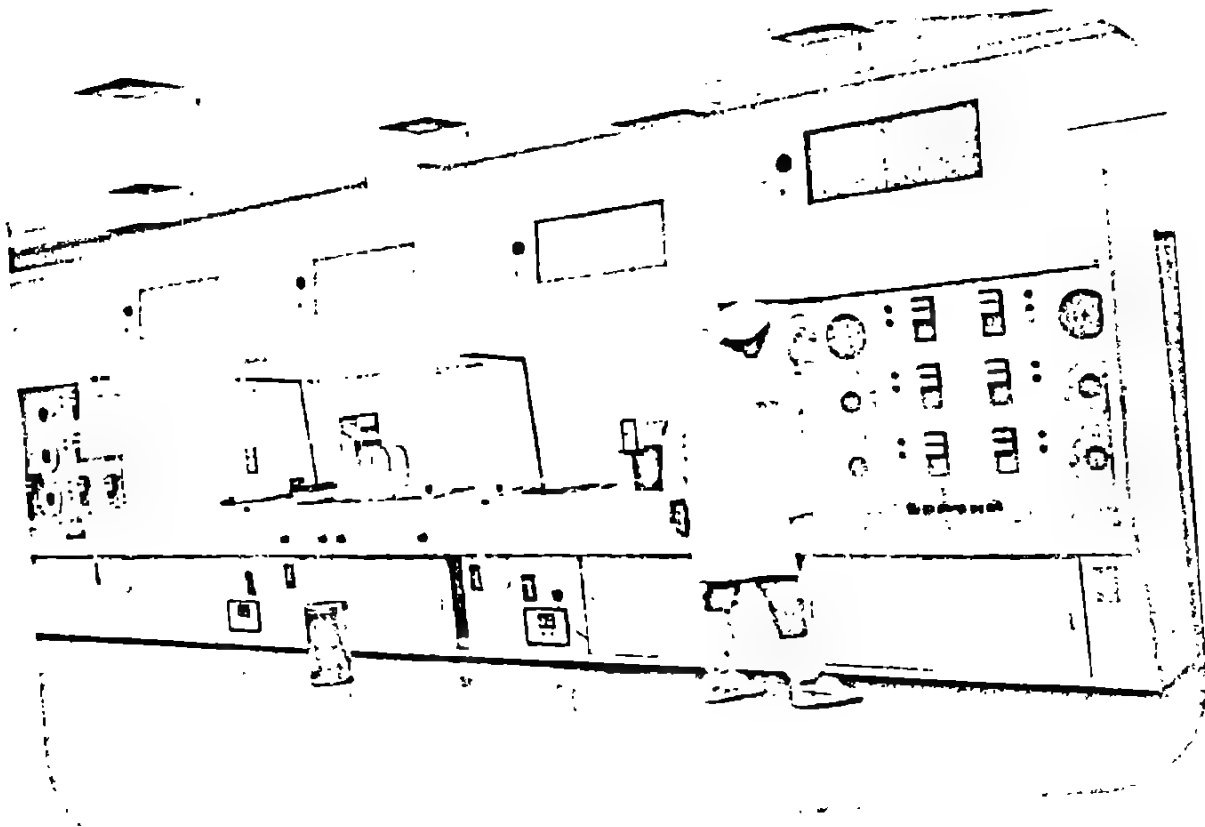


Fig. 6 Wafer Processing AREA

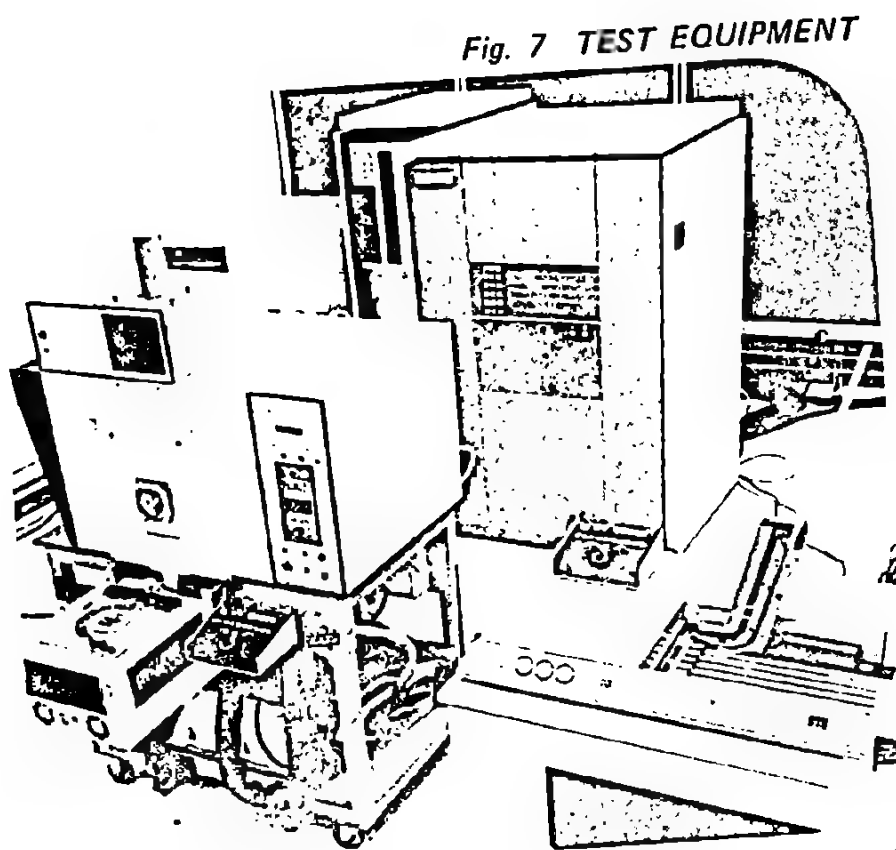


Fig. 7 TEST EQUIPMENT

CHAPTER 14



MOTOROLA
CMOS Products

MOTOROLA CMOS PRODUCTS



- A THE 1973 CMOS FAMILY**
- B FAMILY DATA SHEET**
- C THE CMOS PRODUCT RANGE**
- D LOGIC DIAGRAMS**

A THE 1973 CMOS FAMILY MC14000, MC14500, MC14400 SERIES

FUNCTION	AL/CL/CP
GATES	Dual 3-Input NOR plus Inverter MC14000
	Quad 2-Input NOR 14001
	Dual 4-Input NOR 14002
	Dual Pair and Inverter 14007
	Quad 2-Input NAND 14011
	Dual 4-Input NAND 14012
	Triple 3-Input NAND 14023
	Triple 3-Input NOR 14025
	Triple Gate 14501
	Expandable AND-OR-INVERT 14506
	Quad Exclusive OR 14507
	AND/OR/Exclusive NOR 14519
	Dual 5-Input Majority Logic Gate 14530
BUFFERS	Hex Inverter/Buffer MC14009
	Hex Buffer 14010
	Hex Inverter/Buffer 14049
	Hex Buffer 14050
	Strobed Hex Inverter/Buffer 14502
FLIP-FLOPS	Dual Type D Flip-Flop MC14013
	Dual JK Flip-Flop 14027
SHIFT REGISTERS	18-Bit Shift Register MC14006
	Dual 4-Bit Static Shift Register 14015
	8-Bit Static Shift Register 14021
	8-Bit Universal Bus Register 14034
	4-Stage Parallel In, Parallel Out Shift Register 14035
	Dual 64-Bit Static Shift Register 14517
	Variable Length 64-Bit Shift Register 14557
	128-Bit Static Shift Register 14562
	4x4 Multiport Register 14580
MULTIPLEXERS	Quad Analog Switch/Quad Multiplexer MC14016
	Dual 4-Channel Analog Data Selector 14529
	Dual 4-Channel Digital Multiplexer 14539

DECODERS, ENCODERS, LATCHES	BCD/Decimal Binary/Octal Decoder	MC14028
	Quad Latch	14042
	Dual 4-Bit Latch	14508
	4-Bit Latch/4-to-16 Line Decoder-Output (Active High)	14514
	4-Bit Latch, 4-to-16 Line Decoder-Output (Active Low)	14515
	8-Bit Priority Encoder	14532
	Dual Binary to 1 of 4 Decoder/Demultiplexer	14555
	Dual Binary to 1 of 4 Decoder/Demultiplexer (Inverting)	14556
COUNTERS	Decade Counter/Divider	MC14017
	14-Stage Binary Counter	14020
	Octal Counter/Divider	14022
	7-Stage Binary Counter	14024
	12-Bit Binary Counter	14040
	BCD Up/Down Counter	14510
	Binary UP/Down Counter	14516
	Dual BCD Up Counter	14518
	Dual Binary Up Counter	14520
	24-Stage Frequency Divider	14521
	Programmable BCD Divide-by-N 4-Bit Counter	14522
	Programmable Binary Divide-by-N 4-Bit	14526
	5-Stage Decade Counter	14534
	3-Digit Counter	14553
TIMERS	Programmable Counter/Timer	MC14536
	Industrial Time Base Generator	14566
DATA ROUTING FUNCTIONS	8-Channel Data Selector	MC14512
	Quad 2 Channel Data Select	14519
DISPLAY/DECODER/DRIVERS	BCD-to-7 Segment Latch/Decoder/Driver	MC14511
	BCD-to-7 Segment Latch/Decoder/Liquid Crystal Driver	14543
ARITHMETIC FUNCTIONS	4-Bit Full Adder	MC14008
	Triple Full Adder (Positive)	14032
	Triple Full Adder (Negative)	14038
	ALU (74181 Type)	14581
	Look-Ahead Carry Block	14582
MEMORIES	64 x 1 Bit RAM	MCM14505
	256 x 4 Bit ROM	14524
	256 x 1 Bit RAM	14537
	64 x 4 Bit RAM	14552

SPECIAL FUNCTIONS	Phase-Locked Loop (PLL)	MC14046
	BCD Rate Multiplier	14527
	Dual Monostable Multivibrator	14528
	12-Bit Parity Tree	14531
	Successive Approximation	
	Analog/Digital Register	14549
	2 x 2 Flow Through Multiplier	14554
	Cascadable Successive Approximation Analog/Digital Register	14559
	Dual Schmitt Trigger	14583
	4-Bit Magnitude Comparator	14585
SYSTEMS	Touch Tone Encoder	MC14410
	Bit Rate Generator	14411
	3 ¹ / ₂ Digit DVM	14435

Devices with 24 pins or above are presently not available in CP.

FAMILY DATA SHEET

FAMILY DATA

The MC14000/14500 Series devices are designed with particular attention given to achieving unified, family oriented specifications. Therefore, the devices in this series exhibit common performance characteristics appropriate for their respective logic type (gate, flip-flop, counter, etc.) and temperature-voltage series, including guaranteed family interface parameters.

This data sheet presents the common characteristics of the devices, and should be used together with the unique characteristics of each device as presented in the individual device data sheet.

All CMOS devices in this series are available in three types:

- **AL Series**

Supply Voltage Range = 3.0 Vdc to 18 Vdc
Operating Temperature Range = -55°C to +125°C
Hermetic Ceramic Package
Extra 100% Hi Rel Processing

- **CL Series**

Supply Voltage Range = 3.0 Vdc to 16 Vdc
Operating Temperature Range = -40°C to +85°C
Hermetic Ceramic Package

- **CP Series**

Supply Voltage Range = 3.0 Vdc to 16 Vdc
Operating Temperature Range = -40°C to +85°C
Plastic Package

All three types (AL, CL, CP) offer the following features:

- Quiescent Power Dissipation = 10 nW/package typical for Gates
- Noise Immunity = 45% of V_{DD} typical
30% of V_{DD} guaranteed minimum
- Diode Protection on All Inputs
- Single Supply Operation - Positive or Negative
- High Fanout - > 50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance - 5.0 pF typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance - 750 ohms typical

CMOS

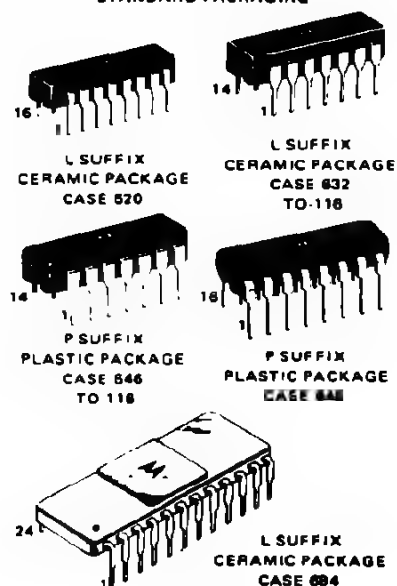
(LOW POWER COMPLEMENTARY MOS)

MC14000AL/CL/CP
series

MC14500AL/CL/CP
series

FAMILY DATA

STANDARD PACKAGING



OTHER PACKAGING

All devices may be obtained in chip form for the manufacturer of hybrid microcircuits. These chips are subjected to the same rigid in process controls as the packaged devices. A data sheet describing CMOS chips is available upon request.

All device types may also be obtained in a flat package upon special request. Contact your Motorola representative for price and delivery information.

AREAS OF APPLICATION

Communication, Navigation, & Identification

Aircraft Avionics
Military Communications
Satellite Surveillance
Space Communications
Ground Support Equipment

Industrial

Industrial Switching Equipment
Marking Machines/Metering Equipment
Weight Measuring Equipment (Scales, etc.)
Computer Manufacturing
Calculator Manufacturing
Pocket Pagers
Medical Equipment

Communication Systems (Portable)

Instrumentation Equipment (Portable)
Camera Controls
Machine Controls
Timing Products

Consumer

Home Surveillance/Protection Equipment
Consumer Home Appliances
Personal/Animal Detection & Pest Control

Automotive

Anti-Skid Controls
Automotive Safety Controls

MAXIMUM RATINGS (Voltage referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage AL Series CL/CP Series	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Series CL/CP Series	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RELIABILITY

All MC14000/14500 Series devices receive Reliability and Quality Assurance in-line monitor verification of all dc, functional, and switching parameters.

Additionally, all AL type parts receive the following 100% hi-rel processing steps:

- Internal Visual Inspection
MIL-STD-883 Method 2010.18 (Modified)
- Temperature Cycling
MIL-STD-883 Method 1010C - 10 cycles, 65°C to 150°C
- Fine Leak Test (Sample)
MIL-STD-883 Method 1014A - 10^{-8} atm cc/s
- Gross Leak Test - Dye Penetrant
- Marking per Specification
- External Visual Examination
MIL-STD-883 Method 2009

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	AL Series			CL/CP Series			Unit
			Min	Typ	Max	Min	Typ	Max	
Operating Power Supply Voltage	V_{DD}	-	3.0	-	18	3.0	-	16	Vdc
Output Voltage ($V_{in} = V_{DD}$ or V_{SS})	V_{out}	-	-	-	$V_{SS} + 0.01$	-	-	$V_{SS} + 0.01$	Vdc
			$V_{DD} - 0.01$	-	-	$V_{DD} - 0.01$	-	-	
Noise Immunity*	"0" Level	V_{NL}	-	30% V_{DD}	45% V_{DD}	-	30% V_{DD}	45% V_{DD}	Vdc
	"1" Level	V_{NH}	-	30% V_{DD}	45% V_{DD}	-	30% V_{DD}	45% V_{DD}	Vdc
Output Drive Current P Channel (I_{source}) ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) N Channel (I_{sink}) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	I_{OH}	5.0	-0.5	-1.5	-	-0.2	-1.5	-	mAdc
		10	-0.5	-1.0	-	-0.2	-1.0	-	
		15	-	-3.6	-	-	-3.6	-	
	I_{OL}	5.0	0.4	0.8	-	0.2	0.8	-	mAdc
		10	0.9	1.2	-	0.5	1.2	-	
		15	-	7.8	-	-	7.8	-	
Input Current ($V_{SS} \leq V_{in} \leq V_{DD}$)	I_{in}	-	-	10	-	-	10	-	pA dc
Input Capacitance ($V_{in} = 0$)	C_{in}	-	-	5.0	-	-	5.0	-	pF
Quiescent Dissipation Gates Dual Flip-Flops	P_D	5.0	-	0.005	0.25	-	0.025	2.5	μW
		10	-	0.01	1.0	-	0.05	10	
		15	-	0.03	-	-	0.15	-	
		5.0	-	0.025	5.0	-	0.05	50	
		10	-	0.05	20	-	0.2	200	
		15	-	0.125	-	-	1.0	-	
Output Rise and Fall Times (10-90%) ($C_L = 15$ pF)	t_r, t_f	5.0	-	100	175	-	100	200	ns
		10	-	35	75	-	35	110	
		15	-	15	-	-	15	-	
Gate Turn-On Delay, Turn-Off Delay (50% of input waveform to 50% of output waveform) ($C_L = 15$ pF)	t_{PHL}, t_{PLH}	5.0	-	60	75	-	60	100	ns
		10	-	25	50	-	25	160	
		15	-	12	-	-	12	-	
Clock Repetition Rate ($C_L = 15$ pF)	PRF	5.0	3.0	4.0	-	2.5	4.0	-	MHz
		10	7.0	10	-	5.0	10	-	
		15	-	15	-	-	15	-	
		5.0	1.5	3.0	-	1.0	3.0	-	
		10	3.0	5.0	-	2.0	5.0	-	
		15	-	8.0	-	-	8.0	-	

*DC Noise Margin (V_{NH} , V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level, that the circuit will withstand before producing an output state change.



MOTOROLA Semiconductor Products Inc.

TYPICAL FAMILY GATE CHARACTERISTICS

OUTPUT SOURCE CURRENT

FIGURE 1 - $V_{GS} = -5.0 \text{ Vdc}$, $V_{DD} = 5.0 \text{ Vdc}$

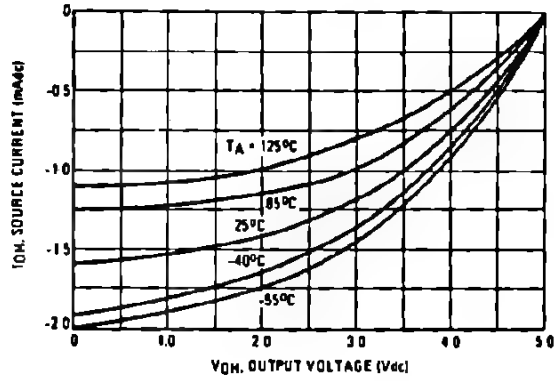


FIGURE 2 - $V_{GS} = -10 \text{ Vdc}$, $V_{DD} = 10 \text{ Vdc}$

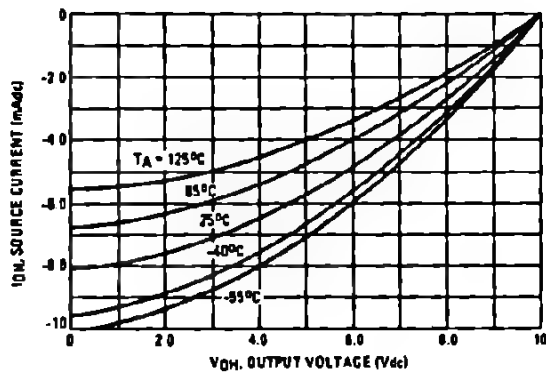
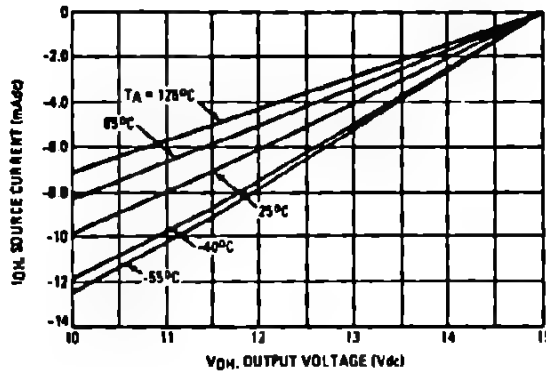


FIGURE 3 - $V_{GS} = -15 \text{ Vdc}$, $V_{DD} = 15 \text{ Vdc}$



OUTPUT SINK CURRENT

FIGURE 4 - $V_{GS} = 5.0 \text{ Vdc}$, $V_{DD} = 5.0 \text{ Vdc}$

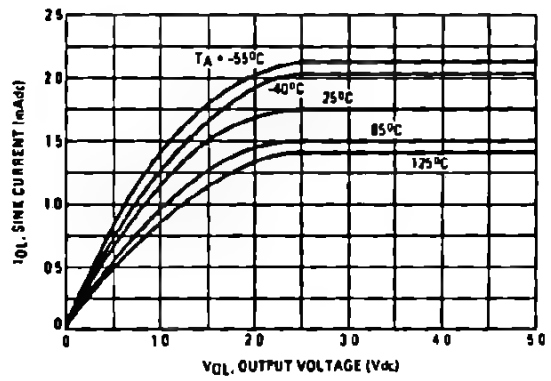


FIGURE 5 - $V_{GS} = 10 \text{ Vdc}$, $V_{DD} = 10 \text{ Vdc}$

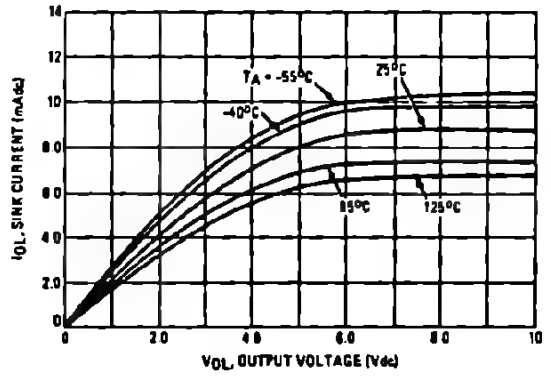
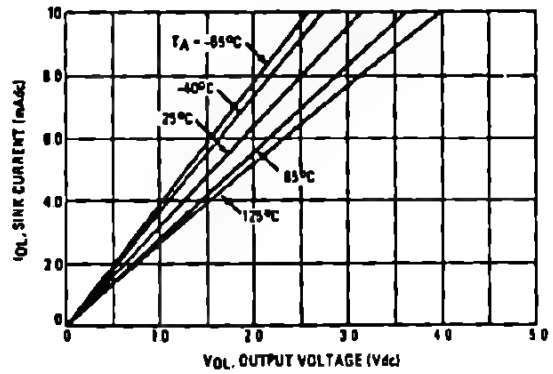


FIGURE 6 - $V_{GS} = 15 \text{ Vdc}$, $V_{DD} = 15 \text{ Vdc}$



TYPICAL FAMILY GATE CHARACTERISTICS (continued)

FIGURE 7 - VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

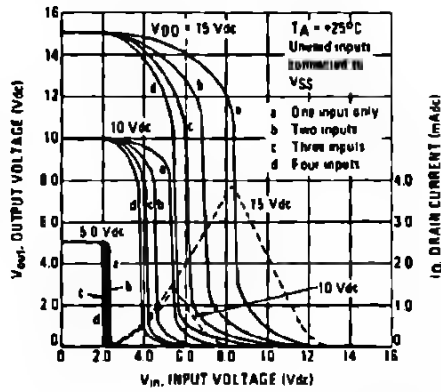


FIGURE 8 - VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

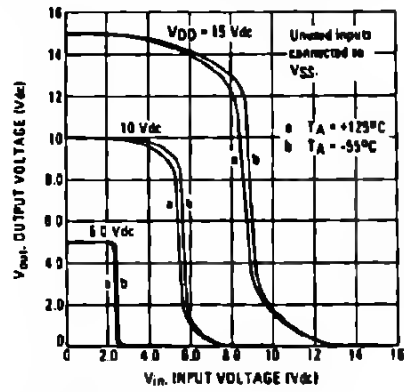


FIGURE 9 - GATE POWER DISSIPATION CHARACTERISTICS

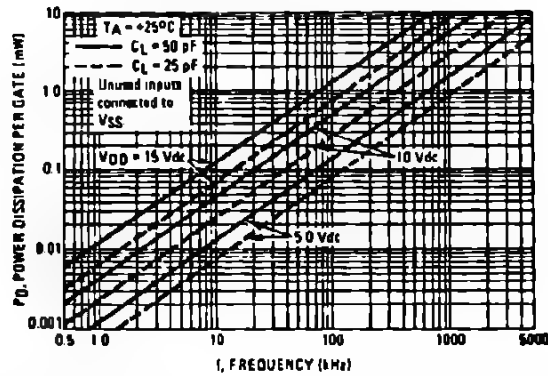


FIGURE 10 - RISE AND FALL TIME versus LOAD CAPACITANCE

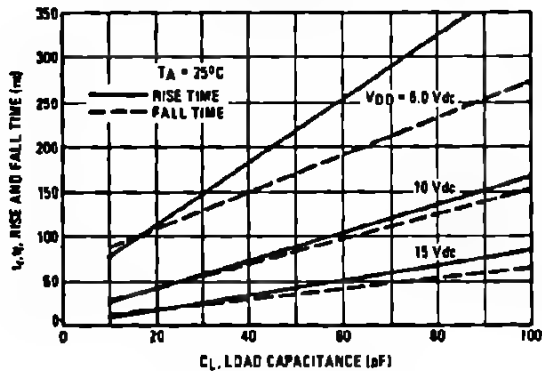
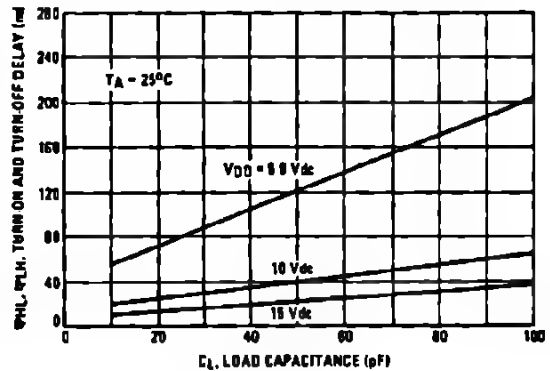


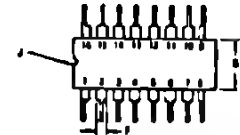
FIGURE 11 - TURN-ON AND TURN-OFF DELAY CHARACTERISTICS



MOTOROLA Semiconductor Products Inc.

PACKAGE DIMENSIONS

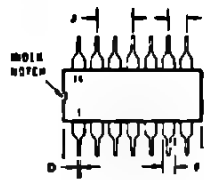
L SUFFIX
CERAMIC PACKAGE
CASE 620



NOTE:
1 DIM "B" IS MEASURED AT CENTER OF LEADS WHEN FORMED PARALLEL
2 / UNDER NOTCH IN LEAD KEY DOT OR DOT IN C (RANGE)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.760	18.750	19.310
B	0.740	0.775	18.750	19.600
C	0.170	0.200	4.300	5.080
D	0.375	0.378	9.500	9.590
E	0.133	0.15	3.380	3.750
F	0.095	0.095	2.400	2.400
G	0.100 TP		2.54 TP	
H	0.115	0.125	2.900	3.175
I	0.115	0.125	2.900	3.175
J	0.115	0.125	2.900	3.175
K	0.115	0.125	2.900	3.175
L	0.115	0.125	2.900	3.175
M	0.115	0.125	2.900	3.175
N	0.115	0.125	2.900	3.175
O	0.115	0.125	2.900	3.175
P	0.115	0.125	2.900	3.175
Q	0.115	0.125	2.900	3.175
R	0.115	0.125	2.900	3.175
S	0.115	0.125	2.900	3.175
T	0.115	0.125	2.900	3.175
U	0.115	0.125	2.900	3.175
V	0.115	0.125	2.900	3.175
W	0.115	0.125	2.900	3.175
X	0.115	0.125	2.900	3.175
Y	0.115	0.125	2.900	3.175
Z	0.115	0.125	2.900	3.175

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

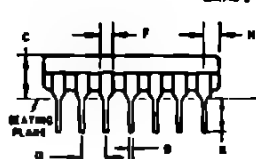
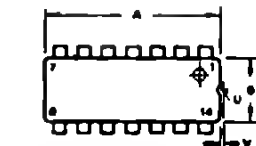


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.660	0.760	16.760	19.300
B	0.660	0.760	16.760	19.300
C	0.170	0.200	4.300	5.080
D	0.375	0.378	9.500	9.590
E	0.375	0.378	9.500	9.590
F	0.375	0.378	9.500	9.590
G	0.375	0.378	9.500	9.590
H	0.375	0.378	9.500	9.590
I	0.375	0.378	9.500	9.590
J	0.375	0.378	9.500	9.590
K	0.375	0.378	9.500	9.590
L	0.375	0.378	9.500	9.590
M	0.375	0.378	9.500	9.590
N	0.375	0.378	9.500	9.590
O	0.375	0.378	9.500	9.590
P	0.375	0.378	9.500	9.590
Q	0.375	0.378	9.500	9.590
R	0.375	0.378	9.500	9.590
S	0.375	0.378	9.500	9.590
T	0.375	0.378	9.500	9.590
U	0.375	0.378	9.500	9.590
V	0.375	0.378	9.500	9.590
W	0.375	0.378	9.500	9.590
X	0.375	0.378	9.500	9.590
Y	0.375	0.378	9.500	9.590
Z	0.375	0.378	9.500	9.590

NOTE:
1 "B" - Inserted Position of Lead Centers.
2 "E" - 0 except 1 notched notch.

SEE REF TO 116 dimensions and notes apply

P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116



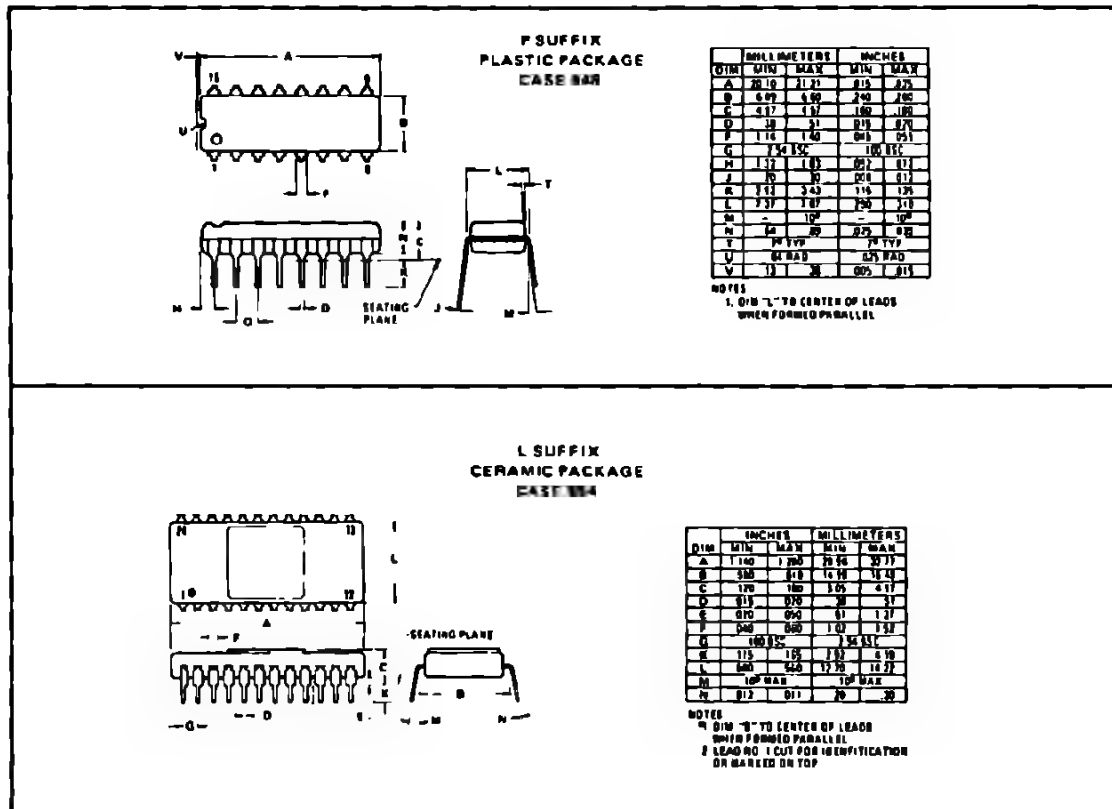
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.00	18.75	0.700	0.740
B	18.00	18.75	0.700	0.740
C	4.00	4.17	0.150	0.160
D	9.50	9.59	0.375	0.378
E	9.50	9.59	0.375	0.378
F	9.50	9.59	0.375	0.378
G	9.50	9.59	0.375	0.378
H	9.50	9.59	0.375	0.378
I	9.50	9.59	0.375	0.378
J	9.50	9.59	0.375	0.378
K	9.50	9.59	0.375	0.378
L	9.50	9.59	0.375	0.378
M	9.50	9.59	0.375	0.378
N	9.50	9.59	0.375	0.378
O	9.50	9.59	0.375	0.378
P	9.50	9.59	0.375	0.378
Q	9.50	9.59	0.375	0.378
R	9.50	9.59	0.375	0.378
S	9.50	9.59	0.375	0.378
T	9.50	9.59	0.375	0.378
U	9.50	9.59	0.375	0.378
V	9.50	9.59	0.375	0.378
W	9.50	9.59	0.375	0.378
X	9.50	9.59	0.375	0.378
Y	9.50	9.59	0.375	0.378
Z	9.50	9.59	0.375	0.378

Dimension 1, 10 lead exception when
lowest parallel



MOTOROLA Semiconductor Products Inc.

PACKAGE DIMENSIONS (continued)



INPUT PROTECTION

Motorola CMOS circuits have built-in protection circuitry on all inputs to prevent device damage to the sensitive input gates that could result from improper testing or handling procedures prior to final assembly. This protection scheme is necessary because the extremely high impedance on the MOS gate oxide (approximately 10^{12} ohms) allows even a low energy source to generate a high enough potential (usually 100 volts) to rupture this gate oxide and thus destroy the device. While protection circuitry is effective in reducing over-voltages, it is expected that the user will take normal precautions to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

UNUSED INPUTS

Unused inputs must be connected to the supply voltage (V_{DD} or V_{SS}) that is appropriate for the system logic design.

C THE CMOS PRODUCT RANGE

At present, 80 general purpose digital building blocks have been defined. They have been divided into three categories:

MC 14000 SERIES

These functions represent popular digital logic devices.

MC 14500 SERIES

These functions represent a combination of popularly customer requested, previously unavailable logic types and popular TTL MSI functions. Already other manufacturers are second sourcing several of these devices or have announced intentions to do so.

MC 14400 SERIES

This series represents a growing list of functions which are actual systems or sub-systems, e.g. MC 14435 – 3¹/₂ digit DVM chip.

NUMERICAL INDEX OF DEVICES

DEVICE	FUNCTION
MC14000	Dual 3-Input NOR Gate plus Inverter
MC14001	Quad 2-Input NOR Gate
MC14002	Dual 4-Input NOR Gate
MC14006	18-Bit Shift Register
MC14007	Dual Pair and Inverter
MC14008	4-Bit Full Adder
MC14009	Hex Buffer (Inverting)
MC14010	Hex Buffer (Non-inverting)
MC14011	Quad 2-Input NAND Gate
MC14012	Dual 4-Input NAND Gate
MC14013	Dual Type D Flip-Flop
MC14015	Dual 4-Bit Static Shift Register
MC14016	Quad Analog Switch/Quad Multiplexer
MC14017	Decade Counter/Divider
MC14020	14-Stage Binary Counter
MC14021	8-Bit Static Shift Register
MC14022	Octal Counter/Divider
MC14023	Triple 3-Input NAND Gate
MC14024	7-Stage Binary Counter
MC14025	Triple 3-Input NOR Gate
MC14027	Dual J-K Flip-Flop
MC14028	BCD-to-Decimal Decoder/Binary-to-Octal Decoder
MC14032	Triple Full Adder (Positive)
MC14034	8-Bit Universal Bus Register
MC14035	4-Stage Parallel In, Parallel Out Shift Register
MC14038	Triple Full Adder (Negative)
MC14040	12-Bit Binary Counter
MC14042	Quad Latch
MC14046	Phase-Locked Loop (PLL)
MC14049	Hex Buffer (Inverting)
MC14050	Hex Buffer
MC14410	Touch Tone Encoder
MC14411	Bit Rate Generator
MC14435	3½ Digit-Digital Voltmeter
MC14501	Triple Gate
MC14502	Strobed Hex Inverter/Buffer
MC14506	Expandable AND-OR-INVERT Gate with Inhibit
MC14507	Quad Exclusive OR Gate
MC14508	Dual 4-Bit Latch
MC14510	BCD Up/Down Counter
MC14511	BCD-to-Seven Segment Latch/Decoder/Driver
MC14512	8-Channel Data Selector
MC14514	4-Bit Latch/4-to-16 Line Decoder (Output Active High)
MC14515	4-Bit Latch/4-to-16 Line Decoder (Output Active Low)
MC14516	Binary Up/Down Counter
MC14517	Dual 64-Bit Static Shift Register
MC14518	Dual BCD Up Counter

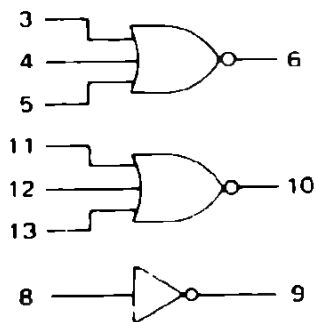
MC14519	4-Bit AND/OR Select
MC14520	Dual Binary Up Counter
MC14521	24-Stage Frequency Divider
MC14522	Programmable BCD Divide-by-N 4-Bit Counter
MC14526	Programmable Binary Divide-by-N 4-Bit Counter
MC14527	BCD Rate Multiplier
MC14528	Dual Monostable Multivibrator
MC14529	Dual 4-Channel Analog Data Selector
MC14530	Dual 5-Input Majority Logic Gate
MC14531	12-Bit Parity Tree
MC14532	8-Bit Priority Encoder
MC14534	5-Stage Decade Counter
MC14536	Programmable Counter/Timer
MC14539	Dual 4-Channel Digital Multiplexer
MC14543	BCD-to-Seven Segment Latch/Decoder/Liquid Crystal Driver
MC14549	Successive Approximation Analog/Digital Register
MC14553	3-Digit Counter
MC14554	2 x 2 Flow Through Multiplier
MC14555	Dual Binary to 1 of 4 Decoder
MC14556	Dual Binary to 1 of 4 Decoder (Inverting)
MC14557	Variable Length 64-Bit Shift Register
MC14559	Cascadable Successive Approximation Analog/Digital Register
MC14562	128-Bit Static Shift Register
MC14566	Industrial Time Base Generator
MC14580	4 x 4 Multiport Register
MC14581	Arithmetic Logic Unit
MC14582	Look-Ahead Carry Block
MC14583	Dual Schmitt Trigger
MC14585	4-Bit Magnitude Comparator
MCM14505	64 x 1 Bit RAM
MCM14524	156 x 4 Bit ROM
MCM14537	256 x 1 Bit RAM
MCM14552	64 x 4 Bit RAM

LOGIC DIAGRAMS

LOGIC DIAGRAMS

GATES

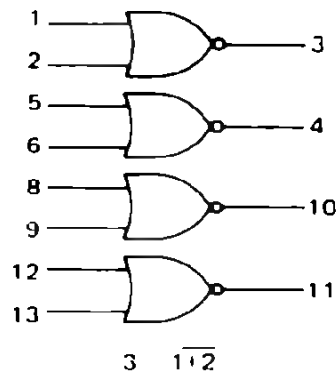
MC14000
Dual 3-Input NOR Gate plus Inverter



V_{DD} = Pin 14
 V_{SS} = Pin 7

6 $\overline{3 + 4 + 5}$
9 $\overline{8}$

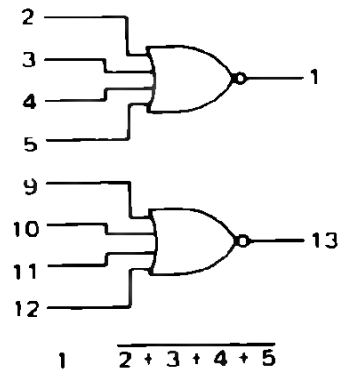
MC14001
Quad 2-Input NOR Gate



V_{DD} = Pin 14
 V_{SS} = Pin 7

3 $\overline{1 + 2}$

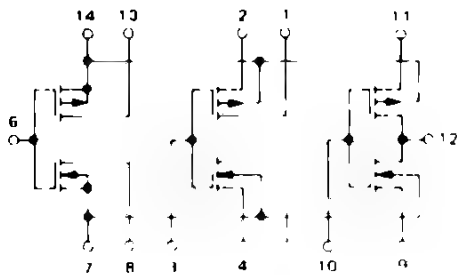
MC14002
Dual 4-Input NOR Gate



V_{DD} = Pin 14
 V_{SS} = Pin 7

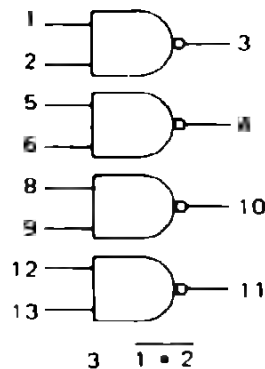
1 $\overline{2 + 3 + 4 + 5}$

MC14007
Dual Pair and Inverter



V_{DD} = Pin 14
 V_{SS} = Pin 7

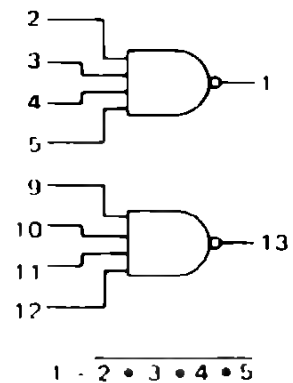
MC14011
Quad 2-Input NAND Gate



V_{DD} = Pin 14
 V_{SS} = Pin 7

3 $\overline{1 \cdot 2}$

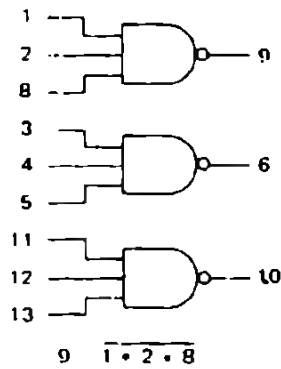
MC14012
Dual 4-Input NAND Gate



V_{DD} = Pin 14
 V_{SS} = Pin 7

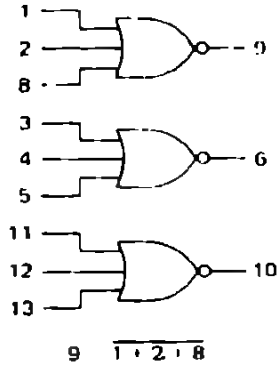
1 $\overline{2 \cdot 3 \cdot 4 \cdot 5}$

MC14023
Triple 3-Input NAND Gate



V_{DD} = Pin 14
 V_{SS} = Pin 7

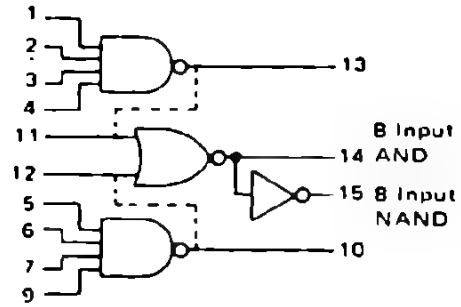
MC14025
Triple 3-Input NOR Gate



V_{DD} = Pin 14
 V_{SS} = Pin 7

MC14501
Triple Gate

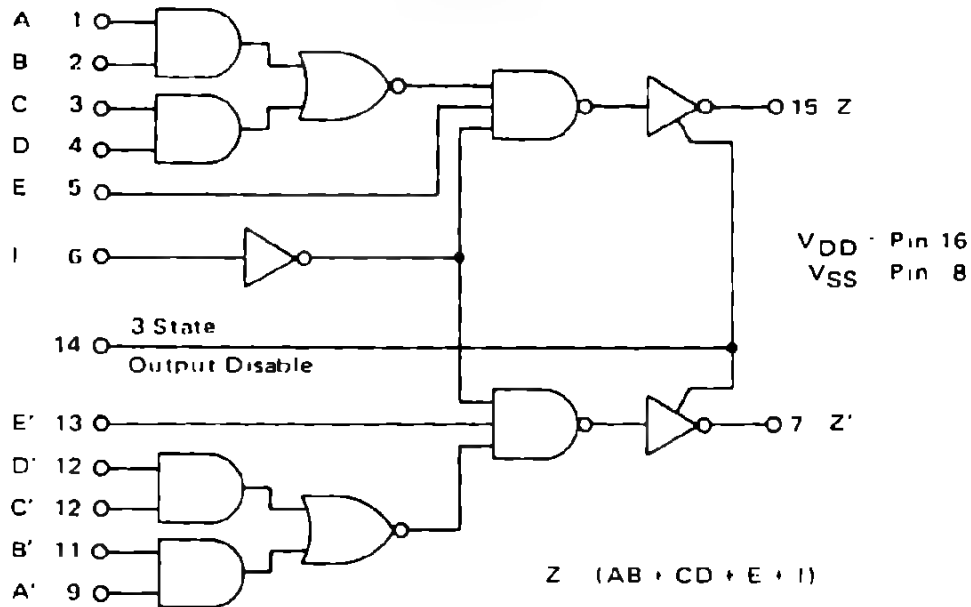
Use Dotted Connection Externally to Obtain 8 Input Functions



Note: Pin 14 must not be used as an input to the Inverter.

V_{DD} = Pin 16
 V_{SS} = Pin 8

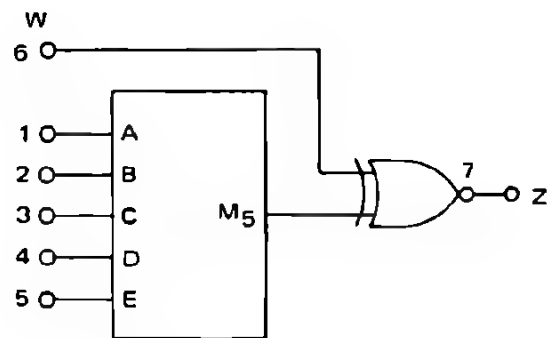
MC14506
Dual Expandable AND-OR-INVERT Gate



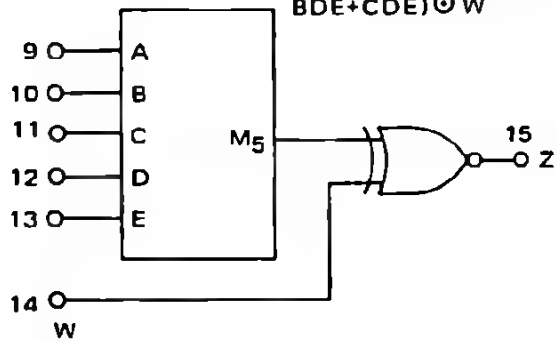
V_{DD} = Pin 16
 V_{SS} = Pin 8

$$Z = (AB + CD + E + I)$$

MC14530
Dual 5-Input Majority
Logic Gate



$$Z = M_5 \odot W = (ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE) \odot W$$

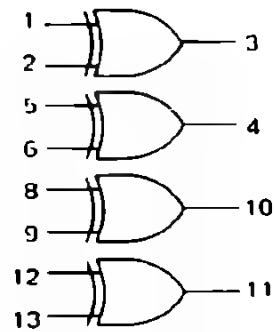


*M₅ is a logical "1" if any three or more inputs are logical "1"

$$\odot \equiv \text{Exclusive NOR} \equiv \overline{\text{Exclusive OR}}$$

V_{DD} = Pin 16
V_{SS} = Pin 8

MC14507
Quad Exclusive OR Gate

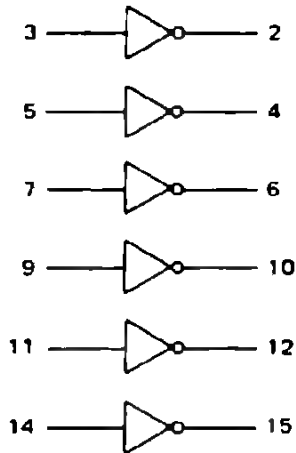


$$3 = 1 \odot 2$$

V_{DD} = Pin 14
V_{SS} = Pin 7

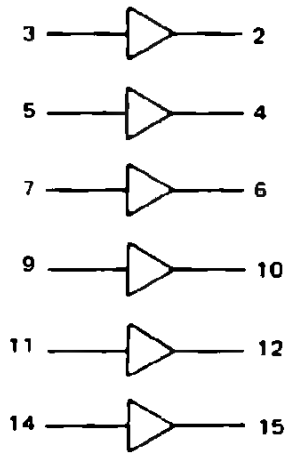
BUFFERS

MC14008
Hex Inverter/Buffer



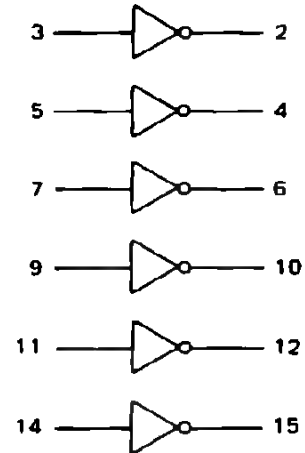
V_{DD} = Pin 16
 V_{SS} = Pin 8
 V_{CC} = Pin 1

MC14010
Hex Buffer



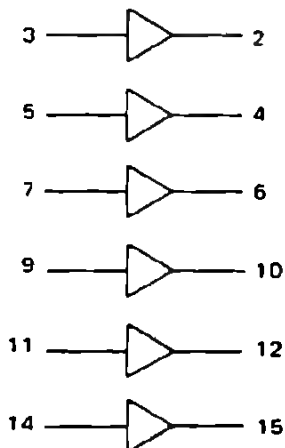
V_{DD} = Pin 16
 V_{SS} = Pin 8
 V_{CC} = Pin 1

MC14049
Hex Inverter/Buffer



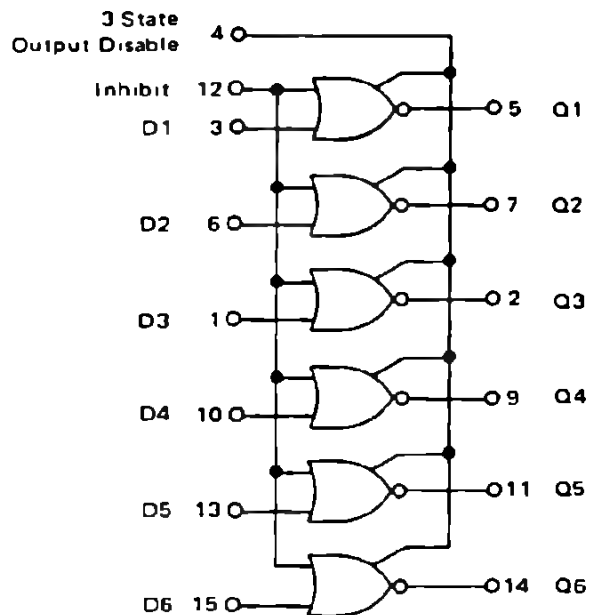
V_{SS} = Pin 8
 V_{CC} = Pin 1

MC14050
Hex Buffer



V_{SS} = Pin 8
 V_{CC} = Pin 1

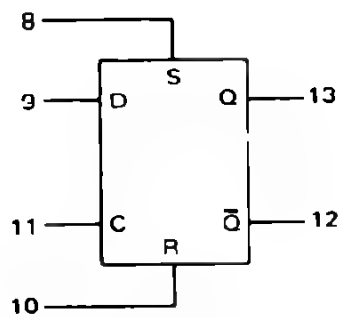
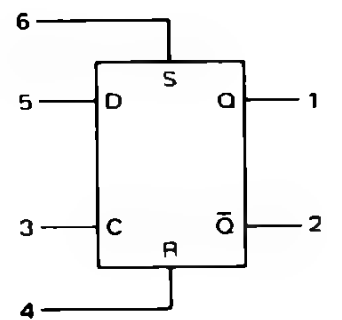
MC14502
Strobed Hex Inverter/Buffer



V_{DD} = Pin 16
 V_{SS} = Pin 8

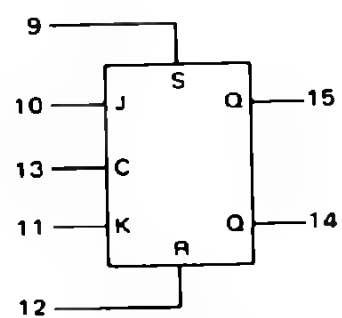
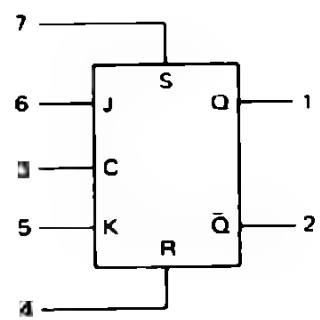
FLIP-FLOPS

MC14013
Dual Type D Flip-Flop



V_{DD} = Pin 14
 V_{SS} = Pin 7

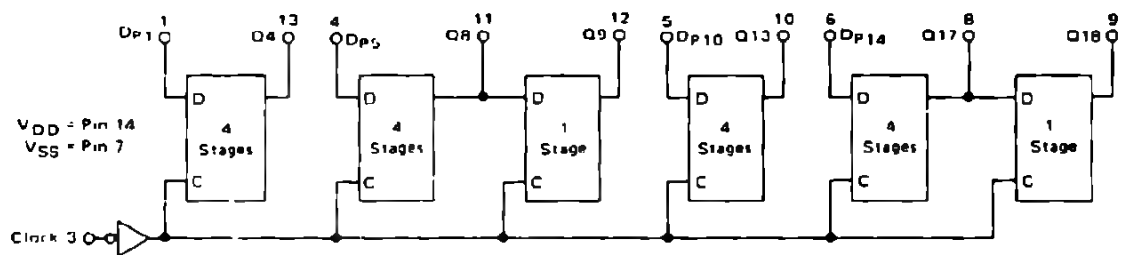
MC14027
Dual J-K Flip-Flop



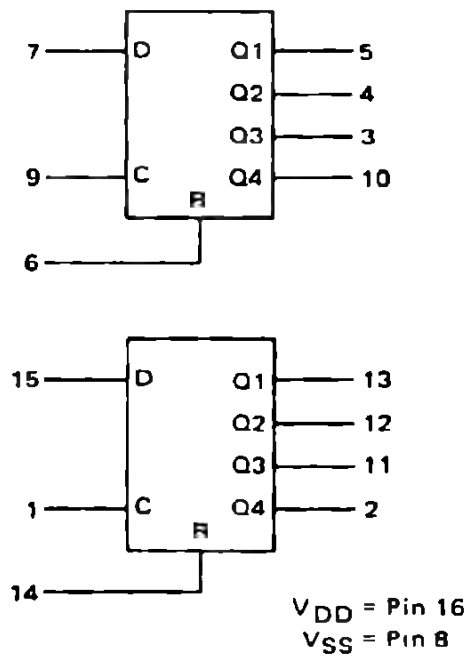
V_{DD} = Pin 16
 V_{SS} = Pin 8

SHIFT REGISTERS

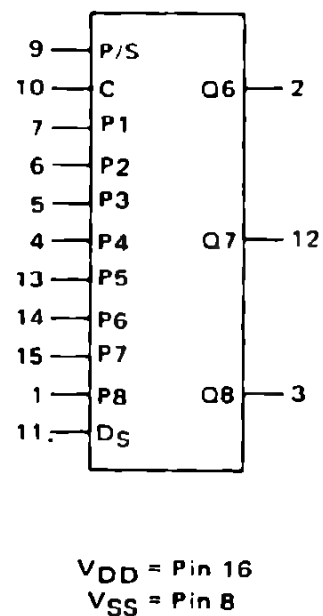
MC14006
18-Bit Static Shift Register



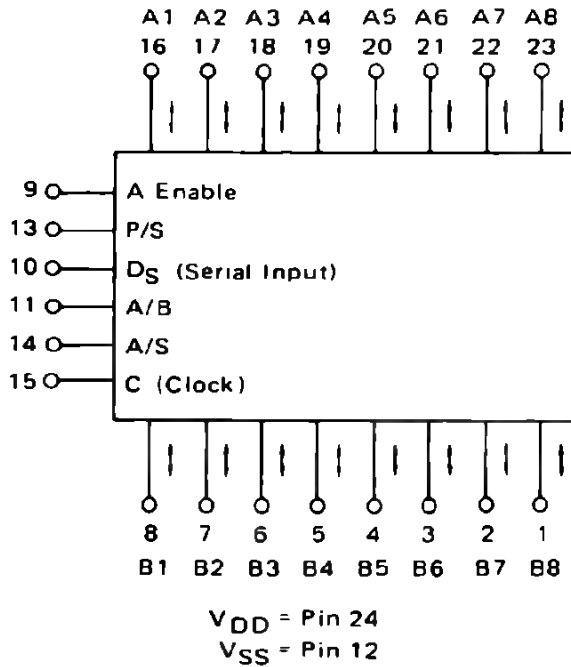
MC14015
Dual 4-Bit Static Shift Register



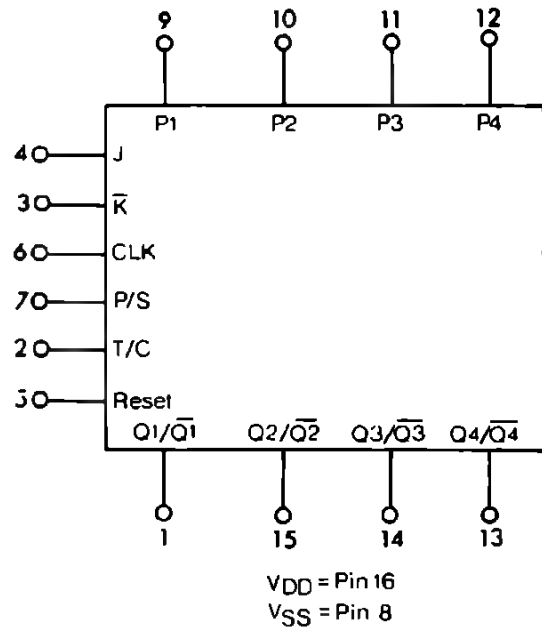
MC14021
8-Bit Static Shift Register



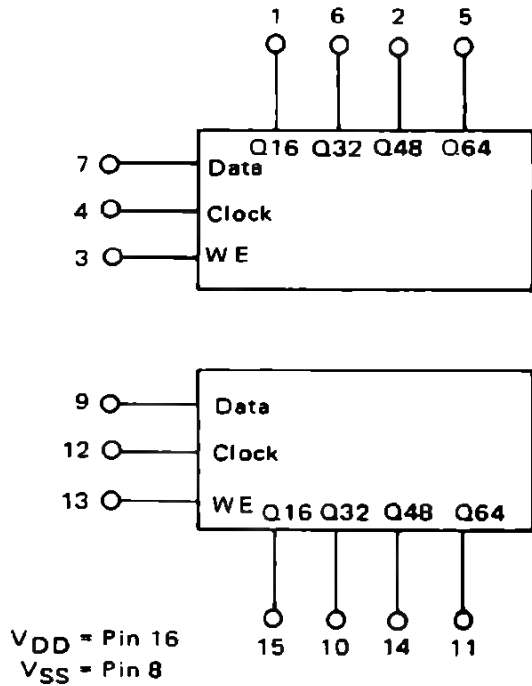
MC14034
8-Bit Universal Bus Register



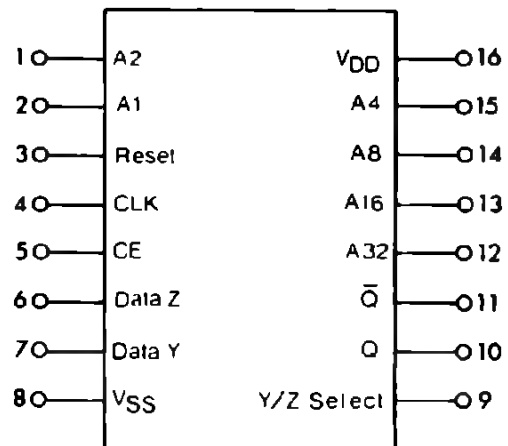
MC14035
4-Stage Parallel In, Parallel Out
Shift Register



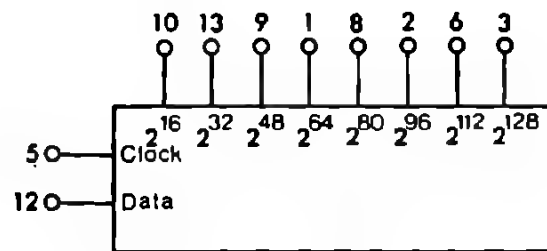
MC14517
Dual 64-Bit Static Shift Register



MC14557
Variable Length 64-Bit Shift Register



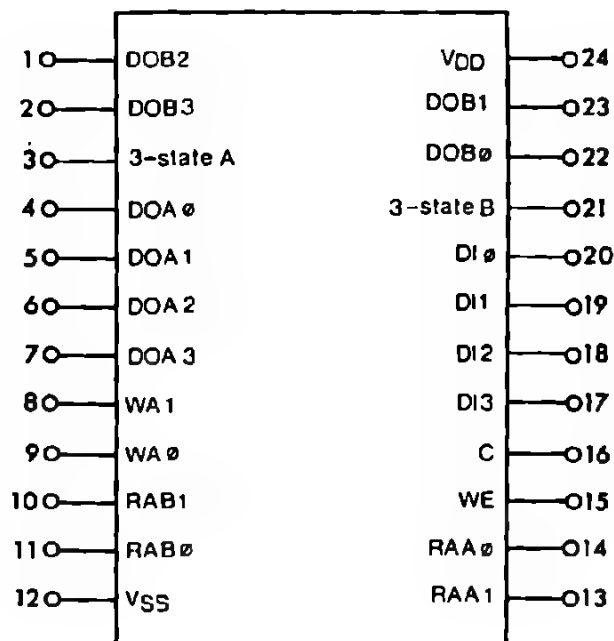
MC14562
128 Bit Static Shift Register



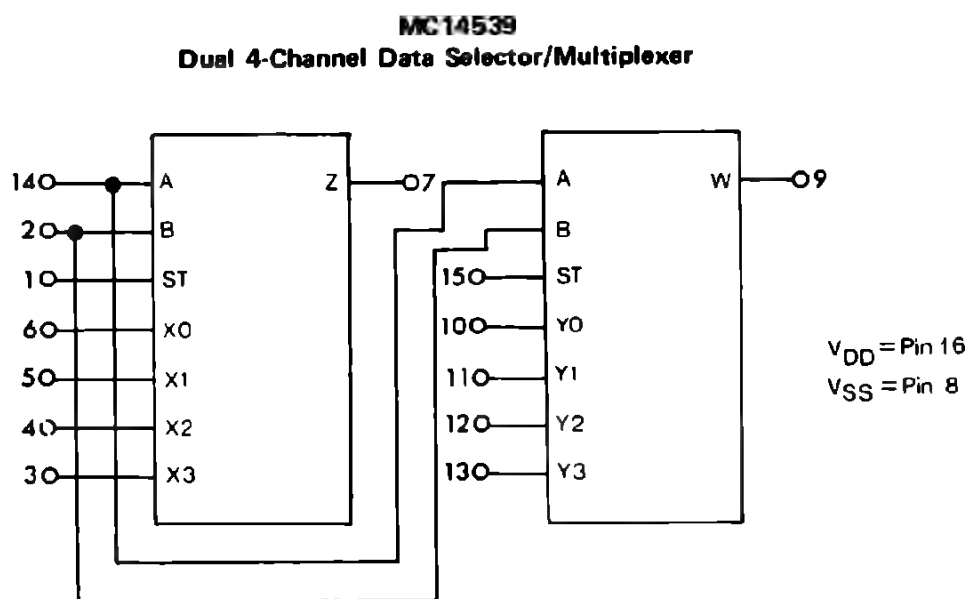
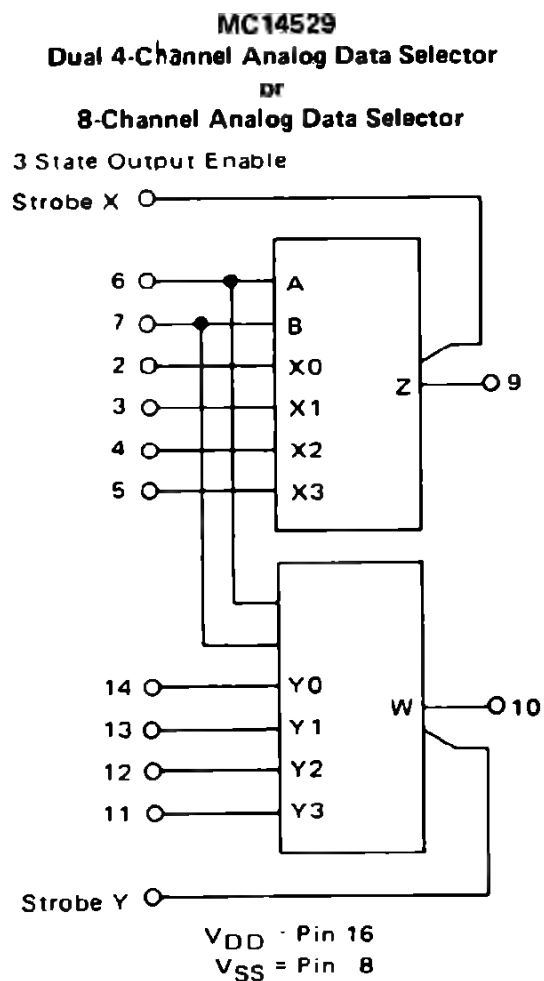
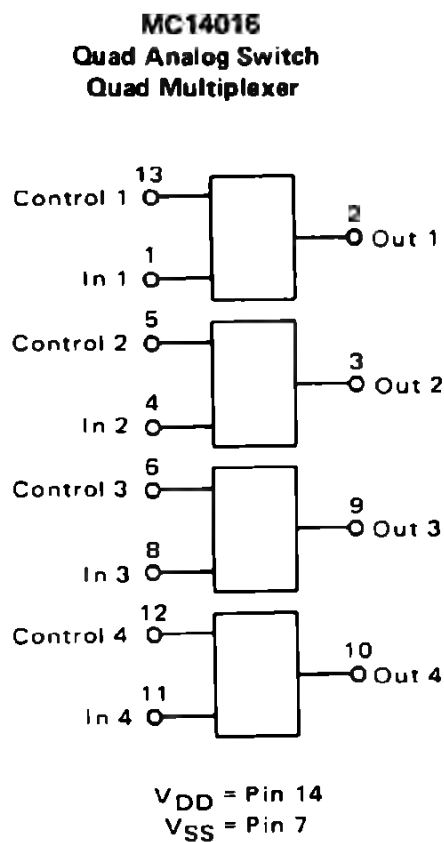
V_{DD} = Pin 14

V_{SS} = Pin 7

MC14580
4 x 4 Multiport Register

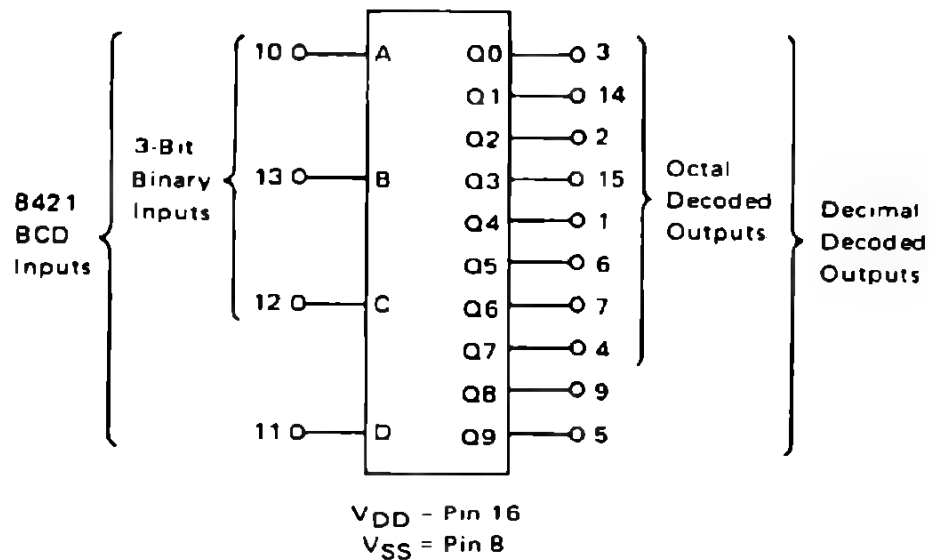


MULTIPLEXERS

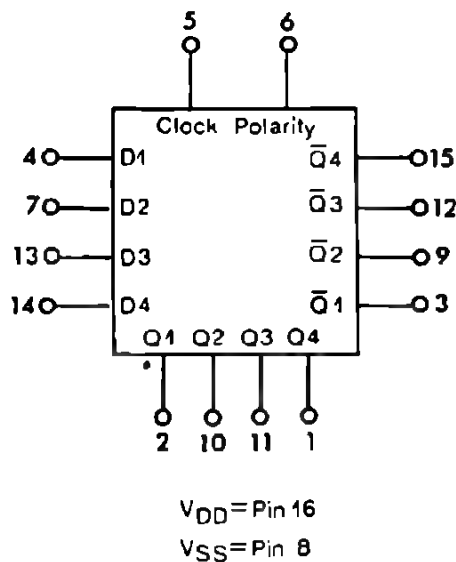


DECODERS/ENCODERS/LATCHES

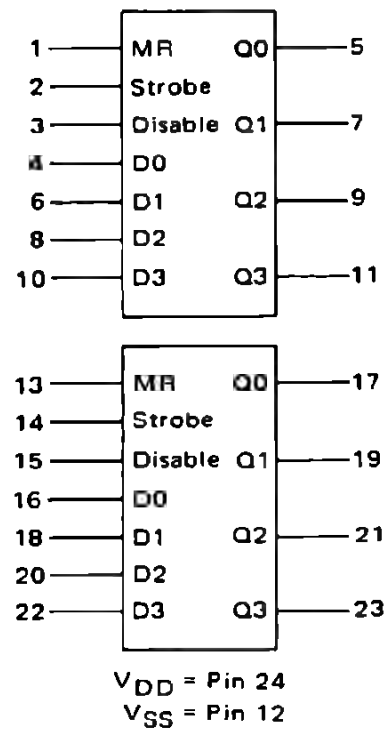
MC14028
BCD-to-Decimal Decoder
Binary-to-Octal Decoder



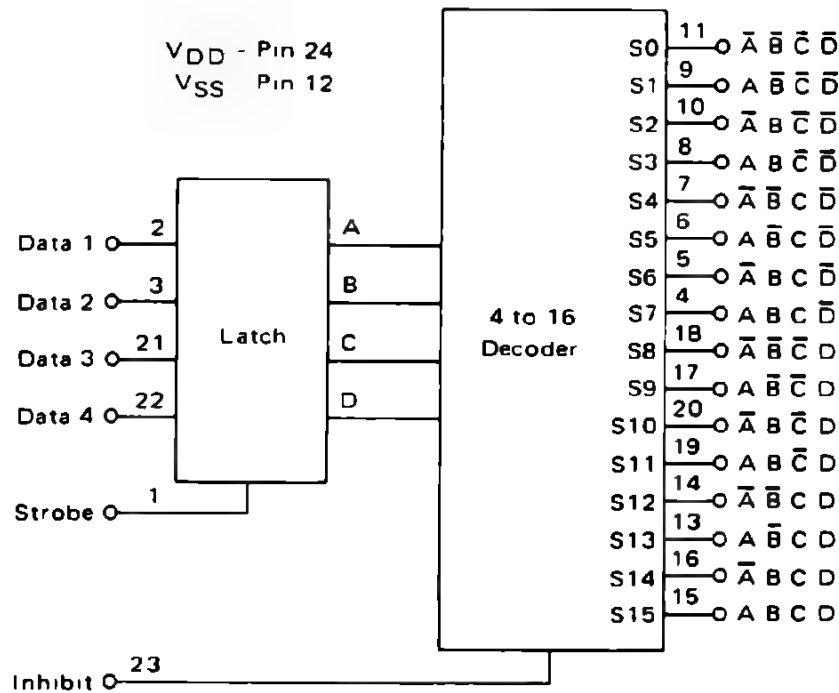
MC14042
Quad Latch



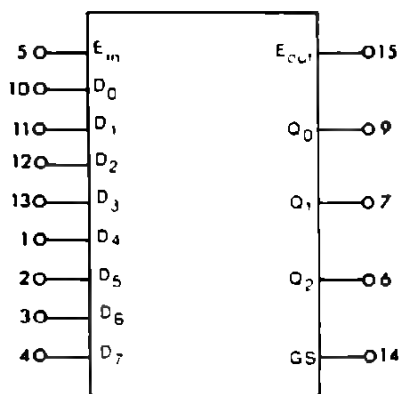
MC14508
Dual 4-Bit Latch



MC14514, MC14515
4-Bit Latch/4-to-16 Line Decoder

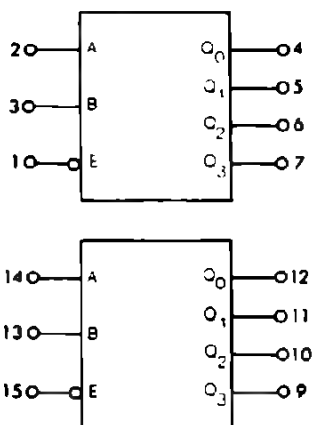


MC14532
8-Bit Priority Encoder



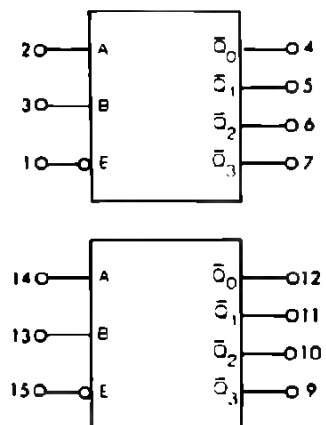
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14555
(Non-Inverting)
Dual Binary to 1 of 4 Decoder/Demultiplexer



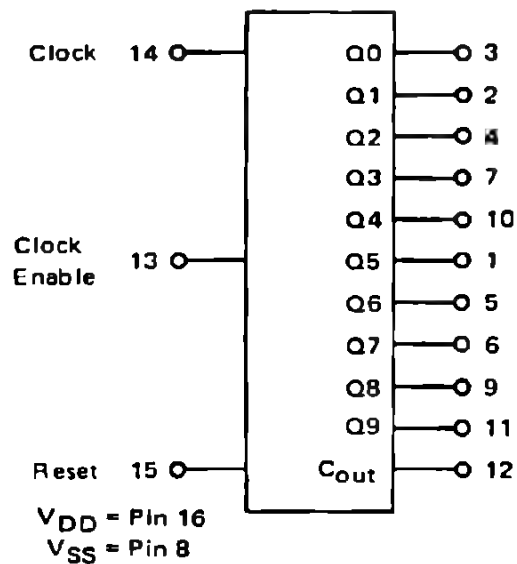
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14556
(Inverting)
Dual Binary to 1 of 4 Decoder/Demultiplexer

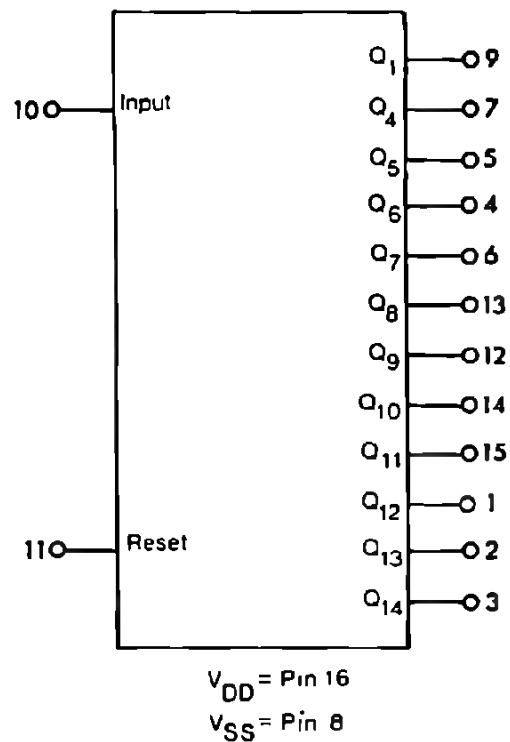


COUNTERS

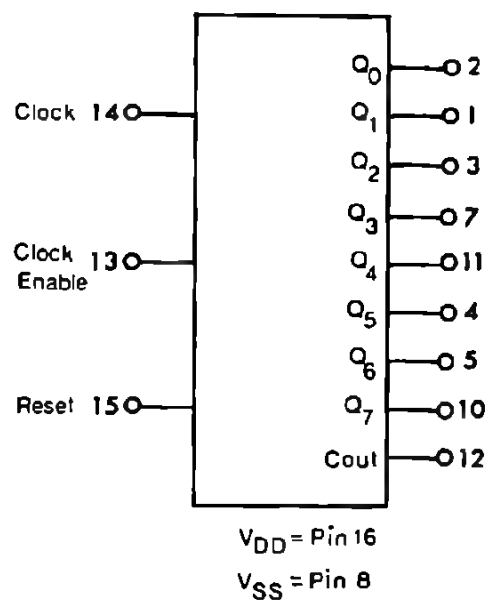
MC14017
Decade Counter/Divider



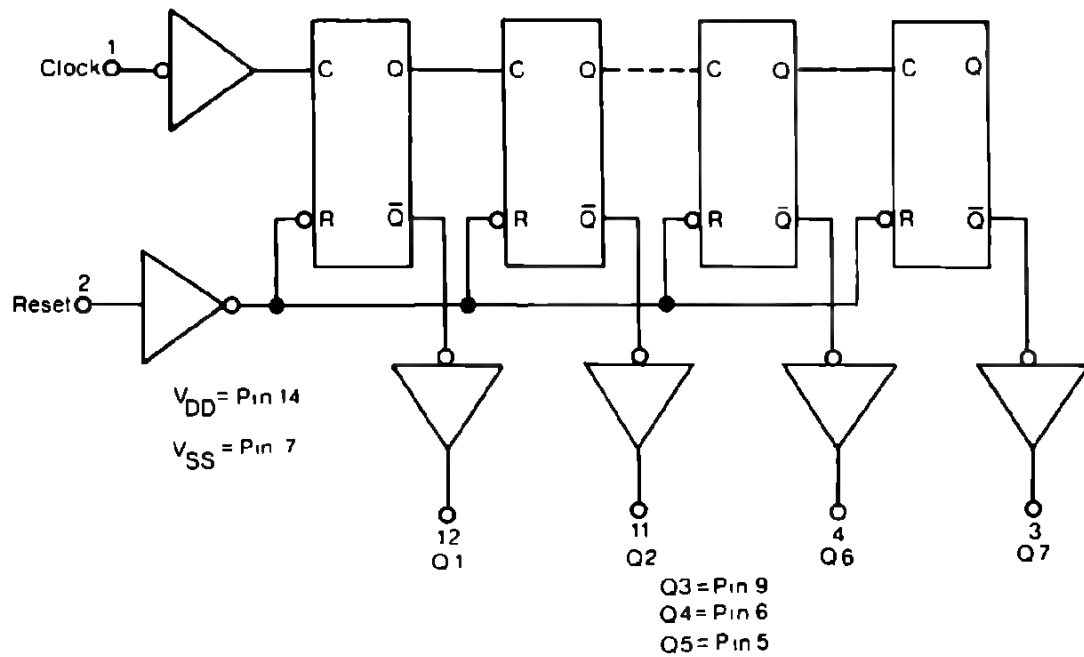
MC14020
14-Stage Binary Counter



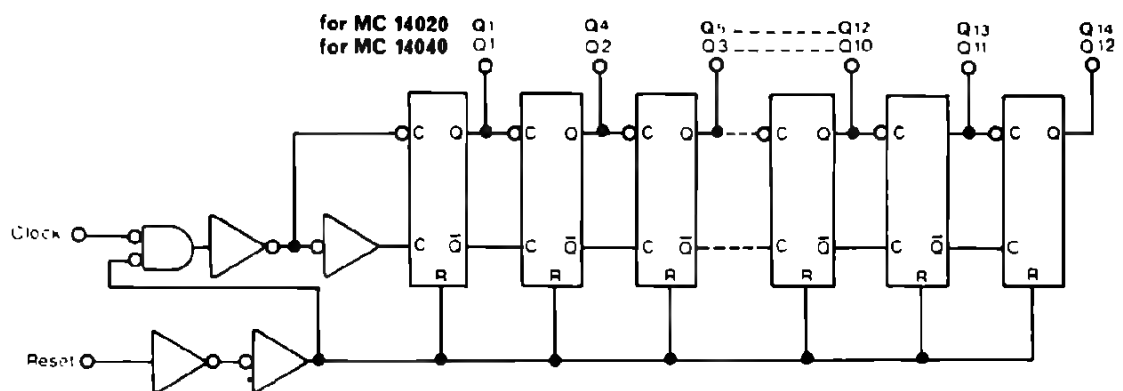
MC14022
Octal Counter/Divider



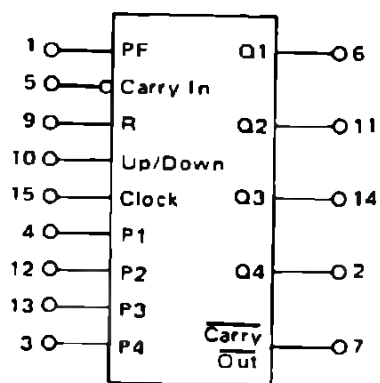
MC14024
7-Stage Binary Counter



MC14040
12-Bit Binary Counter

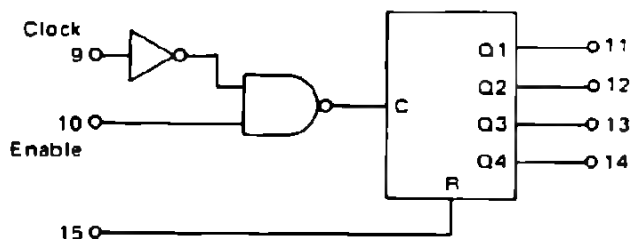
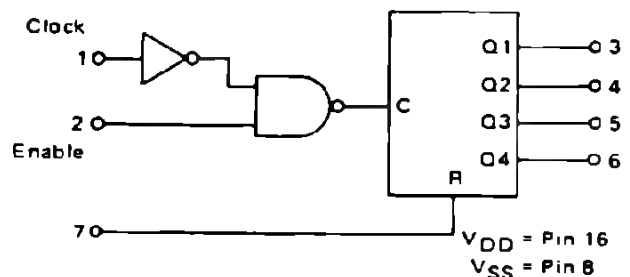


MC14510 – BCD } Up/Down Counters
MC14516 – Binary }

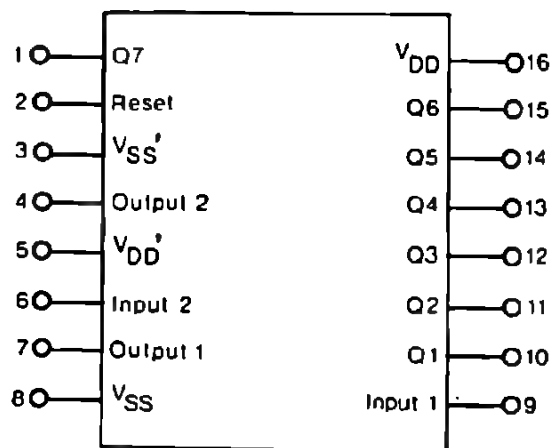


V_{DD} = Pin 16
 V_{SS} = Pin 8

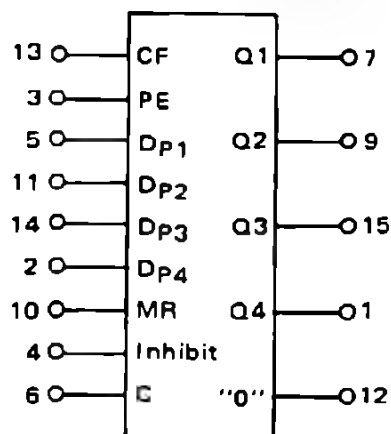
MC14518 – Dual BCD } Up Counters
MC14520 – Dual Binary }



MC14521
24-Stage Frequency Divider

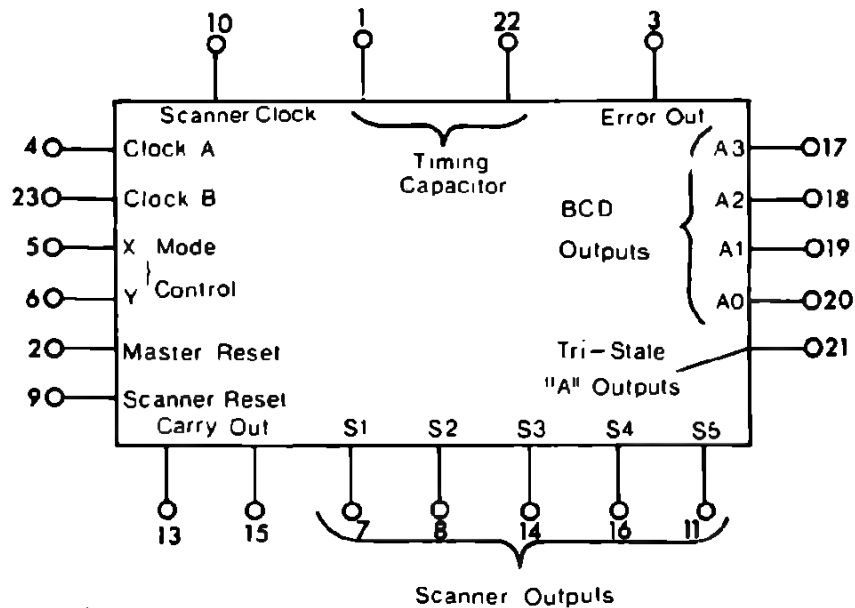


MC14522 – BCD } Programmable
MC14526 – Binary } Divide-by-N
4-Bit Counters



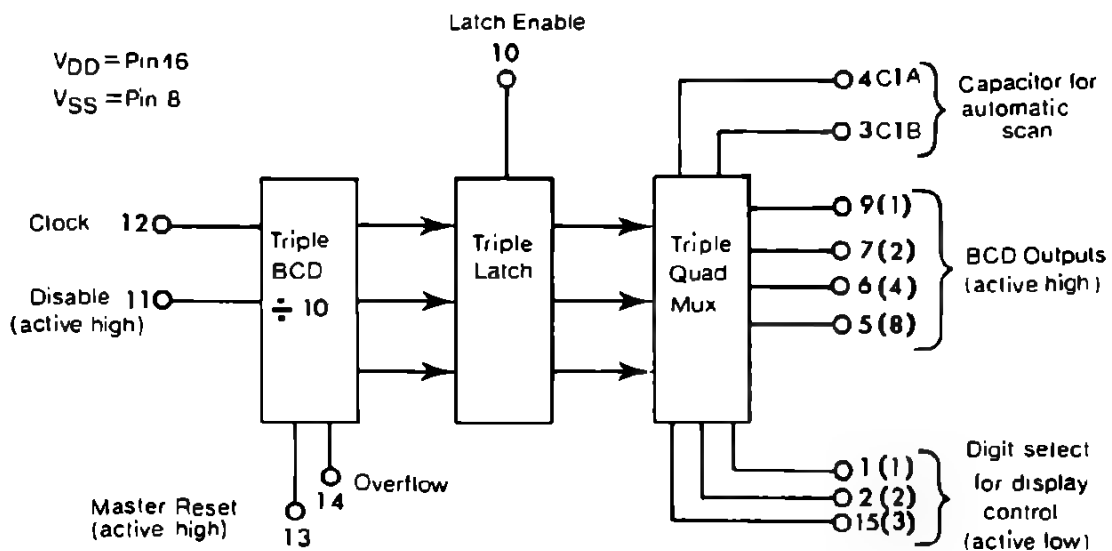
V_{DD} = Pin 16
 V_{SS} = Pin 8

MC14534
5-Stage Decade Counter



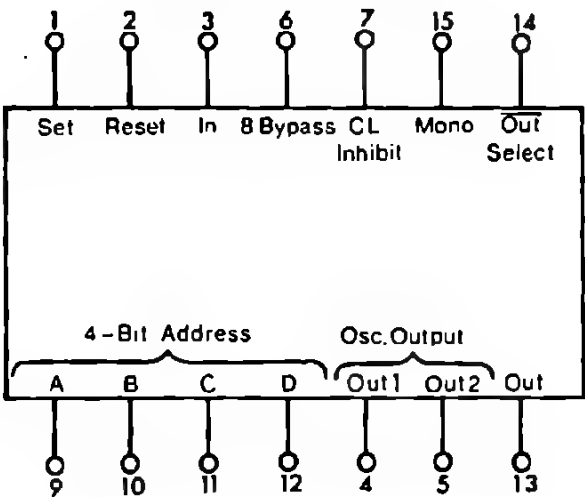
Tri-State "S" Outputs = Pin 15
V_{DD} = Pin 24
V_{SS} = Pin 12

MC14553
3-Digit Counter



TIMERS

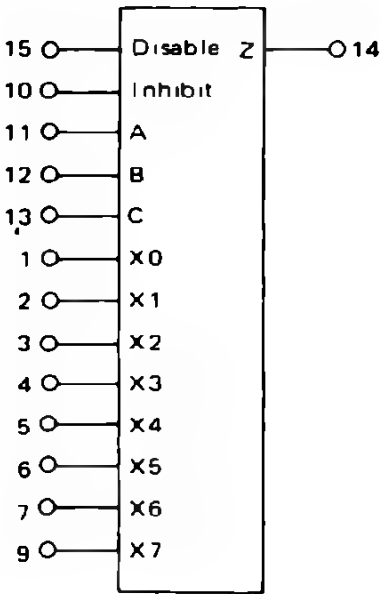
MC14536
Programmable Counter/Timer



MC14566
Industrial Time Base Generator

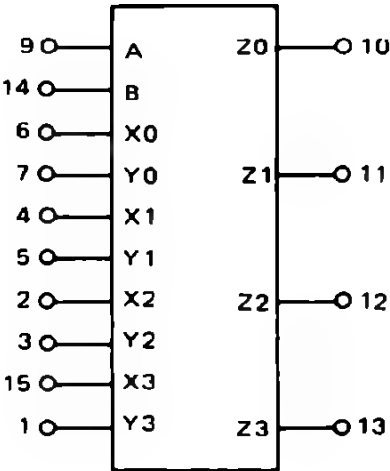
DATA ROUTING FUNCTIONS

MC14512
8-Channel Data Selector



V_{DD} = Pin 16
 V_{SS} = Pin 8

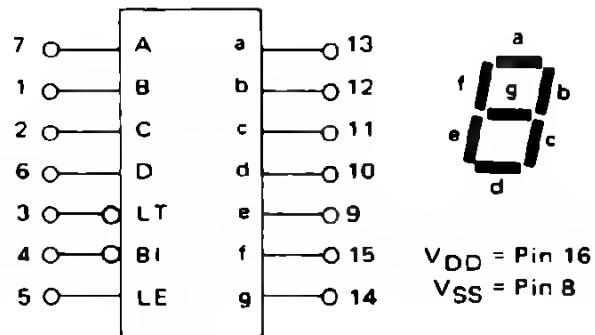
MC14519
4-Bit AND/OR Selector
 or
Quad 2-Channel Data Selector
 or
Quad Exclusive NOR Gate



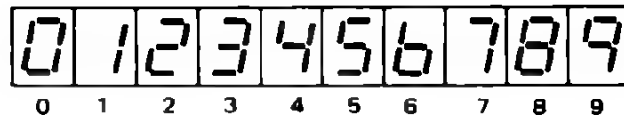
V_{DD} = Pin 16
 V_{SS} = Pin 8

DISPLAY DECODER/DRIVERS

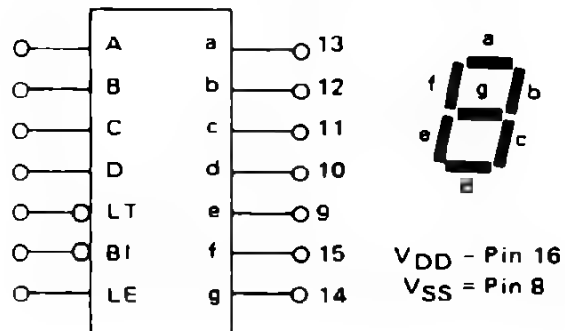
MC14511 BCD-to-Seven Segment Latch/Decoder/Driver



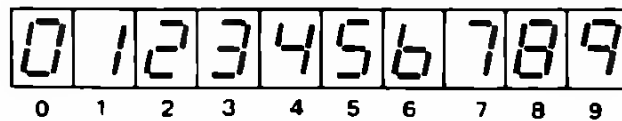
DISPLAY



MC14543 BCD-to-7 Segment Latch/Decoder/Liquid Crystal Driver

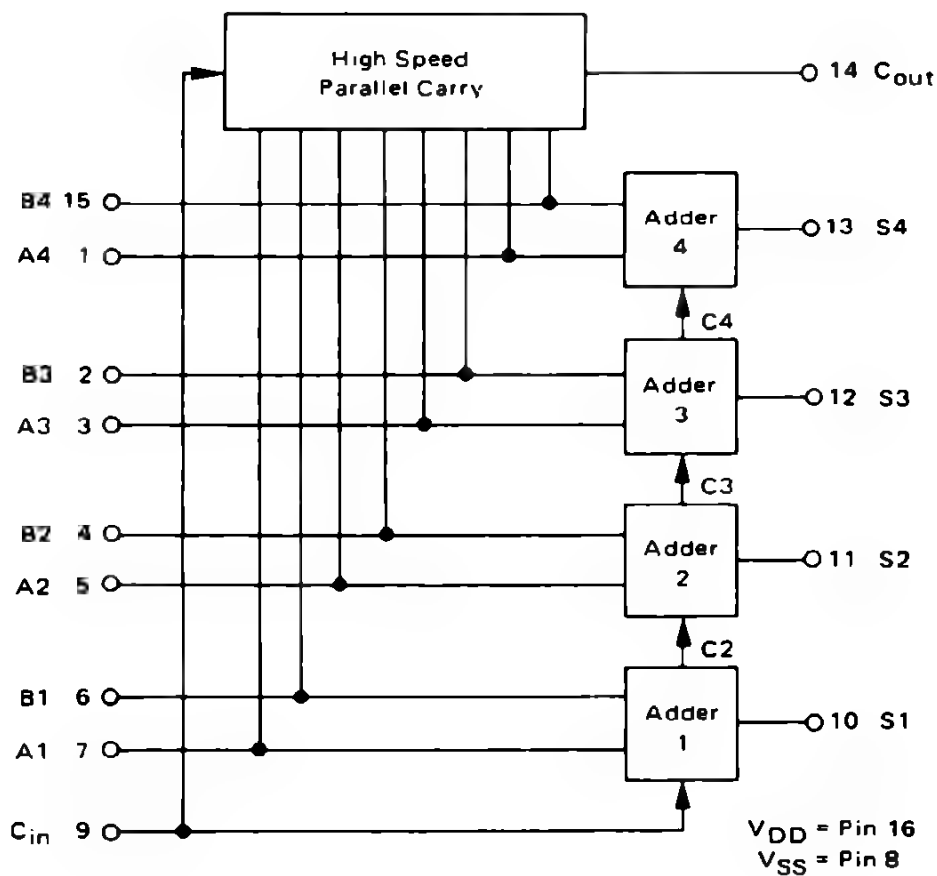


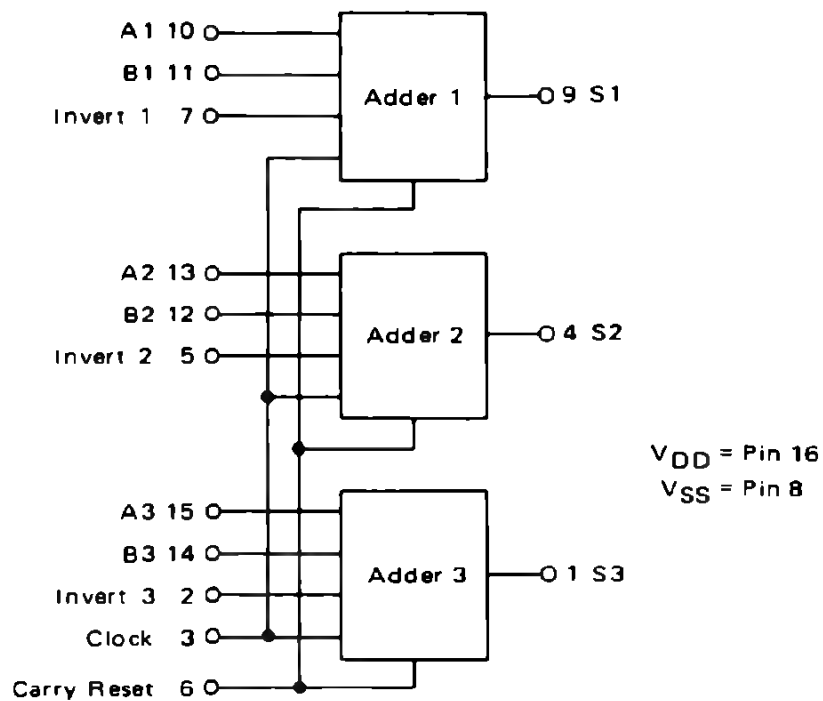
DISPLAY



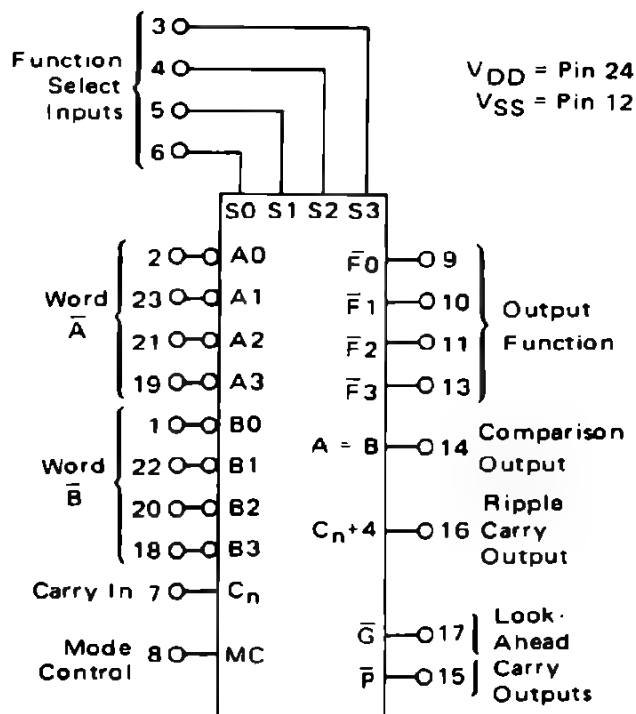
ARITHMETIC FUNCTIONS

MC14008
4-Bit Full Adder

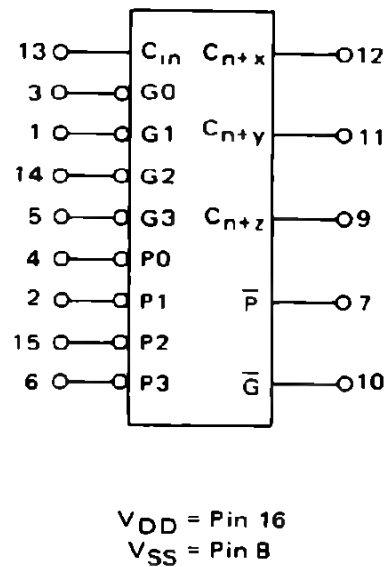




MC14581
Arithmetic Logic Unit

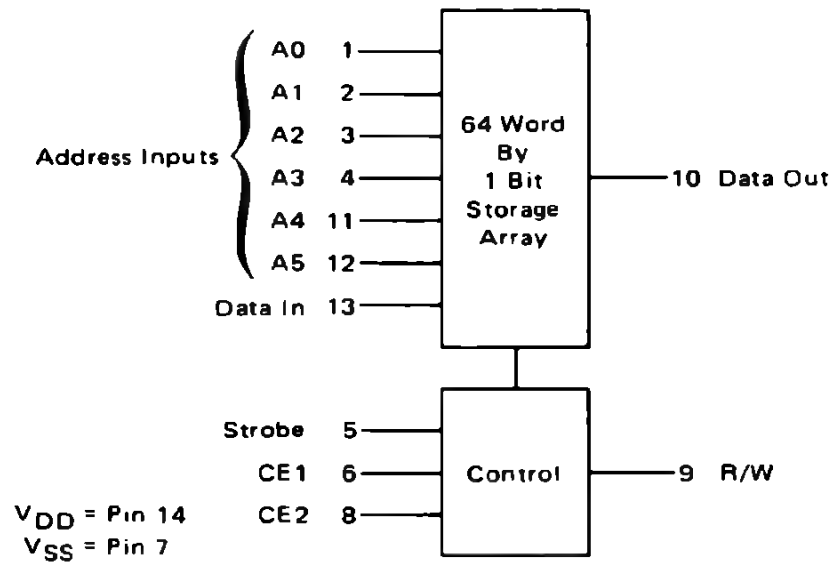


MC14582
Look-Ahead Carry Block

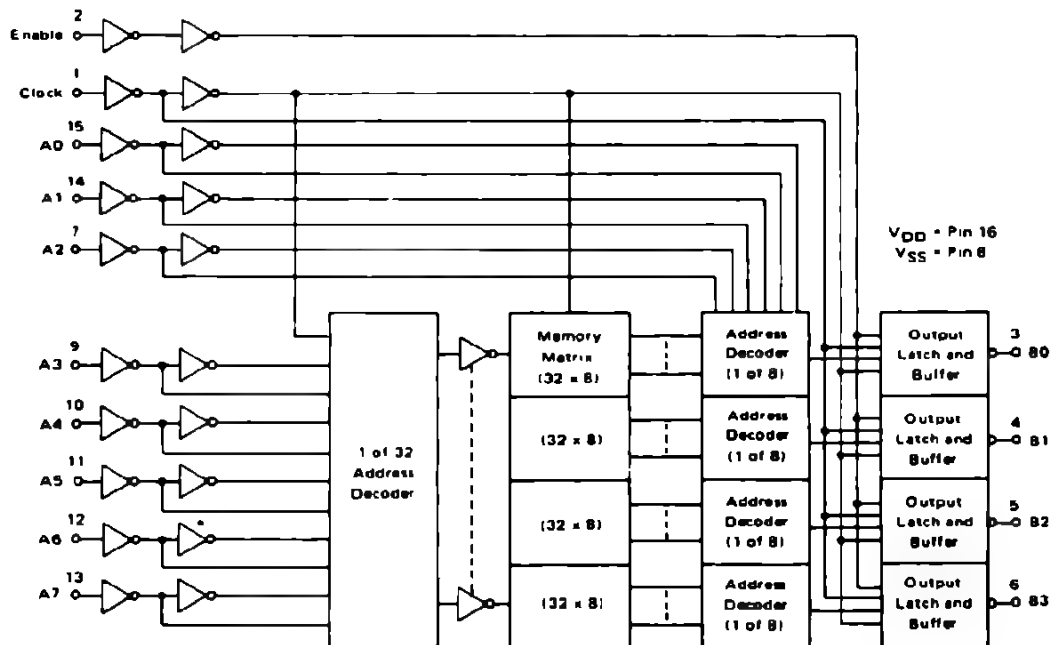


MEMORIES

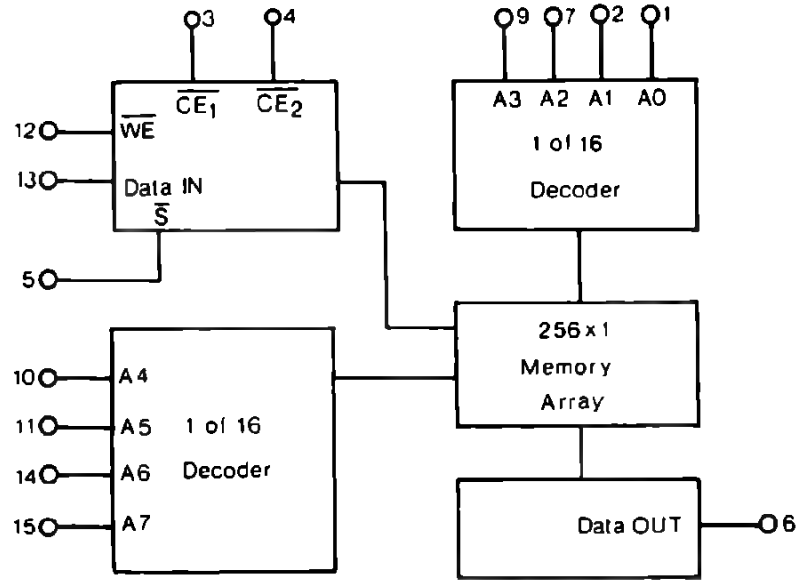
MCM14505 64-Bit Random Access Read-Write Memory



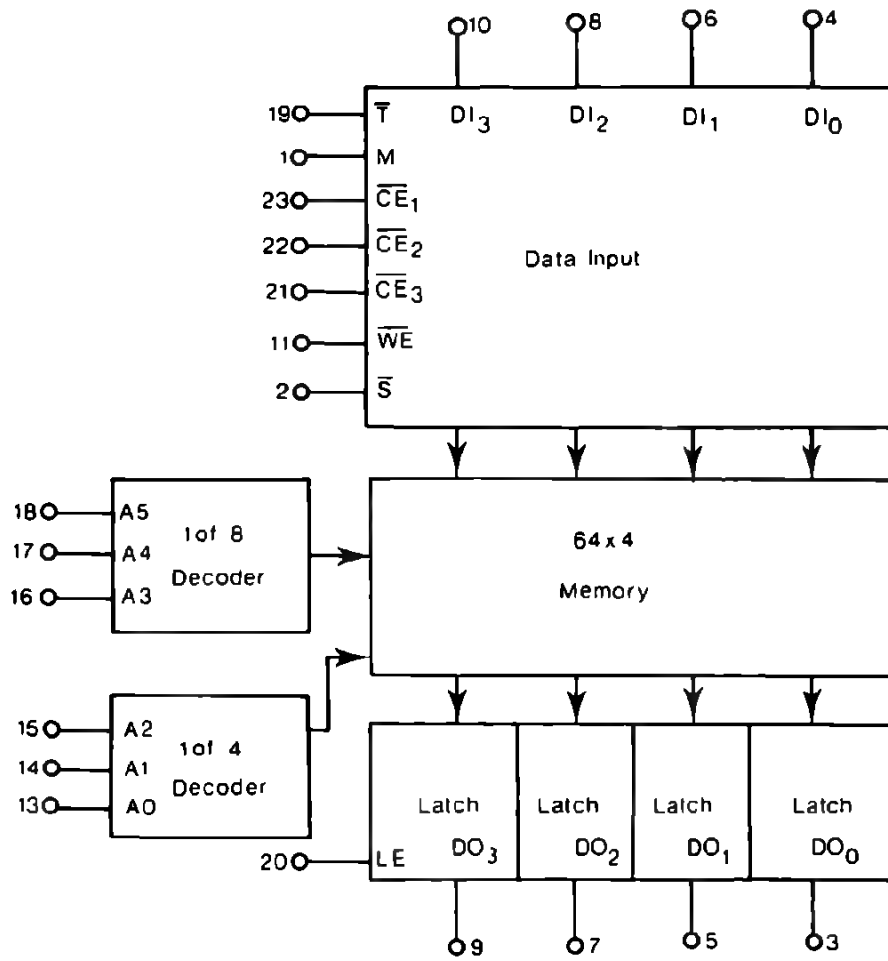
MCM14524 1024-Bit Read Only Memory



256 x 1-Bit RAM

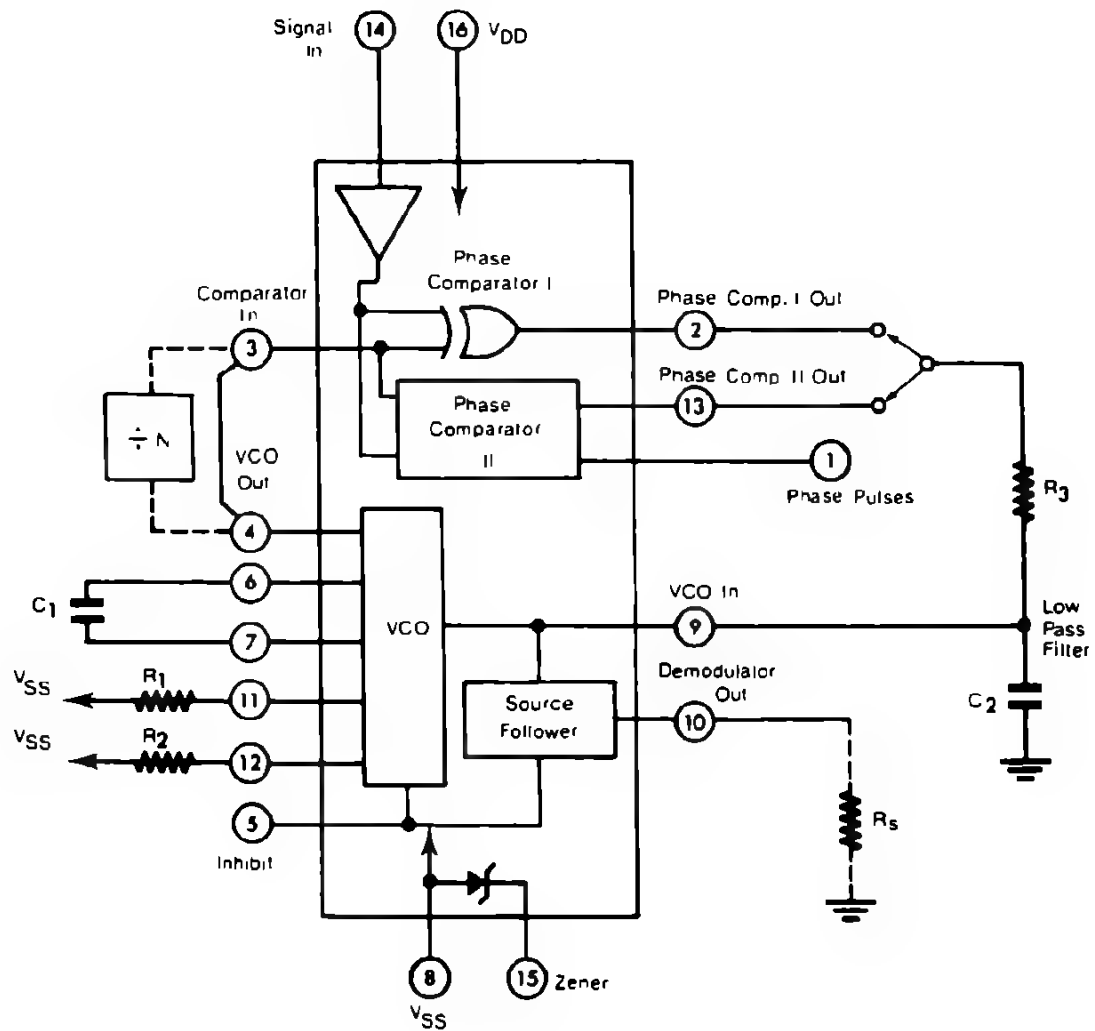


64 x 4 RAM

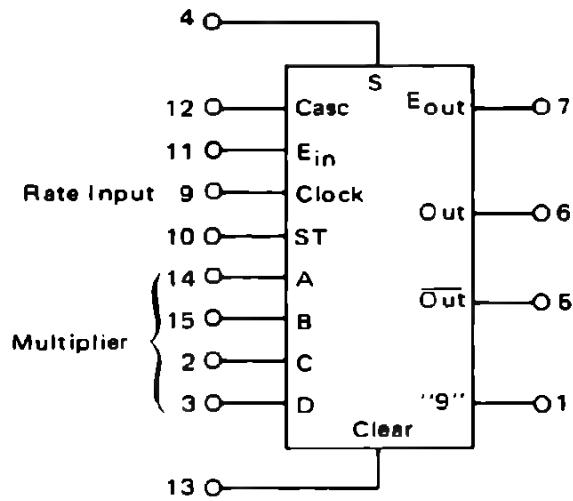


SPECIAL FUNCTIONS

MC14046 Phase Comparator

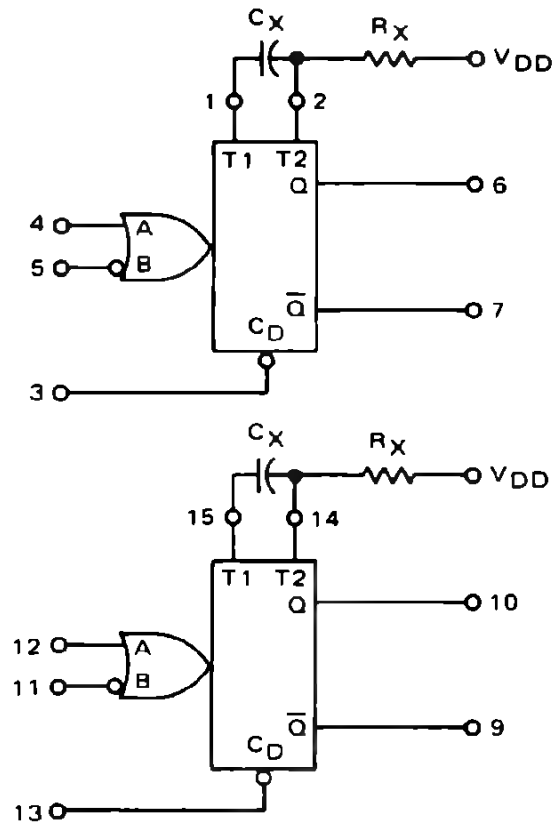


MC14527
BCD Rate Multiplier



V_{DD} = Pin 16
V_{SS} = Pin 8

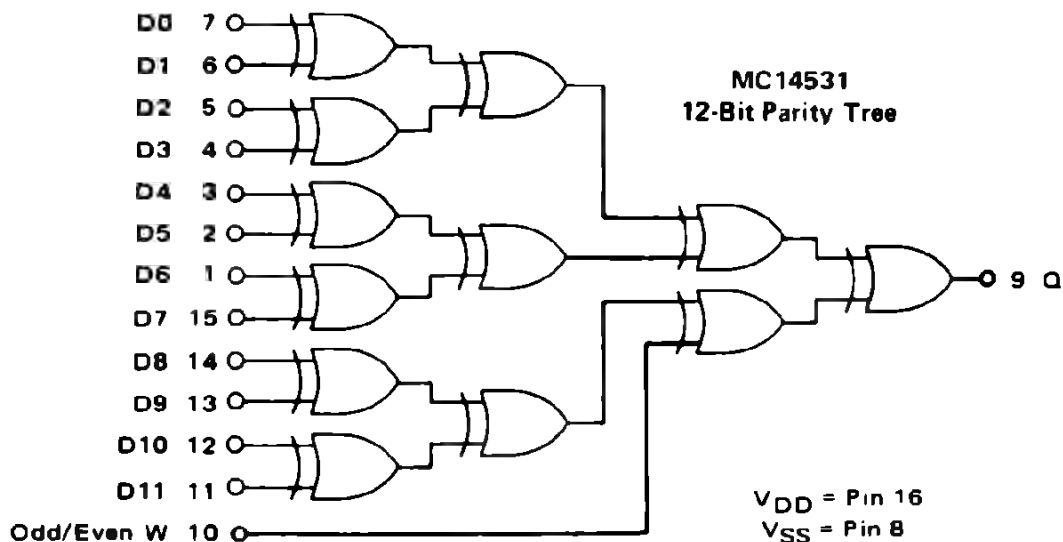
MC14528
Dual Retriggerable/Resettable
Monostable Multivibrator



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

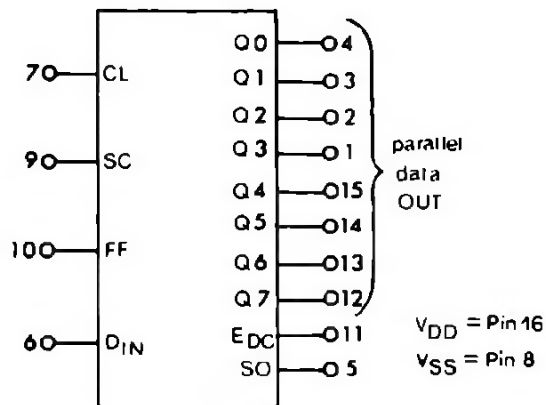
MC14531
12-Bit Parity Tree



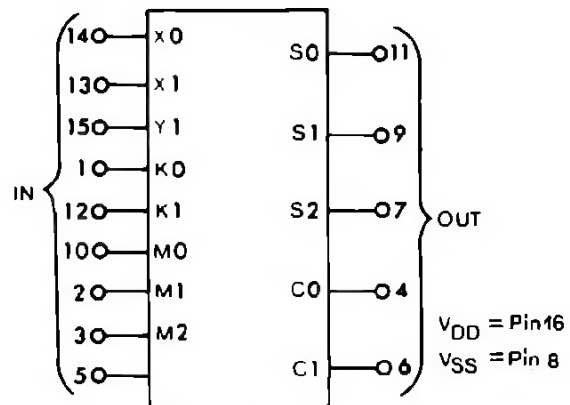
V_{DD} = Pin 16
V_{SS} = Pin 8

$$Q = D0 \oplus D1 \oplus D2 \oplus \dots \oplus D11 \oplus W$$

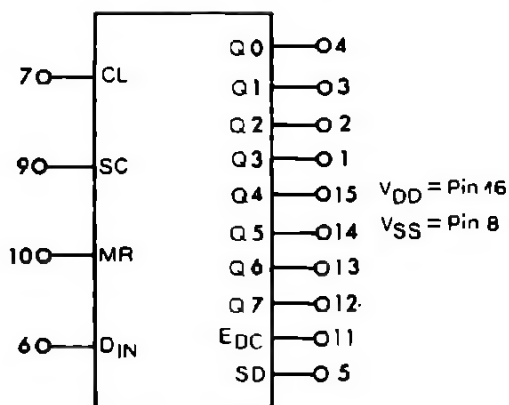
MC14549
Successive Approximation
Analog/Digital Register



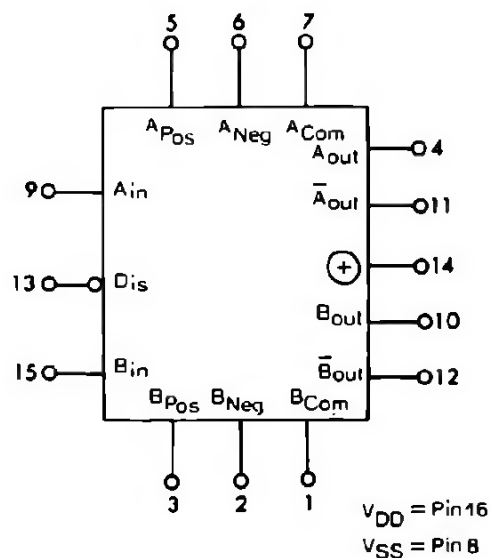
MC14554
2 x 2 Bit Flow Through
Multiplier



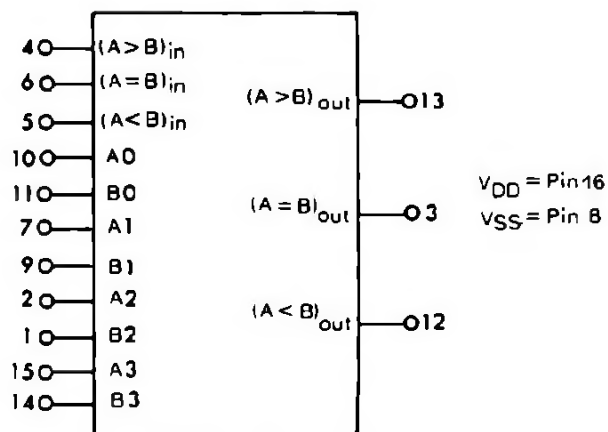
MC14559
Cascadable Successive
Approximation A/D Register



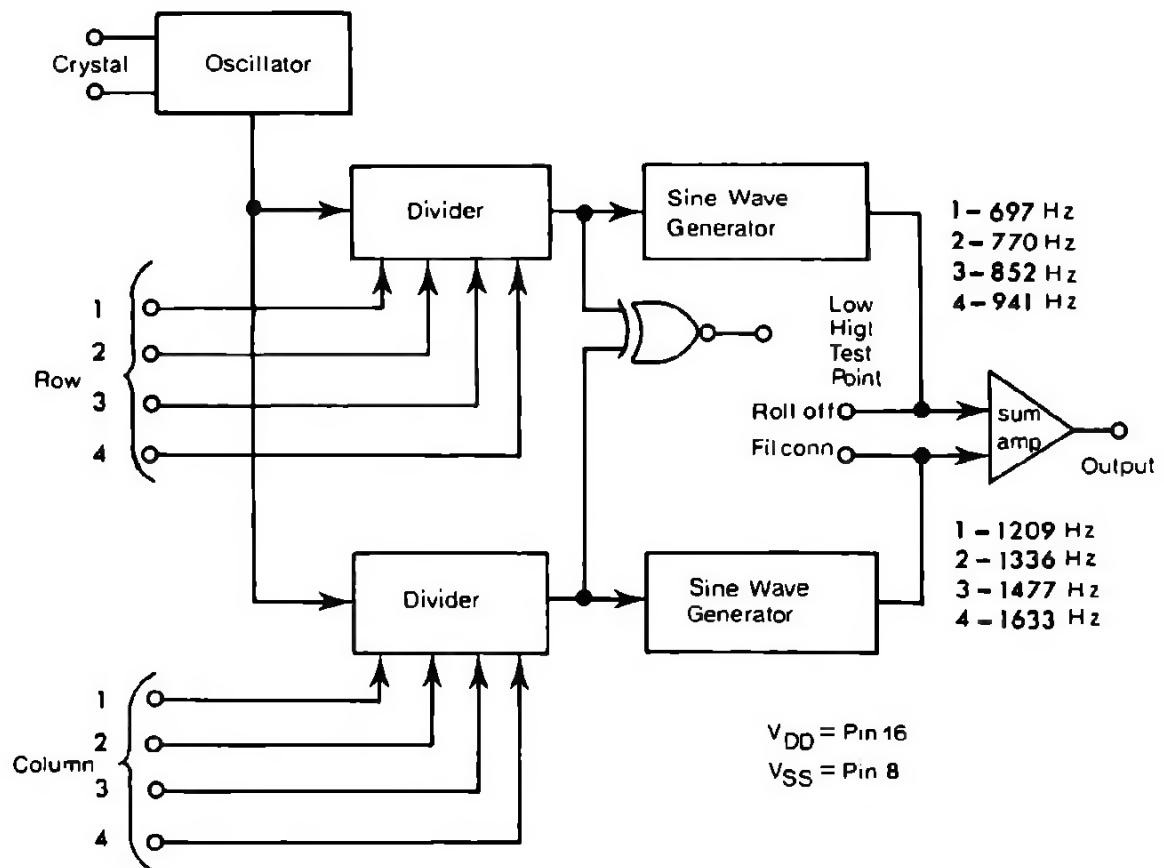
MC14583
Dual Schmitt Trigger

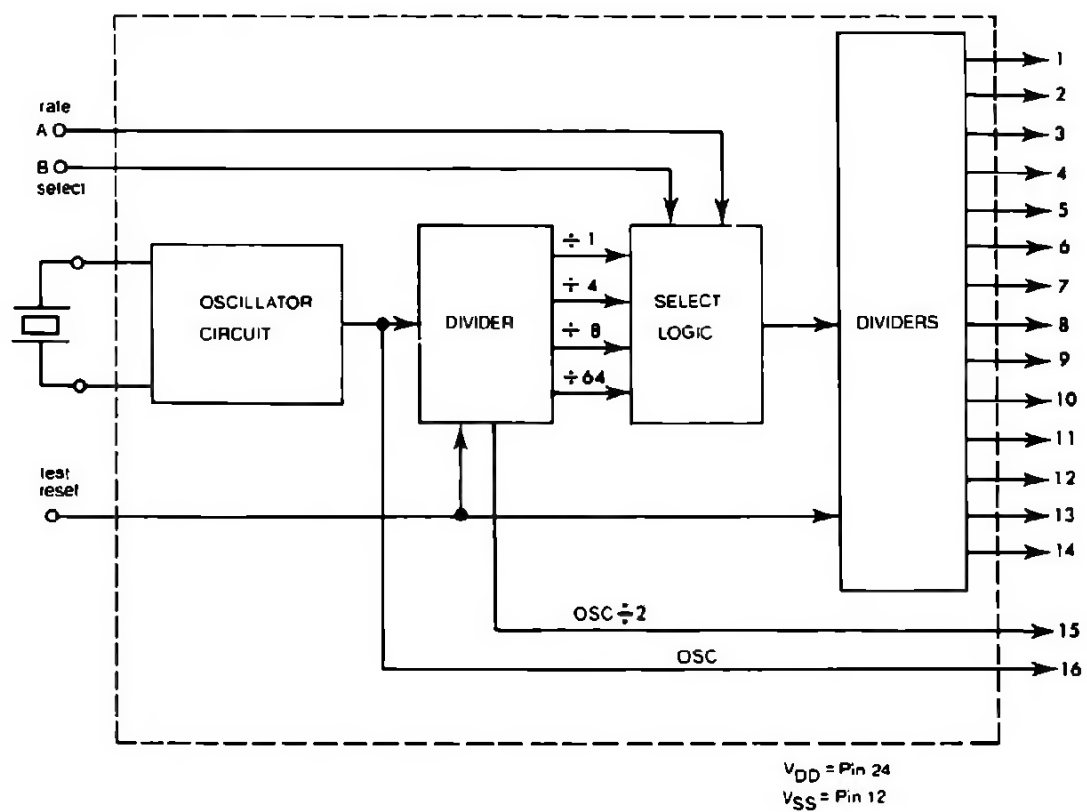


MC14585
4-Bit Magnitude Comparator



MC14410
Touch Tone Encoder





MC14435
3½ Digit DVM

